

32M-Bit (2M × 16) CMOS MASK ROM

FEATURES

- 2,097,152 × 16 bit organization
- Fast access time: 150ns (max.)
- Supply voltage: single +5V
- Current consumption
Operating: 60mA (max.)
Standby: 50 μ A (max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable chip enable and output enable pin
- Package: 42-pin, 600 mil, plastic DIP (JEDEC standard)

GENERAL DESCRIPTION

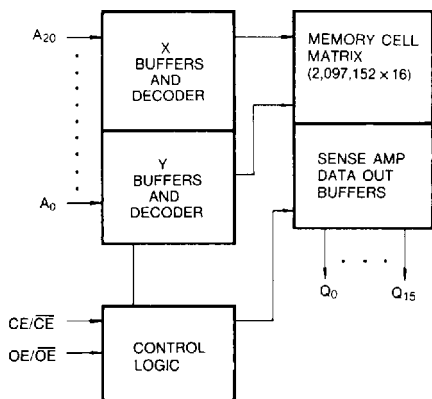
The KM23C32000 is a fully static mask programmable ROM organized 2,097,152 × 16 bit. It is fabricated using silicon gate CMOS process technology.

This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C32000 is packaged in a 42-DIP, provides polarity programmable CE and OE buffer as user option mode.

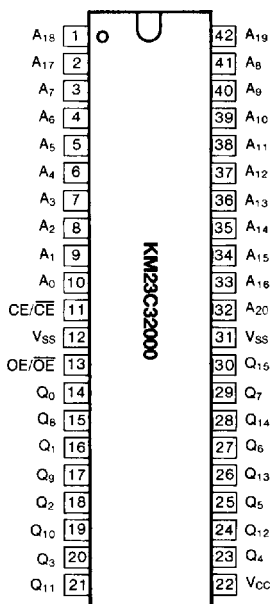
FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A ₀ -A ₂₀	Address Inputs
Q ₀ -Q ₁₅	Data Outputs
CE/CE*	Chip Enable
OE/OE*	Output Enable
V _{CC}	Power (+ 5V)
V _{SS}	Ground

* User Selectable Polarity

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN}	-0.3 to +7.0	V
Temperature Under Bias	T _{bias}	-10 to + 85	°C
Storage Temperature	T _{stg}	-55 to +150	°C

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I _{CC}	CE = OE = V _{IL} , f = 6.7MHz all output open	—	60	mA
Standby Current (TTL)	I _{SB1}	CE = V _{IH} , all output open	—	1	mA
Standby Current (CMOS)	I _{SB2}	CE = V _{CC} , all output open	—	50	μA
Input Leakage Current	I _{LI}	V _{IN} = 0 to V _{CC}	—	10	μA
Output Leakage Current	I _{LO}	V _{OUT} = 0 to V _{CC}	—	10	μA
Input High Voltage, All Inputs	V _{IH}		2.2	V _{CC} + 0.3	V
Input Low Voltage, All Inputs	V _{IL}		-0.3	0.8	V
Output High Voltage Level	V _{OH}	I _{OH} = -400μA	2.4	—	V
Output Low Voltage Level	V _{OL}	I _{OL} = 2.1mA	—	0.4	V

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C _{OUT}	V _{OUT} = 0V	—	12.0	pF
Input Capacitance	C _{IN}	V _{IN} = 0V	—	12.0	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE/CE	OE/OE	Mode	Data	Power
L/H	X	Standby	High-Z	Standby
H/L	L/H	Operating	High-Z	Active
	H/L	Operating	D _{OUT}	Active

AC CHARACTERISTICS

(Ta=0° to +70°C, Vcc=5V± 10%, unless otherwise noted.)

TEST CONDITIONS

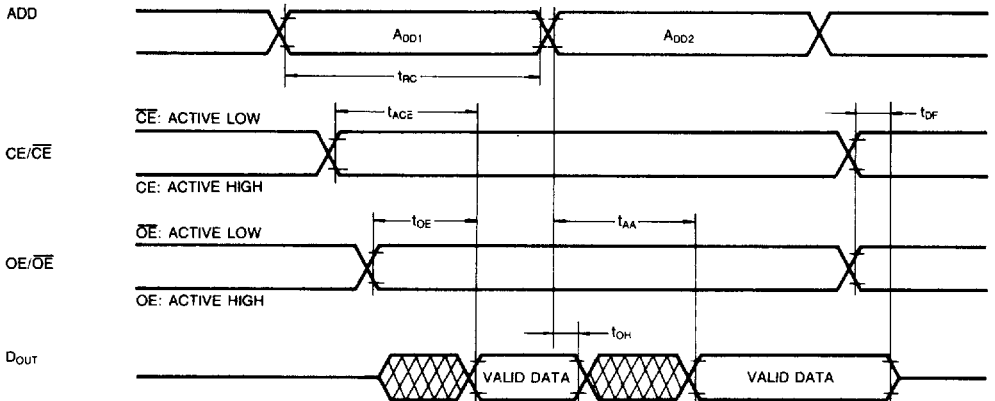
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL = 100pF

READ CYCLE

Parameter	Symbol	KM23C32000(G)-15		KM23C32000(G)-20		KM23C32000(G)-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	150		200		250		ns
Chip Enable Access Time	t _{ACE}		150		200		250	ns
Address Access Time	t _{AA}		150		200		250	ns
Output Enable Access Time	t _{OE}		70		90		110	ns
Output or Chip Disable to Output High-Z	t _{DF}		30		40		50	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns

TIMING DIAGRAM

READ



* After power up, in order to prevent wrong operation of special application, dummy cycle of CE or any address input (Min. 80ns) is required.

PACKAGE DIMENSIONS

42 LEAD PLASTIC DUAL IN LINE PACKAGE (KM23C32000)

Unit: Inches (mm)

