Eclipse: Combining Performance, Density, and Embedded RAM

Updated 8/24/2000

DEVICE HIGHLIGHTS

Flexible Programmable Logic

- .25u, 5 layer metal CMOS process
- 2.5 V Vcc, 2.5/3.3 V drive capable I/O
- 1.5 watts
- Up to 4032 SuperCells
- Up to 583,000 Max System Gates
- Up to 512 I/O

Embedded Dual Port SRAM

- Up to 36-2,304 bit Dual Port High performance SRAM Blocks
- Up to 82,900 RAM bits
- RAM/ROM/FIFO Wizard for automatic configuration
- Configurable and Cascadable

Phase Lock Loop (PDLL)

- 4 PLL/DLLs
- Jitter<200 ps, Lock time <10 us
- Capture and Lock range: 25 to 250 MHz
- Programmable Multiply/Divide: 1x, 2x, 4x

Programmable I/O

- High performance Enhanced I/O (EIO): Less than 3 ns Tco
- Programmable Slew Rate Control
- Programmable I/O Standards
- LVTTL, LVCMOS, PCI, GTL+, SSTL2,and SSTL3
- 8 Independent I/O Banks
- 3 Register Configuration: Input, Output, OE

Advanced Clock Network

- 9 Global Clock Networks
- 1 dedicated
- 8 programmable
- 16 I/O (high drive) networks: 2 I/Os per bank
- 20 Quad-Net Networks: 5 per quadrant

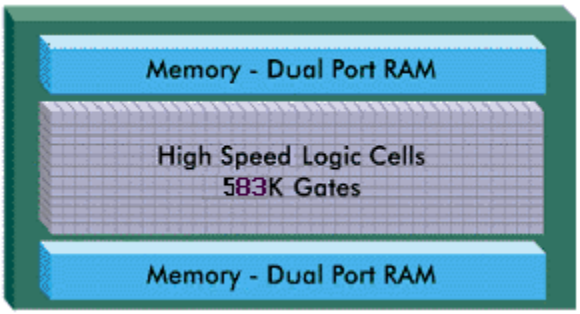

FIGURE 1. Embedded Eclipse Block Diagram

		QL6250	QL6325	QL6500	QL6600
Max Gates		248,160	320,640	488,064	583,008
Logic Array		40x24	48x32	64x48	72x56
Logic Cells		960	1,536	3,072	4,032
Max Flip-Flops		2,688	4,302	7,488	9,600
Max I/O		256	320	448	512
RAM Modules		20	24	32	36
RAM bits		46,100	55,300	73,700	82,900
Packages	PQFP	208	208		
	BGA (1.27mm)	516	516	516	516
	BGA (1.0mm)	484	484	484, 672	484, 672
	FPBGA (0.8mm)	280	280	280	280

TABLE 1. Eclipse Product Family Members

QuickWorks Design Software

The turnkey QuickWorks package provides the most complete ESP and FPGA software solution from design entry to logic synthesis, to place and route to simulation. The packages provide a solution for designers who use third party tools from Cadence, Mentor, OrCAD, Synopsys, Viewlogic, Veribest and other third-party tools for design entry, synthesis, or simulation.

Process Data

Eclipse is fabricated on a .25u 5 layer metal CMOS process. The core voltage is 2.5 volt Vcc supply and 3.3 tolerant I/O with the addition of 3.3 volt Vccio. Eclipse is available in commercial, industrial, and military temperature grades.

Programmable Logic Architectural Overview

The Eclipse features an enhanced Supercell with an additional D flip-flop register and associated control logic. This advanced architectural approach, addresses today's highly register intensive designs.

Function	Description	Slowest speed grade	Fastest speed grade
Multiplexer	16:1	5 ns	2.8 ns
Parity Tree	24	6 ns	3.4 ns
	36	6 ns	3.4 ns
Counter	16 bit	250 MHz	450 MHz
	32 bit	250 MHz	450 MHz
FIFO	128 x 32	155 MHz	280 MHz
	256 x 16	155 MHz	280 MHz
	128 x 64	155 MHz	280 MHz
Clock to out		4.5 ns	2.5 ns
System clock		200 MHz	400 MHz

TABLE 2. Performance Standards

The Eclipse logic Supercell structure, Figure 2, is similar to the .35 mm QuickLogic logic cell with the addition of a second register. Both registers share CLK, SET and RESET inputs. The second register has a two-to-one multiplexer controlling its input. The register can be loaded from the NZ output or directly from a dedicated input. NOTE: The input "PP" is not an "input" in the classical sense. It can only be tied high or low using default links only and is used to select which path "NZ" or "PS" is used as an input to the register. All other inputs can be connected not only to "tiehi" and "tielo" but to multiple routing channels as well.

The complete logic cell consists of two 6-input AND gates, four two-input AND gates, seven two-to-one multiplexers and two D flip-flop with asynchronous SET and RESET controls. The cell has a fan-in of 30 (including register control lines) and fits a wide range of functions with up to 17 simultaneous inputs. It has 6 outputs, 4 combinatorial and 2 registered. The high logic capacity and fan-in of the logic cell accommodate many user functions with a single level of logic delay while other architectures require two or more levels of delay

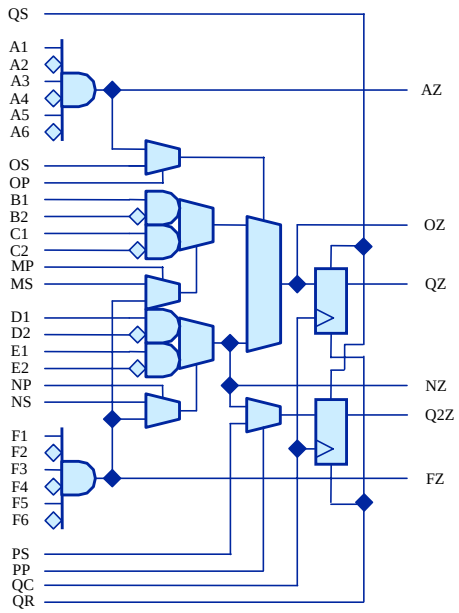

FIGURE 2. Eclipse SuperCell

RAM Modules

The Eclipse Family includes multiple dual-port 2,304-bit RAM modules for implementing RAM, ROM and FIFO functions. Each module is user-configurable into four different block organizations. Modules can also be cascaded horizontally to increase their effective width or vertically to increase their effective depth as shown in Figure 3. The RAM can also be configured as a modified Harvard Architecture, similar to those found in DSPs.

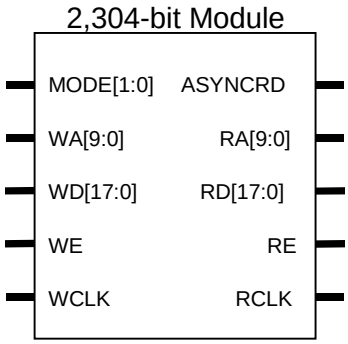

FIGURE 3. 2,304-bit QuickRAM Module

The number of RAM modules varies from 12 to 36 blocks within the Eclipse family, for a total of 46.1K to 82.9k bits of RAM. Using two "mode" pins, designers can configure each module into 128 x 18 (Mode 0), 256 x 9 (Mode 1), 512 x 4 (Mode 2), or 1024 x 2 blocks (Mode 3). The blocks are also easily cascadable to increase their effective width and/or depth. See figure 4.

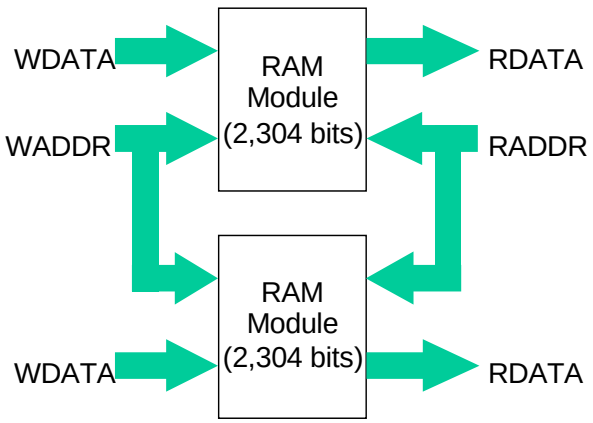

FIGURE 4. Cascaded RAM Modules

The RAM modules are dual-port, with completely independent READ and WRITE ports and separate READ and WRITE clocks. The READ ports support asynchronous and synchronous operation, while the WRITE ports support synchronous operation. Each port has 18 data lines and 10 address lines, allowing word lengths of up to 18 bits and address spaces of up to 1024 words. Depending on the mode selected, however, some higher order data or address lines may not be used.

The Write Enable (WE) line acts as a clock enable for synchronous write operation. The Read Enable (RE) acts as a clock enable for synchronous READ operation (ASYNCRD input low), or as a flow-through enable for asynchronous READ operation (ASYNCRD input high).

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules.

A similar technique can be used to create depths greater than 512 words. In this case address signals higher than the ninth bit are encoded onto the write enable (WE) input for WRITE operations. The READ data outputs are multiplexed together using encoded higher READ address bits for the multiplexer SELECT signals.

The RAM blocks can be loaded with data generated internally (typically for RAM or FIFO functions) or with data from an external PROM (typically for ROM functions). The RAM achieve 155 MHz performance for the lowest speed grade devices when using multiple blocks cascaded together.

Multiple Accessing of Memories

The extremely fast RAM can be used in designs that require multiple memory accessing. The RAM achieves 280 MHz performance for the fastest speed grade and 155 MHz performance for the lowest speed grade devices when using multiple blocks cascaded together. Write through of DATA is also possible with the QuickLogic RAM.

PLL

Phase Lock Loops (PLLs), also known as frequency synthesizers, are used to create a master clock from a lower input frequency clock in DSPs. There are four PLLs in the Eclipse family, one is multiplexed with the dedicated clock and the remaining three connect to global clocks. The PLLs have a frequency range of 25MHz to 250MHz. Frequency synthesis can also be created in increments of multiply by 2, 4 and divide by 2, 4. In addition, there is an early clock option to further reduce the TCO of a system and a PLL output option to drive external devices. A lock detect signal is provided to indicate a PLL is in lock.

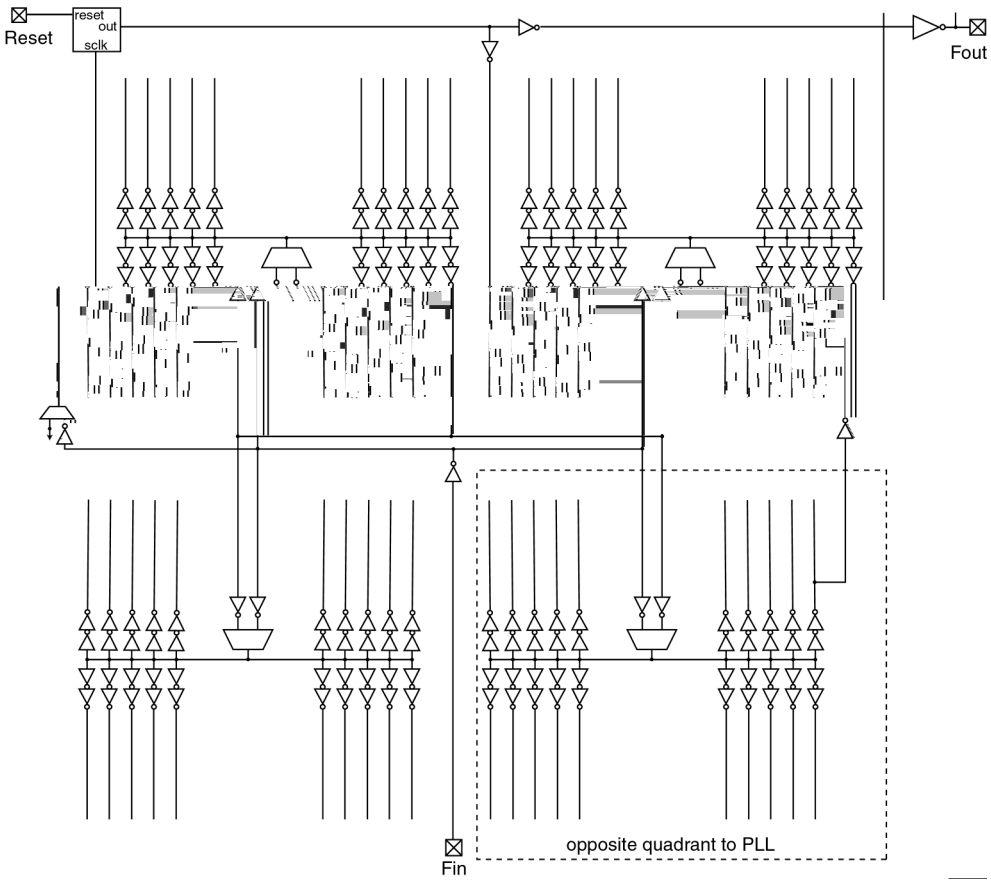

FIGURE 5. PLL Clock Network

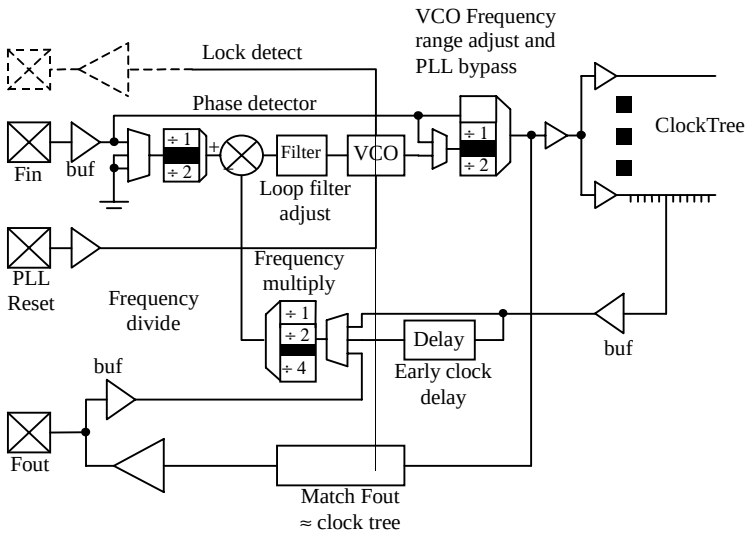

FIGURE 6. PLL Block Diagram

PLL Features

- Phase and frequency lock
- Lock range: 25 MHz to 250 MHz
- Jitter: < 200 ps across all ranges
- Lock time: <200 steps or <10 us (which ever is less)
- Early clock option for Tco <= 3 ns
- No external components
- Frequency multiply and divide @ 4X, 2X, 1X, 0.5X input frequency
- Lock detect for system start-up
- Phased locked output option @ 4X, 2X, 1X, 0.5X input frequency
- PLL standby/bypass mode

I/O Cell Structure

Eclipse features a variety of distinct I/O pins to maximize performance, functionality, and flexibility with bi-directional I/O pins and input-only pins. All input and I/O pins are 2.5V and 3.3V tolerant and comply with the specific I/O standard selected. The outputs swing from Vss to VCCI/O (0V to 3.3V ± 10%). The VCCI/O pins must be tied to a 3.3V supply to provide 3.3V compliance. If 3.3V compliance is not required, then these pins must be tied to the 2.5V supply. Eclipse can also support LVDS and LVPECL I/O standards with the addition of an external resistor. Table 3 summarizes the I/O specifications that will be supported.

I/O Standard	Reference Voltage	Output Voltage	Application
LVTTL	n/a	3.3	general purpose
LVCMOS2	n/a	2.5	general purpose
PCI	n/a	3.3	PCI bus applications
GTL+	1	n/a	high speed bus - Pentium Pro
SSTL3	1.5	3.3	memory bus - Hitachi, IBM
SSTL2	1.25	2.5	memory bus - Hitachi, IBM

TABLE 3. I/O Standards and Applications

As designs become more complex and requirements more stringent, varying I/O standards are developing for specific applications. I/O standards for processors, memories and various bus applications have become common place and a requirement for many systems. In addition, I/O timing has become a greater issue with specific requirements for setup, hold, clock to out, and switching times.

The Eclipse family has addressed these changing system requirements. The Eclipse family includes a completely new I/O cell which consists of programmable I/Os as well as a new cell structure consisting of 3 registers - input, output and output enable. Eclipse will offer banks of programmable I/O that addresses many of the new bus standards that are popular today. In addition, the input register addresses the setup time; the output register addresses clock-to-out time; and the OE register addresses the switching time from high impedance to a given value.

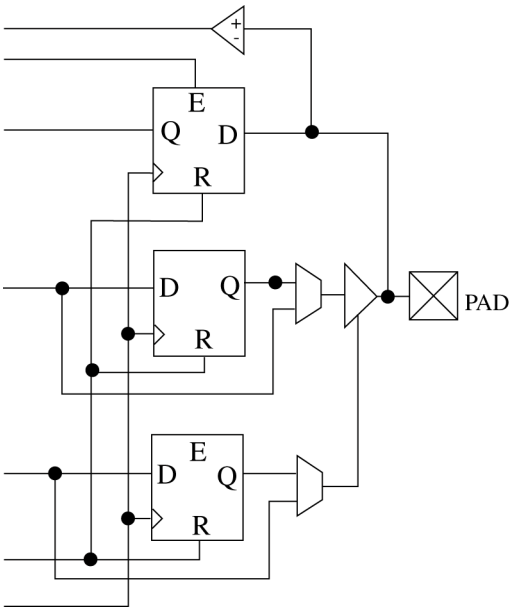

FIGURE 7. Eclipse I/O Cell

The bi-directional I/O pin options can be programmed for input, output, or bi-directional operation. As shown in Figure 7, each bi-directional I/O pin is associated with an I/O cell which features an input/feedback register, an input buffer, output/feedback register, three-state output buffer, an output enable register, and two (2) two-to-one multiplexers.

For input functions, I/O pins can provide combinatorial, registered data or both options simultaneously to the logic array. For combinatorial input operation, data is routed from I/O pins through the input buffer to the array logic. For registered input operation, I/O pins drive the D input of input cell registers, allowing data to be captured with fast set-up times without consuming internal logic cell resources.

For output functions, I/O pins can receive combinatorial or registered data from the logic array. For combinatorial output operation, data is routed from the logic array through a multiplexer to the I/O pin. For registered output operation, the array logic drives the D input of the output cell register which in turn drives the I/O pin through a multiplexer. The multiplexer allows either a combinatorial or a registered signal to be driven to the I/O pin.

The three-state output buffer controls the flow of data from the array logic to the I/O pin and allows the I/O pin to act as an input and/or output. The buffer's output enable can be individually controlled by a logic cell array or any pin (through the regular routing resources), or bank-controlled through one of the global networks. The signal can be also be either combinatorial or registered. This is identical to that of the flow for the output cell. For combinatorial control operation data is routed from the logic array through a multiplexer to the three-state control. For registered control operation, the array logic drives the D input of the OE cell register which in turn drives the three-state control through a multiplexer. The multiplexer allows either a combinatorial or a registered signal to be driven to the three-state control. For output functions, I/O pins can be individually configured for active HIGH, active LOW, or open-drain inverting operation. In the active HIGH and active LOW modes, the pins of all devices are fully 3.3V compliant.

When I/O pins are unused, the OE controls can be permanently disabled, allowing the output cell register to be used for registered feedback into the logic array. I/O cell registers are controlled by clock, clock enable, and reset signals, which can come from the regular routing resources, from one of the global networks, or from two input pins per bank of I/O's. The CLK and RESET signals share a common line, while the clock enables for each register can be independently controlled. Additionally the output and enable

registers will increase a device's register count. The addition of an output register will also decrease the Tco. Since the output register does not need to drive the routing the length of the output path is also reduced.

Extra registers add more inputs and outputs to the I/O structure. Extra routing resources are added to connect the I/O structure to the other parts of the device.

I/O interface support is programmable on a per bank basis. There are 8 I/O banks per chip. Users can not mix 2.5v I/O with 3.3v I/O on the same I/O bank. Figure 5 illustrates the I/O bank configurations.

Each I/O bank is independent of other I/O bank and each I/O bank has it's own VCCIO and VREF supplies. A mixture of different I/O standards can be used on the device, however there is a limitation as to which I/O standards can be supported within a given bank. Differential I/O can be shared with non differential I/O. There can only be one VREF and one VCCIO per bank.

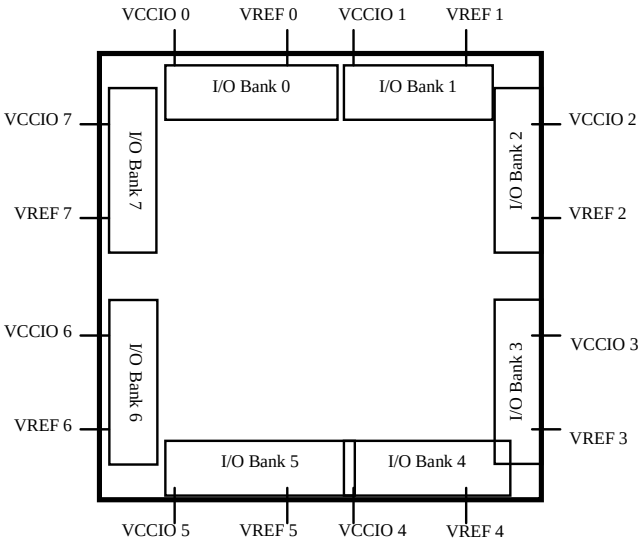

FIGURE 8. Multiple I/O Banks

Programmable Slew Rate

Each I/O has programmable slew rate capability. The rate is programmable to one of two slew rates either fast or slow. The slower rate can be used to reduce ground bounce noise. The slow slew rate is 1 V/ns under typical conditions. The fast slew rate will be 2.8 V/ns

VCCIO = 3.3V	Fast Slew	Slow Slew
Rising Edge	2.8 V/nS	1.0 V/vS
Falling Edge	2.86 V/nS	1.0 V/nS

VCCIO = 2.5V	Fast Slew	Slow Slew
Rising Edge	1.7 V/nS	0.6 V/vS
Falling Edge	1.9 V/nS	0.6 V/nS

Condition: 2.5V, 25C

TABLE 4. Programmable Slew Rate

Programmable Weak Pull-Down

Programmable weak-pull down resistor is available on each I/O. I/O Weak Pull-Down eliminates the need for external pull down resistor for used I/O. The spec for pull-down current is maximum of 150uA under worst case condition. - 148uA @ 3.6V, -55C, - 69 uA@ 2.5V, 25C.

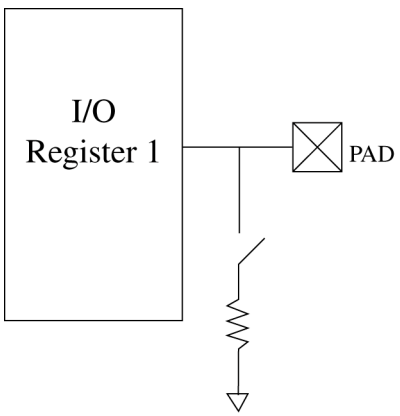

FIGURE 9. I/O Weak Pull-Down

Clock Networks

Global Clocks

There are 8 global clock networks in the Eclipse device family. Global clocks can drive logic cell, I/O, and RAM registers in the device. Three Global clocks will each have access to a PLL. Five global clocks will have access to a Quad Net (local clock network) connection with a programmable connection to the register inputs.

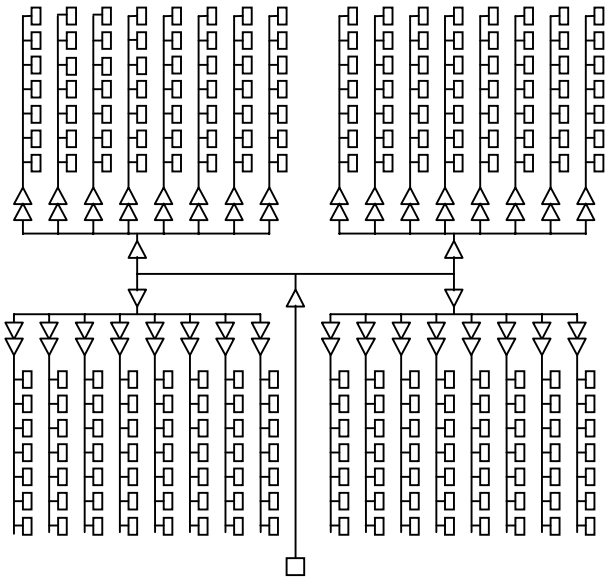

FIGURE 10. Global Clock Methodology

Quad-Net NETWORK

There are 5 Quad-Net local clock networks in each quadrant for a total of 20 in a device. Each Quad-Net is local to a quadrant. Quad-Net is multiplexed with the clock buffer before driving the column clock buffers.

Dedicated Clock

There is one dedicated clock in the Eclipse device family. It connects to the clock input of the SuperCell, I/O and RAM registers through a hardwired connection and is multiplexed with the programmable clock input. There are four inversions from pad to register inputs and the dedicated clock takes on the same configuration as the global clock. The dedicated clock provides a fast global network with low skew. The dedicated clock has access to one of four PLL's. You have the ability to select either the dedicated clock or the programmable clock, Figure 11. The performance of the dedicated clock is given in Table 5.

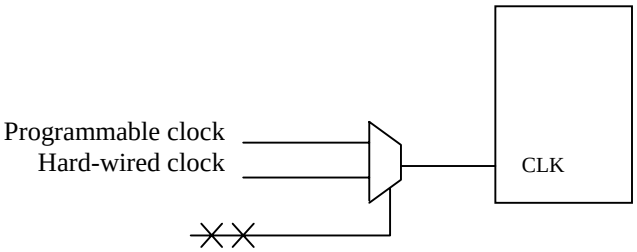

FIGURE 11. Dedicated clock circuitry within logic cell

	Clock Performance	
TT, 25C, 2.5V	Global	Dedicated
Macro (near)	1.51 ns	1.59 ns
I/O (far)	2.06 ns	1.73 ns
Skew	0.55 ns	0.14 ns

TABLE 5. Dedicated Clock Performance

I/O Control and Local Hi-Drives

Each bank of I/O's has 2 input only pins that can be programmed to drive the RST, CLK and EN inputs of I/O's in that bank. These input only pins also double up as high drive inputs to a quadrant. Both as an I/O control or high drive, these buffers can be driven by the internal logic. The performance is indicated in Table 6.

TT, 25C, 2.5V	From Pad	From Array
I/O (slow)	1.00ns	1.14ns
I/O (fast)	0.63ns	0.78ns
Skew	0.37ns	0.36ns

TABLE 6. I/O Control Network/Local High-Drive

Programmable Logic Routing

Six types of routing resources are provided, as in the QuickRAM devices: short (sometimes called segmented) wires, dual wires, quad wires, express wires, distributed networks and defaults. Short wires span the length of 1 logic cell, always in the vertical direction. Dual wires run horizontally and span the length of 2 logic cells. Short and dual wires are predominantly used for local connections. They effectively traverse one or two logic cells utilize an interconnect element to continue to the next cell or to change direction.

Quad wires have passive link interconnect elements every fourth logic cell. As a result, these wires are typically used to implement intermediate length or medium fan-out nets.

Express lines run the length of the programmable logic uninterrupted. Each of these lines has a higher capacitance than a quad, dual or short wire, but less capacitance than shorter wires connected to run the length of the device. The resistance will also be lower because the express wires don't require the use of "pass" links. Express wires provide higher performance for long routes or high fan-out nets.

Distributed networks are described in the clock/control section. These wires span the programmable logic, and are driven by "column clock" buffers. Each dedicated clock network pin buffer is hard wired to a set of column clock buffers. Five global networks "global buffers" can be connected through special purpose routing called "HSCK lines" to either a dedicated pin buffer, or any vertical routing wire crossing it.

Global POR (Power-On Reset)

The Eclipse family of devices features a global power-on reset. This reset will be hardwired to all registers and will reset the registers upon power-up of the device. The circuitry used to support the global POR is similar to the power-up loading circuitry.

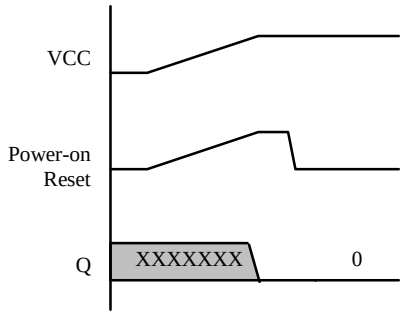

FIGURE 12. Power-On Reset

Separate Power and Logic-Cell Power

To decrease the logic cell area and to eliminate the need for disable transistors in the input stage of the logic cell, a separate power supply for the logic cells has been added to the family. This supply will be grounded during programming and for various test modes.

IEEE Standard 1149.1a.

The Eclipse family of devices supports IEEE standard 1149.1a. The following public instructions are supported: BYPASS, EXTEST, and SAMPLE/PRELOAD. Two additional modes RAMWT and RAMRD can be used to load the RAM. The pin functions will be the same as in the QuickRAM family.

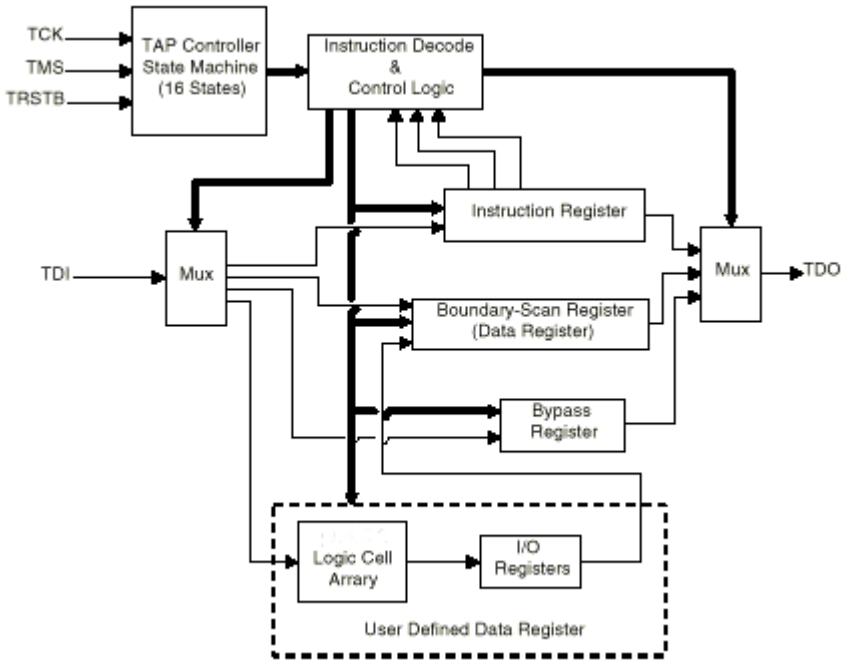

FIGURE 13. JTAG Block Diagram

JTAG BSDL Support

- BSDL-Boundary Scan Description Language
- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/ package combinations from QuickLogic
- Extensive industry support available and ATG (Automatic Test-vector Generation)

Security fuses.

There are two security links, one to disable reading from the array, the other to disable JTAG.

Flexibility fuse.

The flexibility link is actually implemented as two "default" links. If the tie-low link is programmed, RAM power up loading (from an external EPROM) is enabled, which might affect JTAG. If the tie-hi link is programmed, RAM power-up loading (from an external EPROM) will be disabled. JTAG will work normally, and can also be used to load the RAM.

Packaging

Eclipse product will be offered in the following packages. Military temperature range plastic packages will be added as follow on products to the commercial and industrial products.

Pin Count	208	280	484	516	672
Package Style	PQFP	FB BGA	BGA	BGA	BGA
Pitch		0.8mm	1.0mm	1.27mm	1.00mm
Ordering Code	PQ208	PT280	PS484	PB516	PS672
QL6250	X	X	X	X	
QL6325	X	X	X	X	
QL6500		X	X	X	X
QL6600		X	X	X	X

TABLE 7. Packaging Options