AMI SEMICONDUCTORS

SX042

WavePlex™ Wireless Products

Product Description

January, 1996

Spread Spectrum Receiver

General Description

The SX042 Spread Spectrum Receiver (SRX) is a highly programmable baseband CMOS integrated circuit that simplifies the design of direct sequence spread spectrum modems. Used to create very low cost receive-only remote wireless links, the SX042 is designed to serve as the collection host for a large group of SX041 transmitters or SX043 transceivers. Connected to a standard 8 bit microcontroller data bus, the SRX allows the user to manage internal SRX functions including the type and length of PN codes, data rates, chipping rates, slip rates, tracking rates, preamble, transmission protocols, and type of redundancy checks, as well as manage the external circuitry for signal reception.

Features

- Supports multiple SX041 transmitters or SX043 transceivers as system collector host link
- PN clock programmable up to 64M chips per second
- Up to 30dB processing gain; PN code lengths from 3 to 2047 chips
- Data and PN code streams available either separately or combined
- Supports BPSK, DBPSK, QPSK, DPQSK, and QAM modulation schemes
- Supports RF reception in any frequency band
- CRC-32 or CRC-16 decoding and error checking selectable
- Provides selectable code descrambling for spectral whitening
- Address/data bus timing allows interface to many popular 8 bit microcontrollers
- Supports packetized synchronous protocol (HDLC)
- 16 Byte receive data FIFOs reduces interrupt overhead
- Low power 3.3 volt (5 volt option available)
- Power down modes for minimum power usage

Figure 1: BLOCK DIAGRAM

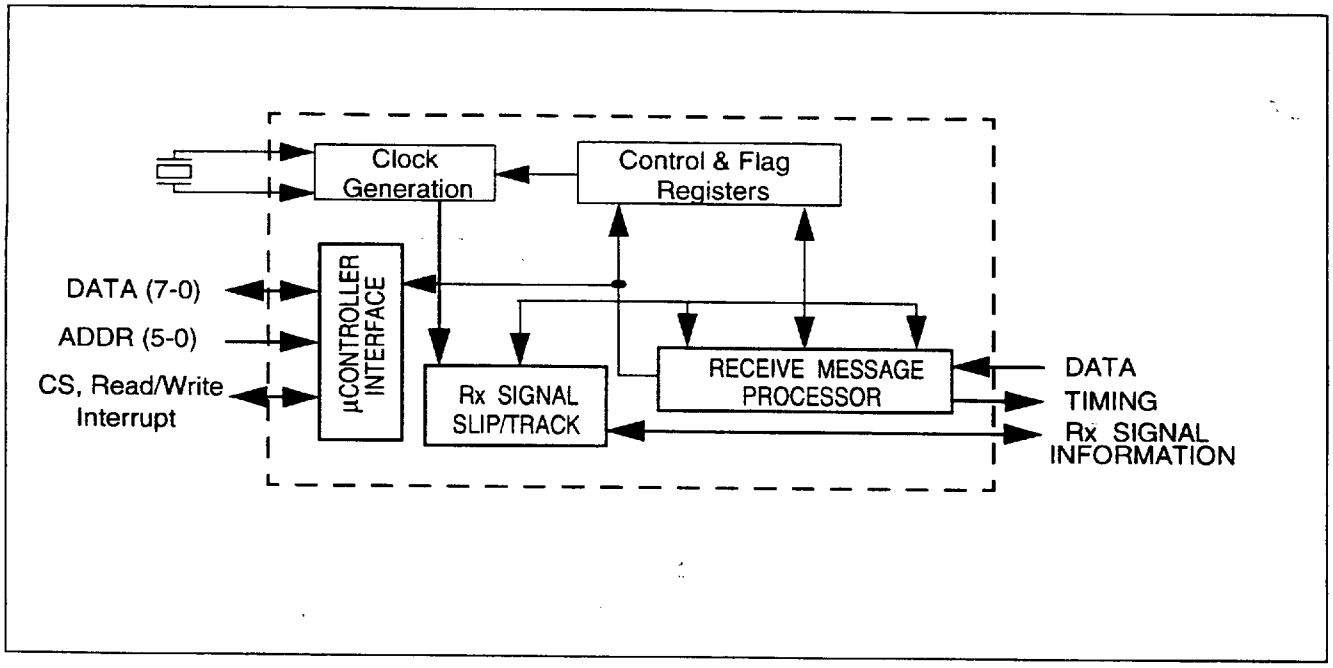
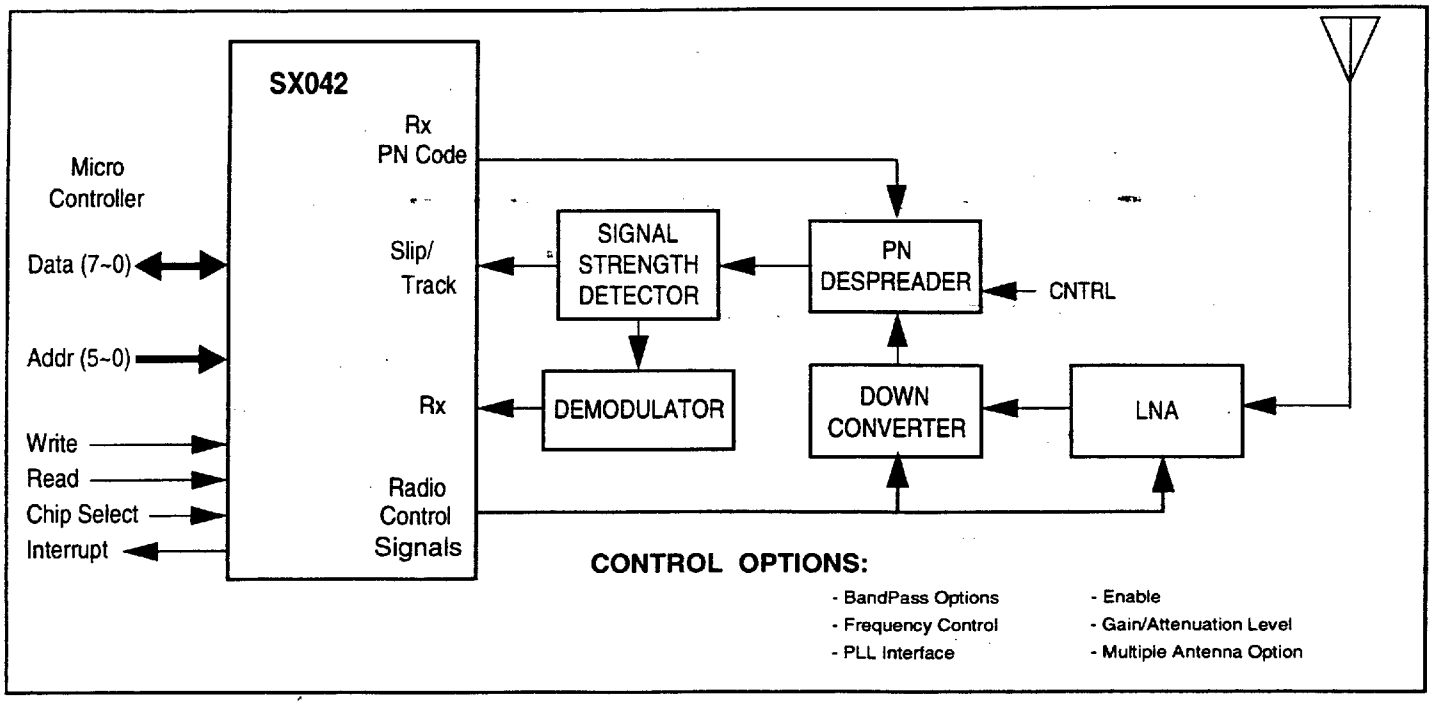


Figure 2. SYSTEM INTERFACE DIAGRAM



Functional Block Overview

The SRX Block Diagram in Figure 1 details the major functional blocks of the device. The microcontroller manages the Message Processors through various control and flag registers on the IC.

The microcontroller can also use registers in the SRX to control various radio functions. Figure 2 above represents the full radio implementation using the SRX.

MICROCONTROLLER INTERFACE: The device has a simple bus interface consisting of a bi-directional tri-state eight-bit data bus , a seven-bit address bus, read, write, and chip select inputs, and a general interrupt output. Target microcontrollers for this interface include the 68HC11, 68HC05, 6502, Z8, 8051, 16C5x, and 16C7x.

Power Manager: The microcontroller can put the IC into Standby Mode (a minimum power state) or select on or off.

CONTROL AND FLAG REGISTERS: The SRX has 52 registers available to the microcontroller. These registers allow programmable control over most characteristics of the receive channels (See Control Options in Figures 3), as well as off-chip control of the radio portion of the design. (See Control Options in Figure 2)

The SX042 includes a programmable 8 to 48 bit variable RF synthesizer interface. This interface supports any of the three popular serial data transfer styles in RF synthesizers: pulsed transfer, active enable transfer, or clock and data only. Or it can be set to a fourth 'user defined' mode. Extra control lines are also available for external circuits that require gain or attenuation level selection, pass band range selection, multiple antenna selection, etc..

In Packet Mode, the SRX can receive a repeating preamble code, HDLC protocols, destination address and control commands, CRC-16 or CRC-32 error detection coding, and end codes as selected by the control registers. A packet mode frame format is shown below:

START FLAG	ADDRESS	CONTROL	INFORMATION	CRC	END FLAG
8 bits	8 bits	8 bits	8 * N bits (any length)	16/32 bits	8 bits

Rx SIGNAL SLIP / TRACK: The SRX uses a 'shift and compare' approach to sync up with the receive signal. Using the 4MHz Tx_Clk for the Rx Phase Lock Loop (see Figure 4) during the capture or 'Slip' mode, the SRX generates the expected PN code (mixed with Preamble) and sends it to the external PN Despreader circuit (see Figure 2). If the generated PN code is synchronized perfectly with the PN code in the receive signal, then the Signal Strength

Detector will return a threshold energy level above a programmable threshold that indicates the match. Otherwise, the PN code will be delayed (shifted) by one half PN chip time period and the procedure is repeated. In this way the Rx PN code is slipped in time until it matches the EPOCH period of the received signal.

Once synchronization is achieved, the SRX transfers to a Tracking mode that uses the Receive Signal Strength input to drive the PLL, and dithers the PN Code delay in small steps around the synchronized signal to maintain solid tracking.

An internal "Track_on" signal alerts the Receive channel that a readable data stream is being presented to the IC.

RECEIVE MESSAGE PROCESSOR: The Receive channel (Figure 3) processes the receive message and delivers bytes of data to the microcontroller.

Word Detect: The Word Detect circuit reconstructs a single data stream from the incoming data streams processed by the external demodulator. BPSK, QPSK, DBPSK, DQPSK, or QAM results from the demodulator are presented on the RxD0 and RxD1 pins.

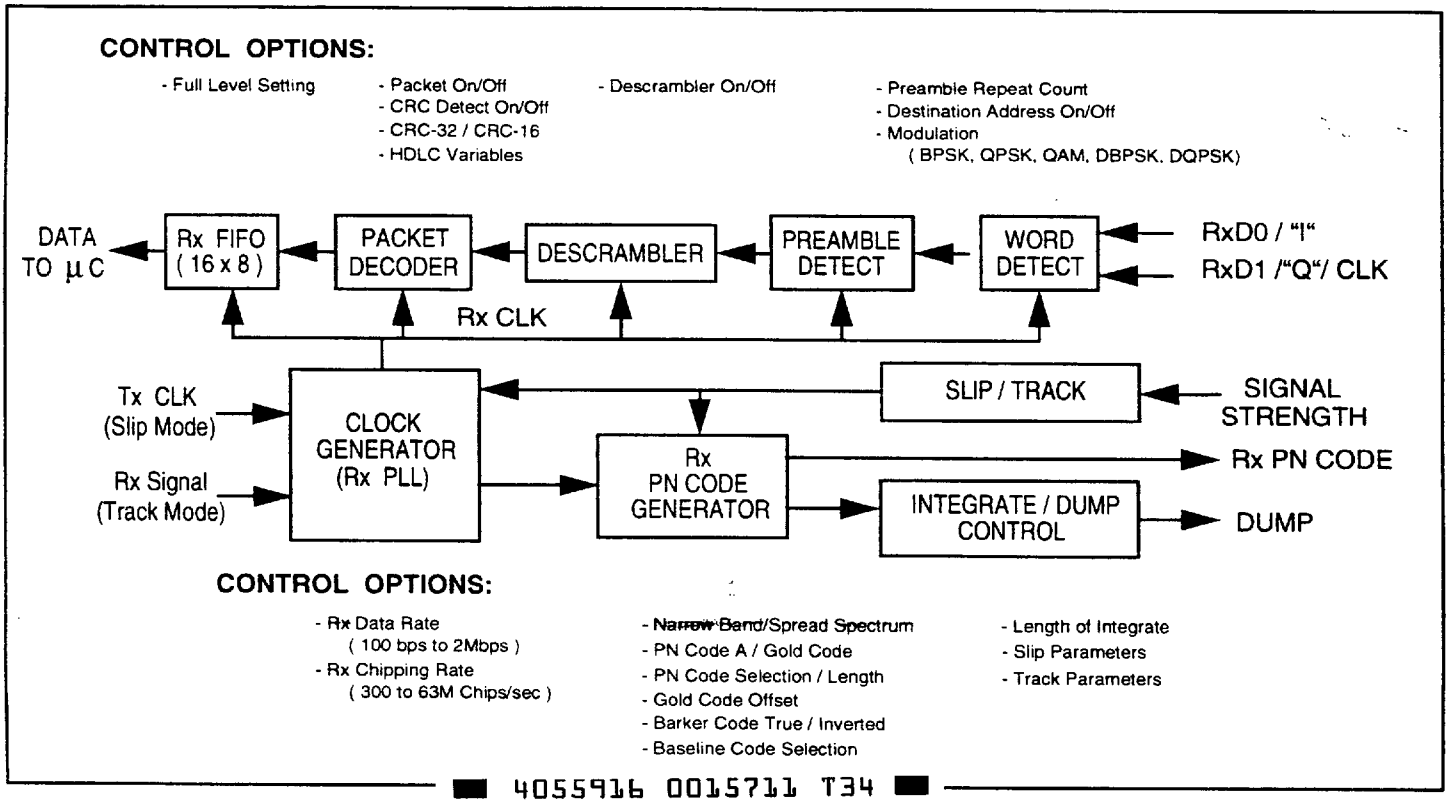
Preamble Detect: The Preamble Detect searches the incoming stream for the expected repeating preamble code followed by the end-of-preamble code. It then flags the Receive channel and microcontroller that a valid message is being received.

Descrambler: The Descrambler recovers the data that was scrambled in the Transmit channel. The descrambler can be programmed on or off.

Packet Decoder: The Packet Decoder verifies the destination address and then recaptures the raw data for the microcontroller. Programmed with the matched settings of preamble, protocol, and error detection of the Transmitter, the decoder alerts the controller of any receive errors, abort codes, lost tracking, and end-of-message information via interrupts and status registers.

Rx FIFO: Byte-wide data for the microcontroller is placed in a 16-byte deep Rx FIFO. The 'FIFO near-full' detect level can be programmed at bytes 0, 2, 4, or 8. The FIFO relays status to the microcontroller by means of the interrupt pin and control registers.

Figure 3. RECEIVE MESSAGE PROCESSOR



Data Rates

The SX042 can achieve data rates dependent on the PN code lengths used. These are shown below for each modulation scheme (nominal).

BPSK and DBPSK:

PN Code Length	Maximum Data Rate bits/sec	Maximum Symbol Rate symbols/sec
3, 7, 11*, 15, 31, 63	1 M	1 M
127	500 K	500 K
255	250 K	250 K
511	125 K	125 K
1023	62.5 K	62.5 K
2047	31 K	31 K

QPSK, DQPSK, QAM **:

PN Code Length	Maximum Data Rate bits/sec	Maximum Symbol Rate symbols/sec
3, 7, 11*, 15, 31, 63	2 M	1 M
127	1 M	500 K
255	500 K	250 K
511	250 K	125 K
1023	125 K	62.5 K
2047	62.5 K	31 K

* The 11 bit Barker code (1, -1, 1, 1, -1, 1, 1, 1, -1, -1, -1).

** QAM requires external ADCs and DACs. Data is transferred serially.

Pin Description

NAME:	TYPE:	FUNCTION:
AGND1	Analog ground	
GND1	ground	
VDD1	Vdd	
OSC1	input	Crystal Oscillator or external reference input. This input is divided by OSCDIV to generate the reference clock for the transmit PLL.
OSC2	padosc	Xtal Osc output.
PLL[0:3]	output	Off-Chip PLL programming; bit0, Enable1; bit1, Sclk; bit2, Enable0; bit3, Sdata.
GND2	ground	
EXT[0:7]	output	External Control port (lower bits), User Defined Functions for radio control.
VDD2	Vdd	
INT	output	Active high. Initiates an interrupt to the microprocessor.
RESET	input	Active low. Sets all registers to default values and forces the SX042 into its standby state.
CS	input	Active low. Selects the chip for reading and writing via the uP interface
RD	input	Active low. Initiates a read operation via the uP interface.
WR	input	Active low. Initiates a write operation via the uP interface.
GND3	ground	
DATA[0:7]	BiDirection	uP Interface data bus.
ADDR[0:6]	input	uP Interface address bus.
VDD3	Vdd	
GND4	ground	
DUMP	output	Integrate & Dump Control logic output.
PN2	output	Receive PN Generator output.
RCVRY	BiDirection	Clock recovery input for Narrow Band Mode. Track-On (active high) output for Spread Spectrum Mode. Indicates to external circuitry that the SX042 is locked and tracking the received PN code.
RXD1	Analog I/O	Receive data input 'Q' or QAM mode output clock to external shift register.

NAME:	TYPE:	FUNCTION:
RXD0	Analog In	Receive data input 'I'.
VREFD	Analog In	Reference voltage for integrate and dump comparators and switches.
AGND2	Analog ground	
VCO2	Analog Input	Receive VCO control voltage input
AVDD2	Analog VDD	
DACOUT1	Analog Output	Receive DAC output during TRACK operation. Note: DACOUT0 and DACOUT1 are provided in the event separate gain control is necessary for SLIP and TRACK operation.
DACOUT0	Analog Output	Receive PLL DAC output during SLIP operation.
RBIAS	Analog Input	Current reference for DACs and analog buffers. Nominal resistor value of 20K ohm to AGND3 for 3.3 volt VDD and 30K ohm for 5 volt VDD.
VREF	Analog Input	Reference voltage for ADC and DACs. Value is mid-scale between VDD and GND
AGND3	Analog ground	
RSSI1	Analog Input	Analog input to the ADC. Received Signal Strength Indicator from the RF receiver. Range is zero to VREF (full scale on internal ADC).
RSSI2	Analog Input	Analog input to the ADC. Received Signal Strength Indicator from the RF receiver. Range is zero to VREF (full scale on internal ADC). This input is not usable in "Slip" mode.
AVDD3	Analog VDD	
AVDD1	Analog VDD	
VCO1	Analog I/O	Master VCO voltage control input.