LCA400K
Compacted Array™ Series Product
Preliminary Datasheet

Overview: Optimized for 3 V Pad-Limited Designs

LCA400K Compacted Array Series ASICs (Application-Specific Integrated Circuits) provide the optimal, cost-effective solution for 3 V pad-limited designs. The LCA400K family is based on LSI Logic's 0.7-micron drawn gate length (0.55-micron effective channel length) HCMOS process technology and offers high gate densities equivalent to those of the LCA300K (0.6-micron) series. To minimize silicon usage for I/O-intensive designs, very fine pad pitches are offered, enabling over 700 pads. Advanced packaging options are featured to match the very fine pad pitch offering of the 400K silicon. The 400K array family is optimized for 3.3 V core operation for high performance and reduced power dissipation, and provides fast time-to-market solutions.

A comprehensive cell library containing a breadth of macrocells, macrofunctions, and value-added elements—such as PLL (Phase-Locked Loop) cells, NTL/GTL I/Os, and PCI (Peripheral Component Interconnect) Bus I/Os—allows the designer to maximize system performance. An extensive selection of 3.3 V and 5 V I/O buffers are compatible with existing bus standards. Figure 1 shows an example design with both 3.3 V and 5 V I/Os.

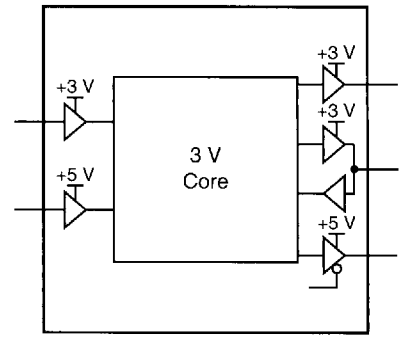

Figure 1. 400K Technology: 3 V Core, 5 V or 3 V I/O Capability

Robust design methodology is vital to ensure First-Time-Right™ system implementations in silicon. The 400K technology is supported by industry-leading EDA design tools and LSI Logic's C-MDE™ (Concurrent Modular Design Environment®) Design System to provide a variety of front-end platforms for logic design.

Features and Benefits

- Optimized for 3.3 V performance
- Low power dissipation
- High I/O-to-gate ratio with over 700 fine-pitch I/Os
- Split I/O power ring option for both 3 V and 5 V I/O implementation
- True 5 V and 3.3 V I/O interface capabilities
- Built-in multiplexer to simplify JTAG implementation
- Library characterized from 2.7 V to 3.6 V
- Special cells: GTL/NTL, PLLs, PCI Bus I/O
- Compilable ASIC memory:
  - up to 9 Kbits RAM (1- and 2-port)
  - over 72 Kbits ROM
- Fast prototype turnaround time
- Tight worst-case/best-case PVT delay window
- High reliability process
- Advanced packaging to match fine pad pitches

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Masterslice Sizes

The LCA400K product family includes fifteen array sizes as shown in Table 1 below. The masterslices range in density from 4,400 to 165,000 usable gate complexities with 104 to 724 I/Os. The pad counts for each masterslice correspond to the four different pad pitches for optimization of pad-limited designs.

Table 1. LCA400K Masterslices

Masterslice	Total Gates	Usable Gate		Pad Count (by Pad Pitch)			
		Nominal	Maximum	B	C	D	E
LCA400 013	12,810	4,500	6,200	144	132	108	104
LCA400 023	22,518	7,900	10,800	184	168	136	128
LCA400 030	30,268	10,600	14,500	208	192	160	148
LCA400 040	40,176	14,000	18,900	240	220	176	168
LCA400 053	52,824	18,500	24,300	272	248	200	188
LCA400 074	74,382	26,000	33,500	320	292	236	220
LCA400 097	96,768	33,900	42,600	360	328	264	248
LCA400 123	122,850	43,000	52,800	404	368	296	280
LCA400 153	152,764	53,500	64,200	448	408	328	308
LCA400 185	185,136	64,800	77,800	492	448	360	340
LCA400 236	235,800	82,500	96,700	552	504	400	380
LCA400 275	274,510	96,000	112,500	592	540	436	408
LCA400 317	317,376	111,100	130,100	636	580	464	440
LCA400 355	355,488	124,400	145,800	672	612	492	464
LCA400 411	411,048	143,900	164,700	724	660	528	500

The actual usable gate count of a masterslice will vary depending upon design methodology and content. Sixteen pads per die are dedicated to power and ground. Contact your LSI Logic applications engineer for detailed power and ground guidelines.

The package types corresponding to the four pad pitches are referenced in Table 2. Refer to the "Package Information" section on page 8 for details on LSI Logic's breadth of advanced packaging options.

Table 2. Package Pad Pitch Compatibility

Package	Pad Pitch (mil)			
	B	C	D	E
PQFP/TQFP			x	x
PQFPi[1]	x	x		
PBGA			x	x
MQUAD			x	x
PGA			x	x
TQHS	x	x	x	x
TBGA	x	x	x	x
E-PBGA			x	x
COT	x	x	x	x

1. PQFP with package interposer.

Low Power Dissipation

Component power dissipation management is an essential element in ASIC designs. A substantial amount of power can be saved with the 3 V core operation of the 400K technology. For example, a two-input NAND gate in 400K dissipates 2.71 µW/MHz/gate (fanout = 2, 0.5-mm metal). The power savings obtained with the 400K technology result in longer battery life in portable devices and less heat dissipation and improved reliability in all applications.

High Performance I/Os

Designers may choose from a large selection of LSI Logic I/Os that all interface with existing bus standards. Available I/O types include 5 V CMOS, 5 V TTL, or 3.3 V with a single, unified LVTTL/LVCMOS threshold voltage for low-power applications. Output drive strengths for both sets range from 2 to 24 mA and therefore may be selected to fit specific design requirements. For each output, slew rate control may be selected from a choice of buffers with different edge-rate characteristics. The slew rate controlled buffers improve switching performance and minimize ground bounce in non-critical paths. Because the I/O power ring can be split automatically, I/O voltage levels of both 3 V and 5 V can be supported by an individual design. This capability enables the ASIC design to interface to devices with different power supplies and provides added flexibility in minimizing system power dissipation.

Value-Added Cells

The 400K product family contains value-added cells—PCI bus I/O buffers, NTL I/Os, and PLL cells—to help maximize system performance.

PCI Bus I/O Buffers

The PCI bus is rapidly becoming an increasingly popular bus interface to add-in cards. To support this growing trend, LSI Logic offers universal (3.3 V/5 V) and non-universal (3 V) PCI bus I/O buffers in the 400K technology. The PCI buffers are fully compliant with the industry standard and use only one I/O slot and one pad cell for implementation in ASIC designs. The use of the PCI bus buffers reduces the time and effort needed to design an ASIC that interfaces to the PCI bus.

NTL I/Os

The potential for noise from large groups of simultaneously switching outputs can become a serious issue for high-speed ASIC designs. Noise is a particular concern for pad-limited designs with extensive I/O requirements. To address this problem, LSI Logic offers NTL I/Os to reduce power dissipation and noise. The NTL I/Os allow a small output driver voltage swing from 0.8 V to a maximum of 1.0 V. The NTL interfaces are capable of supporting up to 100 MHz bussed signals with 48 mA drive capabilities. The high-speed, low-noise attributes make NTL buffers ideally suited for both backplane and point-to-point interfaces in EDP applications.

PLL Cells

Individual clock delays may differ from chip to chip because of process variations and different loadings—which may cause potential clock skew problems between each chip and the system clock. To minimize clock skew and achieve synchronization, LSI Logic offers PLL cells for use with 400K designs of up to 100 MHz clock frequency. These analog PLLs are capable of limiting chip-to-chip clock skew to less than 150 ps.

PVT Factors

The 400K delay derating factors are one of the tightest in the industry with best case/worst case of 0.68/1.61 for commercial conditions, as shown in Table 3 below. The tight derating factors allow more accurate system designing and increase system performance.

Table 3. LCA400K Derating Factors

Derating Factor	Commercial		Military	
	Best Case	Worst Case	Best Case	Worst Case
Process (K_P)	0.76	1.26	0.76	1.26
Voltage (K_V)	0.95	1.05	0.91	1.12
Temperature (K_T)[1]	0.94	1.21	0.81	1.29
TOTAL	0.68	1.61	0.56	1.82

1. The commercial junction temperature range is 0 to +115° C, and the military junction temperature range is -55 to +150° C.

Test Methodology

As the leading supplier of test solutions in the industry, LSI Logic has the tools to provide cost-effective, fine pad-pitch testing. The 400K technology offers fine pad spacing to minimize die size for I/O-limited designs. The spacing of the finest pitch is so close that probing of all pads is prohibited with the current probe technology. However, such designs may be tested by probing a few pads and exercising an internal scan chain to test the device fully without probing every bond pad. For easy test synthesis capability, automatic insertion of boundary scan into the system logic is possible with LSI Logic's JTAG Builder. The built-in multiplexer in the 400K I/Os further facilitates the implementation of JTAG testing in designs. Additional test methodologies for the 400K technology include:

- LSI Logic's Test Builder for insertion of internal scan and ATPG, which can achieve over 99% fault coverage
- RAM Built-In Self Test (BIST) insertion for self-testing of RAM blocks

Fault simulation for ASICs is also supported using Zycad's XP hardware accelerators.

Development Methodology

The LSI Logic design methodology depicted in Figure 2 ensures Right-First-Time™ silicon. The methodology enables a wide variety of architectural solutions starting with VHDL/HDL inputs into synthesis or direct netlist entry. Comprehensive high-performance simulation closely tied to the silicon process provides accurate results. LSI Logic's C-MDE design system and popular EDA tools from companies such as Synopsys, Cadence, Viewlogic, and Mentor Graphics provide powerful options for design environments. Timing-driven layout linked to logic synthesis allows a designer to reach timing closure quickly, resulting in production-ready layout. Fast prototype turns and pre-production and production capabilities ensure fast time-to-market.

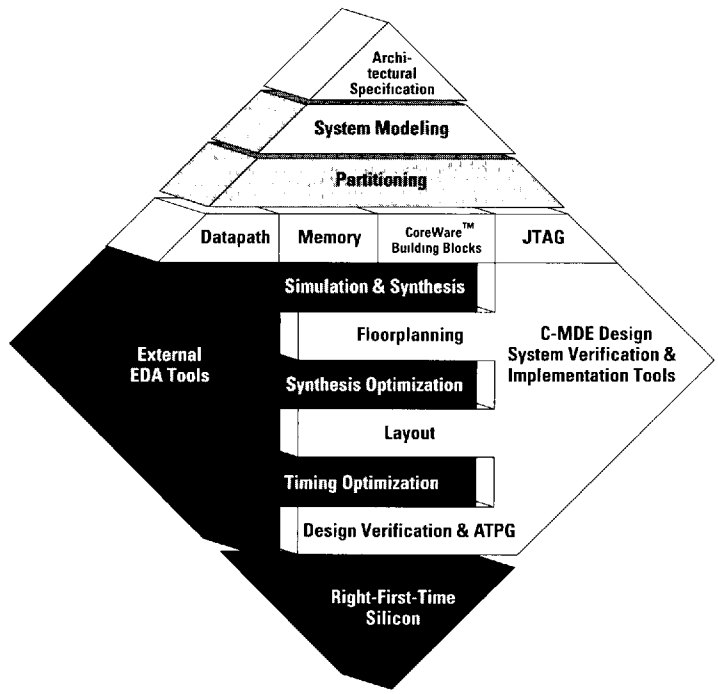


Figure 2. LSI Logic's Design Methodology

Process/ Manufacturing

The 400K Compacted Array family is manufactured using a reliable 0.7-micron drawn (0.55-micron effective) Channel-Free® architecture. This technology is manufactured at LSI Logic's high-volume production facility located in Tsukuba, Japan, using existing manufacturing equipment that has produced over one million 100K ASIC units.

Specifications

Table 4 provides the 400K DC characteristics. The military junction temperature range is -55 to +150° C, ±10% power supply (ceramic packages only). The industrial junction temperature range is -40 to +125° C, ±5% power supply. The commercial junction temperature range is 0 to +115° C, ±5% power supply.

Table 4. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIL	Voltage input LOW TTL inputs CMOS levels				 0.8 0.2 VDD	V
VIH	Voltage input HIGH TTL inputs TTL Schmitt trigger inputs CMOS levels	 (Com/Ind/Mil temp range) (Ind/Mil temp range)	 2.0 2.25 0.7 VDD			 V V V
VT	Switching threshold	TTL CMOS		1.5 2.5		V V
VT+	Schmitt trigger, positive-going threshold	CMOS TTL		1.77 2.0	2.0 2.25	V V
VT-	Schmitt trigger, negative-going threshold	CMOS (5 V) LVCMOS (3.3 V) TTL	1.0 0.8 0.8	1.5 1.04 1.04		V V V
	Hysteresis, Schmitt trigger	CMOS (VIL to VIH) TTL (VIL to VIH)	1.0 0.4	1.5 0.8		V
IIN	Input current, CMOS, TTL Inputs Inputs with pulldown resistors (5 V) Inputs with pulldown resistors (3.3 V) TTL inputs and inputs with pullup resistors (5 V) TTL inputs and inputs with pullup resistors (3.3 V)	VIN = VDD or VSS VIN = VDD VIN = VDD VIN = VSS VIN = VSS	-10 35 35 -35 -35	±1 115 -115 -115 -115	10 222 138 -214 -131	µA µA µA µA µA
VOH	Voltage output HIGH Type B1 Type B2 Type B4 Type B6 Type B8 Type B12[1]	Commercial and Military IOH = -1 mA IOH = -2 mA IOH = -4 mA IOH = -6 mA IOH = -8 mA IOH = -12 mA	 2.4 2.4 2.4 2.4 2.4 2.4			 V V V V V V
VOL	Voltage output LOW Type B1 Type B2 Type B4 Type B6 Type B8 Type B12[1]	Commercial and Military IOL =1 mA IOL = 2 mA IOL = 4 mA IOL = 6 mA IOL = 8 mA IOL =12 mA		 0.2 0.2 0.2 0.2 0.2 0.2	 0.4 0.4 0.4 0.4 0.4 0.4	 V V V V V V
IOZ	3-State output leakage current	VOH = VSS or VDD	-10	±1	10	µA
IOS	Output short circuit current[2]	VDD = 5.25 V, VO = VDD VDD = 5.25 V, VO = VSS VDD = 3.45 V, VO = VDD VDD = 3.45 V, VO = VSS	37 -117 50 -99	90 -75 110 -60	140 -40 182 -31	mA mA mA mA
IDD	Quiescent supply current	VIN = VDD or VSS	User-Design Dependent			
CIN	Input capacitance	Any Input and Bidirectional Buffers	2.5			pF
COUT	Output capacitance	Any Output Buffer[3]	2.0			pF

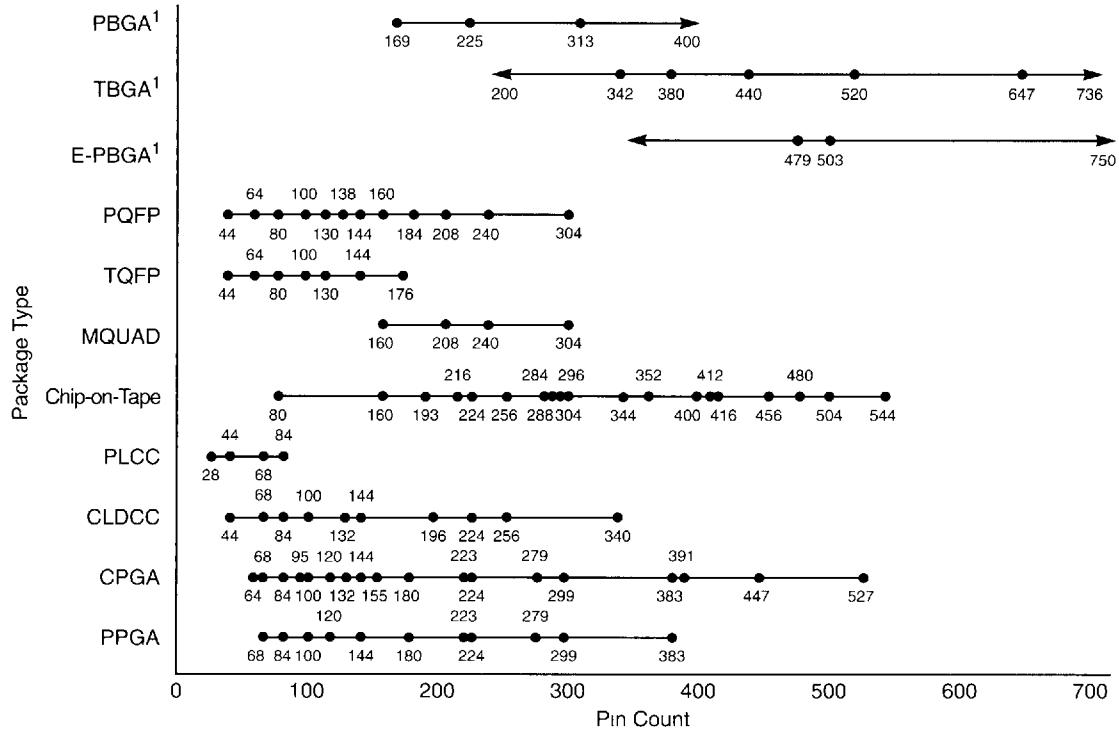
1. Requires two output pads.
2. Type B4 output. Output short circuit current for other outputs will scale.
3. Output using single buffer structure (excluding package).

Package Information

To translate the cost-effective performance of LSI Logic's 400K silicon into system solutions, LSI Logic's ASIC packaging has been specifically matched to 400K capabilities. New packages have been developed and qualified in conjunction with 400K. By combining these new packages with existing packages, LSI Logic's 400K family offers a full range of packaging options.

For high-volume manufacturing of performance devices, LSI Logic has introduced TQHS (Thin Quad Heat Spreader) and TBGA (Tape Ball Grid Array). TQHS is the industry's highest electrical performance QFP and is also the first thin QFP capable of pin counts up to 304 leads. For higher pin counts, Tape Ball Grid Array (TBGA) allows 250 to 750 leads.

In addition, LSI Logic's Advanced Plastic Pin Grid Array (PPGA), Ball Grid Array (BGA), and Chip-on-Tape (COT) packaging technologies are available for high-pin-count, high-frequency applications. Mainstream packages—such as the PQFP, TQFP, MQUAD, and PLCC—benefit from LSI Logic's experience in serving high-volume manufacturing environments. See Figure 3 for a chart of package pin counts.



1. New package families—pin count extensions underway.

Figure 3. Package Pin Counts

Across all packaging technologies LSI Logic provides thermal, electrical, and mechanical modeling of the package and silicon combination, leading to First-Time-Right solutions and a depth of packaging knowledge that allows a designer leverage in making system design trade-offs.