Supertex inc.

HV01

T-52-13-05

16-Channel Matrix TFEL Panel Display Column Driver

Ordering Information

Device	Package Options					
	40-Pin Ceramic DIP	36-Pin Leadless Chip Carrier	36-Pin Leaded Chip Carrier Flat Leads	36-Pin Leaded Chip Carrier Std. Bent Leads	36-Pin Leaded Chip Carrier Reverse Bent Leads	Die
HV01	HV01C	HV01LC	HV01CF	HV01CS	HV01CR	HV01X

Features

- ☐ Up to 60V modulation supply voltage
- ☐ Drives up to 1000 lines
- ☐ Capability of 16 levels of gray shading
- ☐ 15µS per conversion and output cycle
- ☐ Integrated high voltage DMOS and CMOS technology
- ☐ Available in 40-pin DIP, 36 LCC pkg., or in die form

General Description

The HV01 is a 16 channel column driver IC designed for general purpose electroluminescent display use. The chip contains a D to A converter and a push-pull output driver for each channel. Input data is clocked in on the Hi to Low transition of the Clock input and stored in shift registers. This data feeds into the respective 4-bit polynomial counter, which serves as a time measuring device. The output of this counter controls a charging device allowing a ramp signal to set the analog driver to the desired voltage level corresponding to one of the 16 possible gray shades.

Absolute Maximum Ratings

Low Voltage Supply V_{DD}	-0.5V to 14V
High Voltage Supply V_{PP}	-0.5V to 65V
Ramp Voltage V_R	-0.5 to V_{PP} +0.3V
Logic Input Voltage	-0.5V to V_{DD} +0.5V
Storage Temperature	-65°C to 150°C
Power Dissipation[1]	1.6 Watt

Note 1: For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

T-52-13-05

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage Logic Inputs	V_{DD} - 1			V	
V_{IL}	Input Low Voltage Logic Inputs			1	V	
I_{DD}	V_{DD} Supply Current		4	13	mA	V_{DD} = 13.2V, f_{SC} = 3mHz
I_{DDS}	STDBY V_{DD} Supply Current			8	mA	V_{DD} = 13.2V
I_{PP}	V_{PP} (Driver) Supply Current		12		mA	V_{PP} = 60V, t_{CR} = 50µS
I_{PPS}	STDBY V_{PP} Supply Current			5.5	mA	V_{PP} = 60V
I_{IL}, I_{IH}	Input Leakage Current		±1	±50	µA	V_{IN} = 0V or V_{DD}
I_{OH}	Logic Output Source Current	-50			µA	V_{OH} = V_{DD} - 1.0V
I_{OL}	Logic Output Sink Current	50			µA	V_{OL} = 1.0V
I_{AOH}	HV Analog Output Source Current	-8	-40		mA	V_{PP} = 60V, V_R = 60V V_{AOH} = 50V
I_{AOL}	HV Analog Output Sink Current	8	40		mA	V_{PP} = 60V, V_R = 60V V_{AOL} = 10V

AC Characteristics (V_{DD} = 12V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{SL}	Set up time before load (Shift Clock)	200			ns	
t_{HL}	Hold time after load (Shift Clock)	100			ns	
t_L	Load/Count Pulse Width	100			ns	
t_{LS}	Load set up before Count Clock	20			ns	
t_{LC}	Load hold after Count Clock	20			ns	
t_{DR}	Count to Ramp Delay			100	ns	
t_{CR}	Cycle Time of Ramp Signal	8			µs	
t_{RR}	Rise Time of Ramp Signal	3			µs	
f_{SC}	Operating Frequency (Shift Clock)			6	MHz	V_{DD} = 10.8V
t_{DS}	Data set up to shift clock ↓	35			ns	
t_{DH}	Data hold from shift clock ↓	20			ns	
C_H	Internal holding capacitance per part		50		pF	
t_{RF}	Ramp voltage fall time	5			µs	

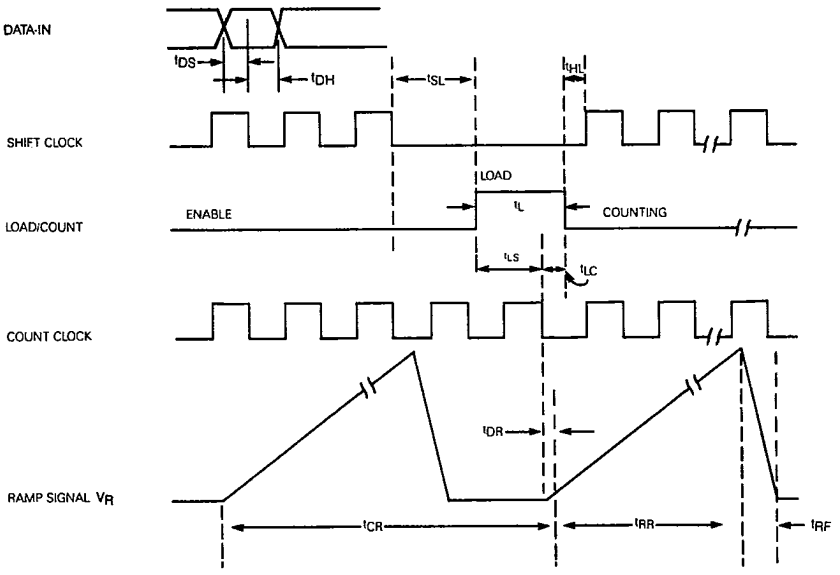
Recommended Operating Conditions*

Parameter	Value
Low Voltage Supply V_{DD}	12V ± 10%
High Voltage Supply V_{PP}	40V to 60V
Logic Input Voltage	0 to V_{DD}
Operating Temperature (T_A)	-40°C to 85°C

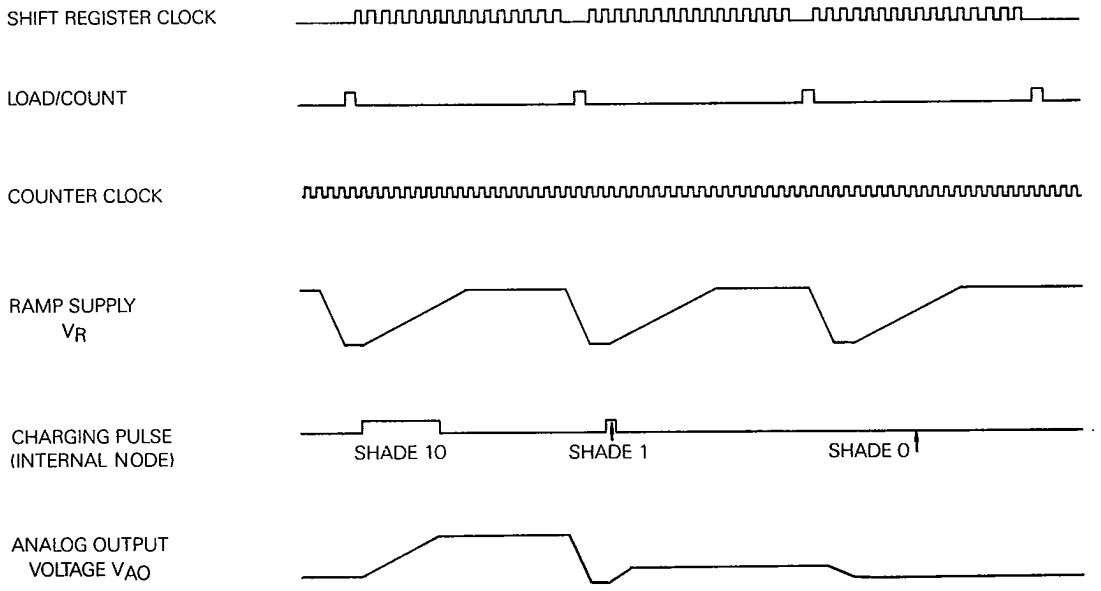
* Recommended Power Up Sequence: V_{DD}, V_{PP}, Logic, V_R

T-52-13-05

Switching Waveforms



Timing Diagram

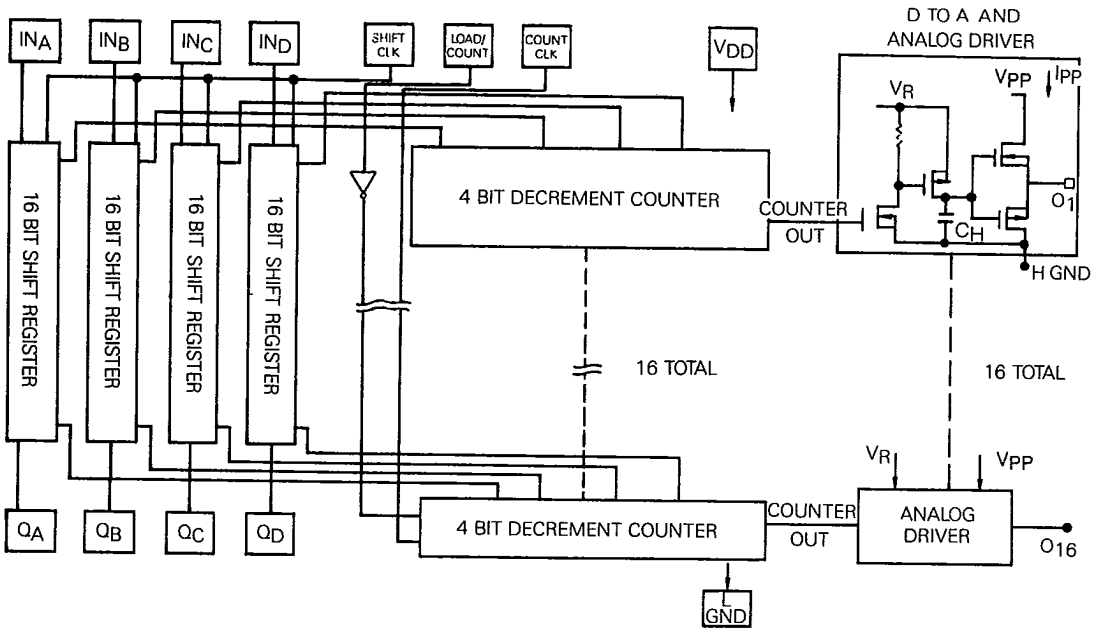


11

Functional Block Diagram

T-52-13-05

HV01



Function Table

Function	Control Inputs				Shift Registers	Counters	Outputs	
	Shift Clock	Counter Clock	Load/ Count	V_R			Serial	Parallel
Load Shift Register	↓	X	L	X	Normal Shift Op	X	Delayed Data-In	X
Load Counter	No↓	↓	H	X	No Change	Load Data From S/R to Counter	No Change	Low
Counting	X	↓	L	Initiates Ramp	X	Translates Data To Time	X	D/A Conversion
Voltage Conversion	X	Pulsing	L	Volt. Ramping Up	X	Counting	X	Follows Ramp

L = Low level, H = High level, X = Irrelevant, ↓ = Hi to Low Transition

Operation of the Column Driver

Operation of the Column Driver can be understood by looking at the logic and timing diagrams. The shift registers store four bits of data for each column to be driven. The four bits are used to program a counter for sixteen possible values (0-15) which generate the sixteen gray shades. Since the shift registers have serial outputs, the chips can be connected in sequence. To load the shift registers we need n times sixteen pulses (where n = the # of chips connected serially). After the last shift clock, we need a short set up time (t_{SL}) before we can load the data of the register into the counter. The loading is performed by the Hi level of a Load/ Count Enable Pulse (t_L). At the end of this pulse the load count enable goes low and the transfer gates which connect the shift registers to the counters turn off and the counter inputs are enabled. The counting will start at the negative going edge of the first count clock pulse (t_{LC}). Concurrently, a positive going ramp signal is initiated whose rise time is equal to the length of 16 count clocks. The output of the counter is, in effect, a pulse width with a termination time controlled by the shift register digital value. The analog storage stage follows the value on the voltage ramp input for the duration of that pulse, and then holds that voltage value. As the timing diagram indicates, each pulse width will specify a different voltage level. In effect a digital to analog converter stage was implemented. If at any time the difference in voltage stored in the analog storage stage and the output voltage differs by more than one transistor threshold (typically 2 to 3 volts), one of the two output transistors will turn on to set the correct voltage on the column.

Programming the Column Driver

The Supertex HV01 Column Driver was built to generate 16 different shades on a thin film electroluminescent panel. These 16 shades are achieved by having 1 of 16 possible voltage levels on the analog outputs.

Depending on the 4 digital inputs fed into the 4 shift registers, data is loaded into each of the 16 counters. These counters will interpret the data and produce a pulse whose width is determined by the data. The output of each drive line is basically a D/A conversion of the timing signal generated by the polynomial counter.

The shade voltages are specified by the digital input according to the table shown. In the table we designate the various shade voltages by numbers. Shade No. 16 is the brightest, while Shade

Gray Shade Decoding Scheme

Brightest Shade No.	INA	INB	INC	IND	
16	1	0	0	1	Brightest
15	1	1	0	1	
14	1	1	1	1	
13	1	1	1	0	
12	0	1	1	1	
11	1	0	1	0	
10	0	1	0	1	
9	1	0	1	1	
8	1	1	0	0	
7	0	1	1	0	
6	0	0	1	1	
5	1	0	0	0	
4	0	1	0	0	
3	0	0	1	0	
2	0	0	0	1	
1	0	0	0	0	Dimmest

Pin Configurations

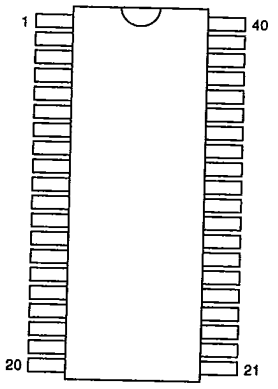
40-Pin DIP

Pin	Function	Pin	Function
1	L GND	21	HVout 8
2	Load Count	22	HVout 7
3	N/C	23	HVout 6
4	O_A	24	HVout 5
5	O_B	25	HVout 4
6	O_C	26	HVout 3
7	O_D	27	HVout 2
8	V_R	28	HVout 1
9	V_{PP}	29	H GND
10	N/C	30	N/C
11	N/C	31	N/C
12	H GND	32	V_{PP}
13	HVout 16	33	V_R
14	HVout 15	34	IN_D
15	HVout 14	35	IN_C
16	HVout 13	36	IN_B
17	HVout 12	37	IN_A
18	HVout 11	38	Shift CLK
19	HVout 10	39	Count CLK
20	HVout 9	40	V_{DD}

36-Pin LCC

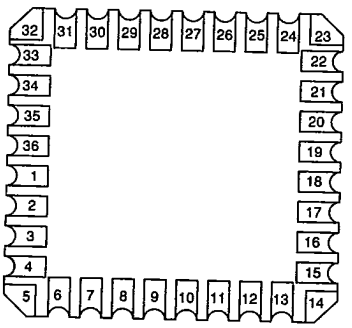
Pin	Function	Pin	Function
1	L GND	19	HVout 8
2	Load Count	20	HVout 7
3	N/C	21	HVout 6
4	O_A	22	HVout 5
5	O_B	23	HVout 4
6	O_C	24	HVout 3
7	O_D	25	HVout 2
8	V_R	26	HVout 1
9	V_{PP}	27	H GND
10	H GND	28	V_{PP}
11	HVout 16	29	V_R
12	HVout 15	30	IN_D
13	HVout 14	31	IN_C
14	HVout 13	32	IN_B
15	HVout 12	33	IN_A
16	HVout 11	34	Shift CLK
17	HVout 10	35	Count CLK
18	HVout 9	36	V_{DD}

Package Outlines



top view

40-pin DIP



top view

36-pin LCC