FREQUENCY DEVICES™

810 SERIES DIGITALLY PROGRAMMABLE QUADRATURE SINEWAVE OSCILLATORS

DS-00810-00

FEATURES

High Purity Quadrature Sinewave Outputs featuring:

- **Digitally Programmable Oscillation Frequencies via CMOS Interface Logic**
- **Internally Latched Control Lines to Store Frequency Selection Data**
- **High Purity Outputs**
  SIN: 0.2% T.H.D.
  COS: 0.08% T.H.D.
- **Plug-in Ready-to-Use Fully Finished Oscillator Component**

APPLICATIONS

Many System Functions Requiring Digitally Progammable Quadrature Sinewave Outputs including:

- **Programmable Automatic Test Equipment (A.T.E.) Systems**
- **Production Test Systems**
- **Industrial Process Control**
- **Distortion Testing**

GENERAL DESCRIPTION

The **810 Series** are digitally-programmable quadrature output sinewave oscillators that are tunable over over a 256:1 frequency range. Delivering two simultaneous high-purity sinusoidal outputs that differ in phase by 90°, these units contain 8-bit CMOS clocked "D" latches which can be digitally configured to operate in any of three modes:

a) Transfer frequency control input data into the latches on the STROBE (or CLOCK) rising edge.

b) As above, but on the STROBE falling edge.

c) Follow the tuning input data, in a non-latching transparent mode.

The present three models offer users the following selection of tuning frequency bands:

- –2 Models: 1.0Hz to 256Hz
- –3 Models: 10Hz to 2560Hz
- –4 Models: 100Hz to 25.6kHz

All **810 Series** models are fully finished quadrature oscillators which require no external components or adjustments, and operate from non-critical ±12 to ±18V power supplies. High purity outputs with harmonic distortion low as 0.2% (SIN) and 0.08% (COS) make these compact (2.0"W x 4.0"L footprint, by 0.4"H or 0.6"H) encapsulated plug-in modules versatile and easy to use.

CONDENSED FREQUENCY SELECTION TABLE

MSB	---	---	---	---	---	---	LSB	<– Bit Weight
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	**Oscillation Frequency (fo)**
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	0	0	0	0	fmax/256
0	0	0	0	0	0	1	1	fmax/64
0	0	0	0	1	1	1	1	fmax/16
0	1	1	1	1	1	1	1	fmax/2
1	1	1	1	1	1	1	1	fmax

Five of the possible 256 frequency selection codes.

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810 SERIES
ANALOG SPECIFICATIONS

ANALOG SPECIFICATIONS (Typical @ 25°C & ±15Vdc unless otherwise noted)	
OSCILLATION FREQUENCY	
Tolerance	±3%
Stability vs. Supply	0.01%/%
Stability vs. Output	0.1%/%
Tuning Characteristics	
Frequency Range	0.1Hz ≥ fo ≥25.6kHz
Programming Range	256:1
Step Size (Resolution)	Fmax/256
Stability vs Temperature	0.01%/°C
OUTPUT AMPLITUDE	
Individual Output	
Initial Preset Level	10Vp-p ±0.5%
Stability	
vs. Temperature	0.2dB/°C
vs. Supply	0.02dB/%
Rated Current @ 20Vp-p	5mA
Output Resistance	1 Ohm
Amplitude Ratio	
Initial Tolerance	0.3dB
Stability	
vs. Temperature	0.01%/°C
vs. Supply	0.01%/%
Quadrature Phase Error	+0.0°, −1.0°
OUTPUT DISTORTION	
Harmonic	
SIN Output Output	0.2%
COS Output Output	0.08%
Non-Harmonic	200μV
POWER SUPPLY (±Vs)	
Operating Voltage	±12 to ±18Vdc
Nominal Range	±15Vdc
Quiescent Current	20mA
TEMPERATURE	
Operating	0°C to +70°C
Storage	−25°C to +85°C

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810 SERIES DC OFFSET, GROUNDING AND CONTROL CHARACTERISTICS

DC OFFSET vs. TEMPERATURE

The DC offset voltage of **810 Series** oscillators originates at two internal sources that cause it to vary with temperature and selected frequency. Slight mismatches between operational amplifier (op amp) semiconductor junctions create the first source of DC offset. Switching element leakage currents flowing through switching-selected tuning resistors predominate as the second source of DC offset. Though small at 25°C, the switch leakage currents increase exponentially with absolute temperature to become significantly large at higher temperatures. This becomes a problem when the oscillator is tuned to low frequencies, when require high-value tuning resistors.

Figure A illustrates the worst case temperature behavior of the offset voltage; this improves with higher frequency codes. The maximum DC offset voltage will generally occur at the highest temperature and the lowest oscillation frequency (all "0" input code). This recommends selection of the model with the LOWEST CORNER OSCILLATION FREQUENCY (fo) possible.

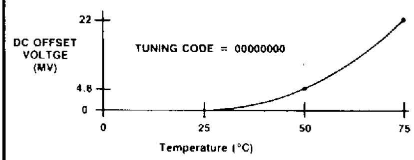

Figure A. The DC offset voltage drift varies with tuning code. Turning on the LSB would halve the maximum DC offset. See discussion.

USER NOTES

Grounding: To achieve specified precision, all analog and digital grounds are connected internal to the oscillator. Should this cause a problem, all digital inputs (C, P, and D_0 - D_7) can be optically isolated.

Settling Time: When tuned to a different frequency, an oscillator requires sufficient transient settling time corresponding to several cycles of the new frequency. PLEASE NOTE: DO NOT use these devices in frequency scanning applications without considering settling time.

DATA CONTROL CHARACTERISTICS

Data Control Lines		
Functions	Latch Strobe (C)	
	Transition Polarity (P)	
Data Control Modes		
Mode 1	P = 0; C = 0	frequency follows input codes
	P = 0; C = 0 – >1	frequency latched on rising edge
Mode 2	P = 1; C = 1	frequency follows input codes
	P = 1; C = 1 – >0	frequency latched on falling edge
INPUT DATA LEVELS (CMOS Logic)		
Input Voltage (Vs = 15V)	**Min.**	**Max. Acceptable**
Low Level In	0 Volts	4 Volts
High Level In	11 Volts	15 Volts
Input Current	**Typ.**	**Max.**
High Level In	-10^{-5} μA	-1μA
Low Level In	$+10^{-5}$μA	$+1$μA
Input Capacitance	5pF	7.5pf
Latch Response		
Data Set Up Time[1]	25 ns	—
Data Hold Time[2]	50 ns	—
Strobe		
Min Pulse Width	80 ns	—

Notes: 1. The time data must be present before occurence of strobe edge.
2. The time data must be present after occurence of strobe edge.

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DIGITAL TUNING CHARACTERISTICS

The digital tuning interface circuits are two 4042 quad CMOS latches which accept the following CMOS-compatible inputs: eight tuning bits (D_0 - D_7), a latch strobe bit (C), and a transition polarity bit (P). Oscillator tuning follows the digital equation given below:

$fo = (fmax/256)\,[1 + D_7*2^7 + D_6*2^6 + D_5*2^5 + D_4*2^4 + D_3*2^3 + D_2*2^2 + D_1*2^1 + D_0*2^0]$

where $D_0 - D_7$ = Logic "0" or "1", and
fmax = maximum tunable frequency
fo = frequency of oscillation
Minimum tunable oscillation = fmax/256 (D_0 –> D_7 = 0)
Minimum frequency step (Resolution) = fmax/256

INPUT DATA FORMAT

Frequency Select Bits

Positive Logic	Logic "1" = +Vs	
	Logic "0" = Gnd	Logic threshold typ. = 0.45Vs
Bit Weighting (Binary-Coded)	D_0 = least significant bit (LSB)	
	D_7 = most significant bit (MSB)	
Frequency Range	256:1, Binary Weighted	

DIGITAL FREQUENCY SELECTION

Nine of the 256 possible frequency selection codes

MSB	---	---	---	---	---	---	LSB	<– **Bit Weight**
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D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	0	0	0	0	fmax/256
0	0	0	0	0	0	0	1	fmax/128
0	0	0	0	0	0	1	1	fmax/64
0	0	0	0	0	1	1	1	fmax/32
0	0	0	0	1	1	1	1	fmax/16
0	0	0	1	1	1	1	1	fmax/8
0	0	1	1	1	1	1	1	fmax/4
0	1	1	1	1	1	1	1	fmax/2
1	1	1	1	1	1	1	1	fmax

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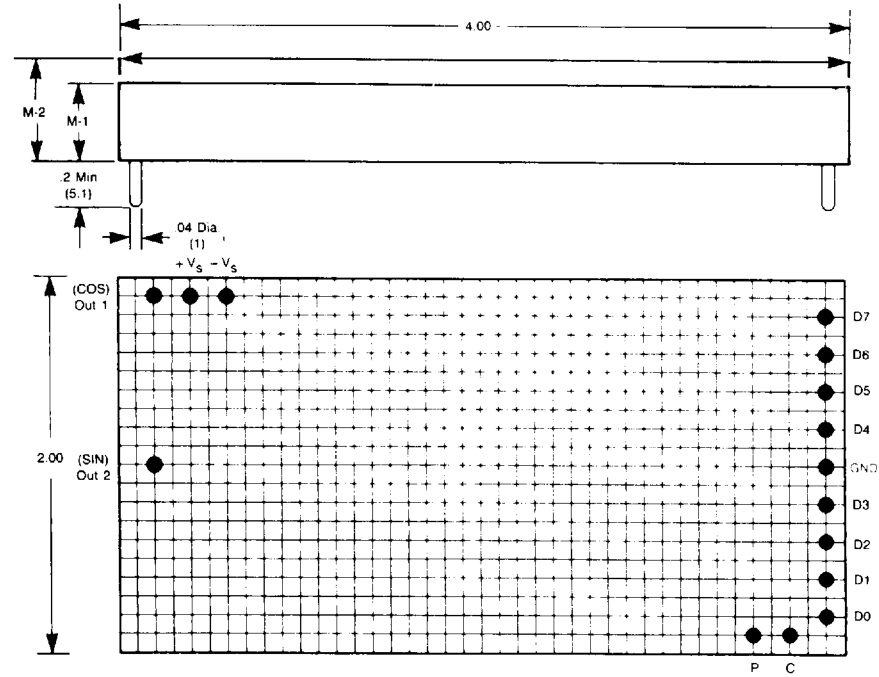
810 SERIES PACKAGE AND PIN-OUT DATA

PACKAGE AND PIN-OUT DATA DIMENSIONS IN INCHES (MM)



0.1 (2.5) GRID
DIMENSIONS IN INCHES AND (MM)

CASE DIMENSIONS. ALL 810 SERIES MODELS

CASE	DIMENSIONS IN INCHES AND (MM)
M-1	2.0″W x 4.0″L x 0.6″H (51 x 102 x 15 mm)
M-2	2.0″W x 4.0″L x 0.4″H (51 x 102 x 10 mm)

TERMINAL KEY

In Analog Input Signal
Out Analog Output Signal
GND Power and Signal Return
"P" Transition Polarity Bit
"C" Tuning Strobe Bit
+Vs Supply Voltage, Positive
−Vs Supply Voltage, Negative

D_0 Tuning Bit 0 (LSB)
D_1 Tuning Bit 1
D_2 Tuning Bit 2
D_3 Tuning Bit 3
D_4 Tuning Bit 4
D_5 Tuning Bit 5
D_6 Tuning Bit 6
D_7 Tuning Bit 7 (MSB)

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810 SERIES
ORDERING INFORMATION

AVAILABLE 810 SERIES OSCILLATOR MODELS

MODEL NUMBER	TUNING (HZ) RANGE	MIN. STEP	CASE
810P8-2	1.0 to 256	1.0	M-1
810P8-3	10 to 2560	10	M-1
810P8-4	100 to 25.6k	100	M-2

HOW TO ORDER

The above table lists the available **810 Series** models, along with the frequency range, resolution and case style combinations that distinguish one model from another. Selection is the simple matter of choosing the oscillator model capable of generating the range of frequencies required by the application. NOTE: FOR LOWEST DC OFFSET AND BEST PERFORMANCE, SELECT THE LOWEST FREQUENCY MODEL CAPABLE OF SPANNING THE FREQUENCY RANGE OF INTEREST.

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