ULTRA-HIGH SPEED, 256K X 8 BIT PAGE MODE WITH EXTENDED DATA OUTPUT (EDO) AND $\overline{CAS}$ BURST MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE	45/45L	50/50L	55/55L	60/60L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	45 ns	50 ns	55 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	22 ns	24 ns	28 ns	30 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	20 ns	22 ns	25 ns	27 ns
Min. Read/Write Cycle Time, (t_{RC})	100 ns	110 ns	115 ns	120 ns
Min. $\overline{CAS}$ Burst Cycle Time (t_{BC})	15 ns	17 ns	20 ns	22 ns

2

Features

- 256K x 8-bit organization
- $\overline{RAS}$ access time: 45, 50, 55, 60 ns
- Page Mode with Extended Data Output for a sustained data rate of 50 MHz
- $\overline{CAS}$ Burst
  - 15 ns $\overline{CAS}$ cycle
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V53C8257H – 512 cycles/8 ms
- Low power dissipation
  - V53C8257H-60
    - — Operating Current – 135 mA max
    - — TTL Standby Current – 2.0 mA max
- Low CMOS Standby Current
  - V53C8257H – 1.0 mA max
- Available in 24 pin 300 mil Plastic DIP and 26/24 pin 300 mil SOJ packages
- Write per bit capability (upon request)

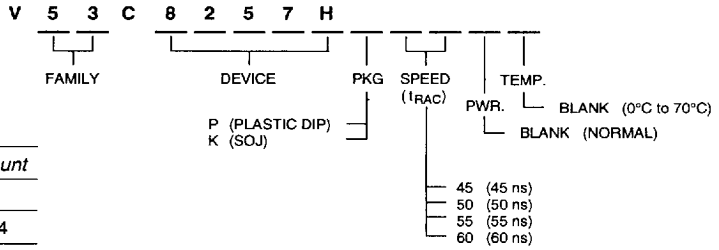
Description

The V53C8257H is a ultra high speed 262,144 x 8 bit CMOS dynamic random access memory. The V53C8257H offers a combination of features: Page Mode with Extended Data Output for high data bandwidth, $\overline{CAS}$ Burst Mode, and Low CMOS standby current.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Page Mode with Extended Data Output operation allows random access of up to 512 (x8) bits within a row with cycle times as fast as 20 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements. The $\overline{CAS}$ burst mode offers high-speed sequential data access within a page boundary. These features make the V53C8257H ideally suited for graphics, digital signal processing and high-performance computing systems.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power	Temperature Mark
	P	K	45	50	55	60	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank



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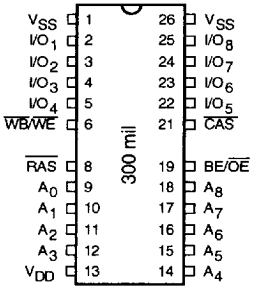
Description	*Pkg.*	*Pin Count*
Plastic DIP	P	24
SOJ	K	26/24

26/24 Lead SOJ PIN CONFIGURATION Top View



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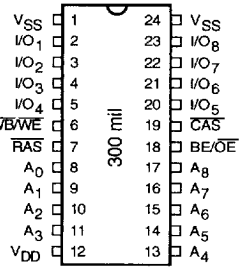
24 Lead Plastic DIP PIN CONFIGURATION Top View



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Pin Names

A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/WE}$	Write Enable, Mask Write Enable
BE/$\overline{OE}$	Output Enable, Burst Mode Enable
I/O_1–I/O_8	Data Input, Output
V_{DD}	+5V Supply
V_{SS}	0V Supply

*Absolute Maximum Ratings**

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

*Capacitance**

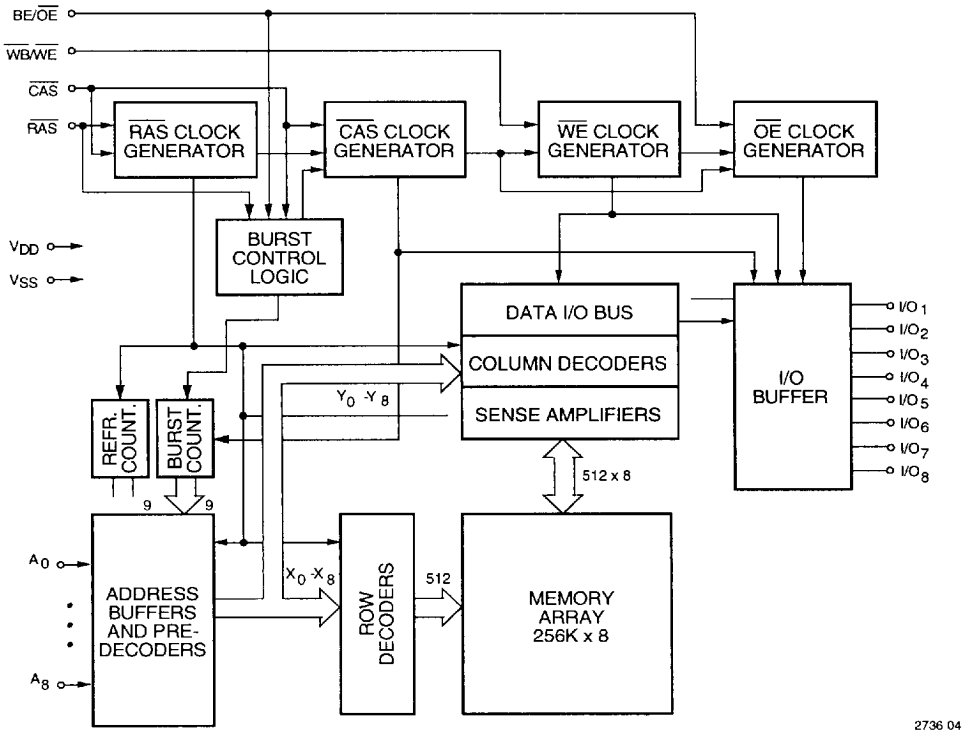
T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, BE/$\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram

256K x 8 Page EDO/Burst Mode



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DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C8257H Min.	Typ.	Max..	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)		−10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10		10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	45			160	mA	$t_{RC} = t_{RC}$ (min.) No burst	1, 2
		50			150			
		55			145			
		60			135			
I_{DD2}	V_{DD} Supply Current, TTL Standby				2	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	45			160	mA	$t_{RC} = t_{RC}$ (min.) No burst	2
		50			150			
		55			145			
		60			135			
I_{DD4}	V_{DD} Supply Current, EDO Page Mode Operation	45			95	mA	Minimum cycle	1, 2
		50			90			
		55			85			
		60			80			
	Burst Mode	45			130	mA		
		50			120			
		55			110			
		60			100			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				2.0	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				1.0	mA	$\overline{RAS} \ge V_{DD} - 0.2$ V, $\overline{CAS} \ge V_{DD} - 0.2$ V, All other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		−1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{DD}+1	V		3
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	45		50		55		60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	45	75K	50	75K	55	75K	60	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	100		110		115		120		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	35		40		45		50		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	45		50		55		60		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	8		8		10		10		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	31	19	36	20	40	20	45	ns	
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	4
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8		9		10		10		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	6		7		10		10		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	14		14		15		15		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	4		4		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	9		9		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		12		12		15		15	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$ (EDO)		12		12		15		15	ns	6, 7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		45		50		55		60	ns	6, 8, 9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		22		24		28		30	ns	6, 7, 10
21	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	Output buffer turn-off delay time	0	8	0	8	0	10	0	10	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	35		40		45		50		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	23	14	26	15	27	15	30	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH\ (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	14		14		15		15		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	14		14		15		15		ns	

AC Characteristics (Cont'd)

#	JEDEC Symbol	Symbol	Parameter	45		50		55		60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12, 13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	6		7		10		10		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	6		7		10		10		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	35		40		45		50		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	14		14		15		15		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	6		7		10		10		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	9		9		10		10		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	8		8		10		10		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	135		145		160		170		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	85		90		100		105		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	31		33		38		40		ns	12
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	65		70		80		85		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	50		54		62		65		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	41		43		55		58		ns	12
42	t_{CL2CL2}	t_{PC}	EDO Page Mode Read or Write Cycle Time	20		22		25		27		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	6		7		8		8		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	22		24		28		30		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		24		26		32		34	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	35		40		45		50		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	12		12		15		15		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	EDO Page Mode Read-Modify-Write Cycle Time	65		70		82		85		ns	

AC Characteristics (Cont'd)

#	JEDEC Symbol	Symbol	Parameter	45		50		55		60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
51		t_{WSR}	$\overline{WB}$ Setup Time	0		0		0		0		ns	
52		t_{RWH}	$\overline{WB}$ Hold Time	8		9		10		10		ns	
53		t_{EMS}	EDO Mode Setup Time	0		0		0		0		ns	
54		t_{EMH}	EDO Mode Hold Time	8		9		10		10		ns	
55		t_{MS}	Mask Data Setup Time	0		0		0		0		ns	
56		t_{MH}	Mask Data Hold Time	8		9		10		10		ns	
57	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
58		t_{REF}	Refresh Interval (512 Cycles)		8		8		8		8	ms	17

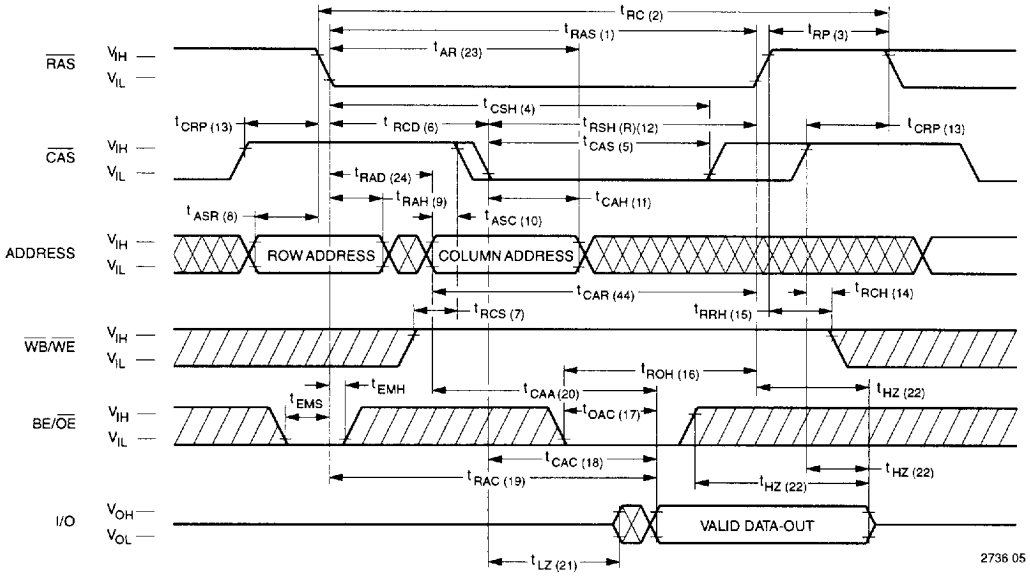
$\overline{CAS}$ Burst Mode

#	JEDEC Symbol	Symbol	Parameter	45		50		55		60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
59	NA	t_{BC}	Burst Cycle Time	15		17		20		22		ns	18
60	NA	$t_{ASC(B)}$	Burst Mode Column Address Setup Time	0		0		0		0		ns	18
61	NA	$t_{CAH(B)}$	Burst Mode Column Address Hold Time	6		7		10		10		ns	
62	NA	$t_{CAC(B)}$	Burst Mode CAS Address Access Time (Burst)	12		12		15		15		ns	
63	NA	t_{ASB}	Burst Mode Access Setup Time	22		24		28		30		ns	18
64	NA	$t_{CAS(B)}$	Burst Mode CAS Low Time	4.5		5		6		6		ns	
65	NA	$t_{CP(B)}$	Burst Mode CAS High Time	6		7		7		8		ns	
66	NA	$t_{CAH(B)}$	Burst Mode CAS Hold Time	10		10		10		10		ns	
67		t_{BSR}	Burst Mode Control Setup Time	10		10		10		10		ns	
68		t_{BHR}	Burst Mode Control Hold Time	12		12		15		15		ns	
69		$t_{COH(B)}$	Data Out Hold after $\overline{CAS}$ low	5		5		5		5		ns	
70		$t_{WCS(B)}$	Burst Write Command Setup Time	0		0		0		0		ns	19
71		$t_{WCH(B)}$	Burst Write Command Hold Time	6		7		10		10		ns	19
72		$t_{RCS(B)}$	Burst Read Command Setup Time	0		0		0		0		ns	19
73		$t_{RCH(B)}$	Burst Read Command Hold Time	6		7		10		10		ns	19

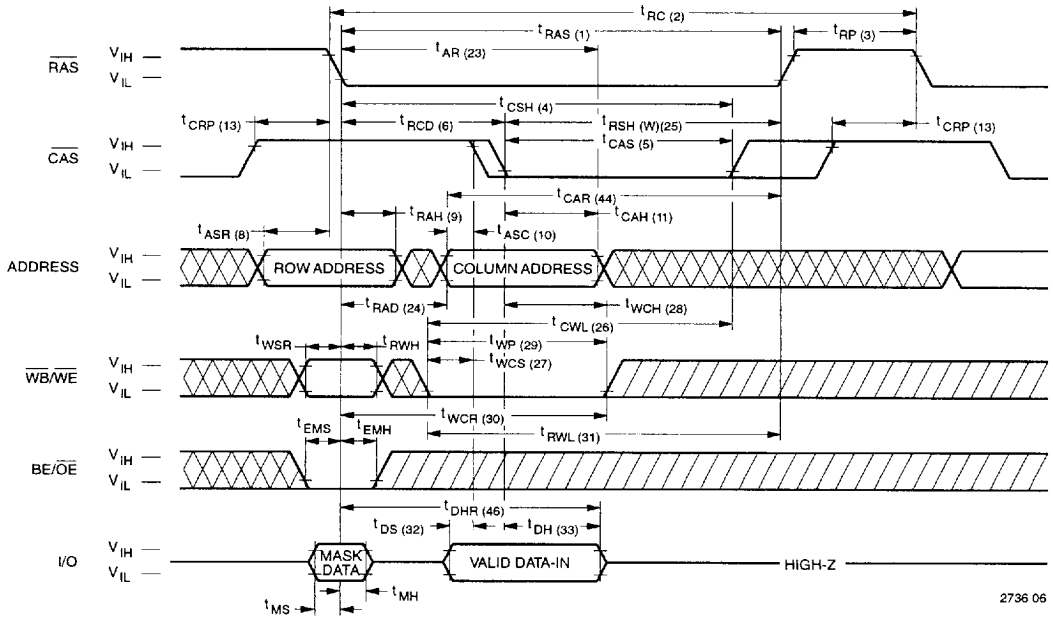
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in EDO Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 50 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WB/WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns except Burst Mode t_T. t_T should be 3 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. To meet t_{BC} (min.), $t_{ASC(B)}$ should be t_{ASB} (min.) – t_{BC} (min.). Otherwise, t_{BC} of first $\overline{CAS}$ cycle should be t_{ASB} (min.) – t_{ASC}(B).
19. During $\overline{RAS}$ low time, burst mode is either set to read mode or write mode only.

Waveforms of Read Cycle

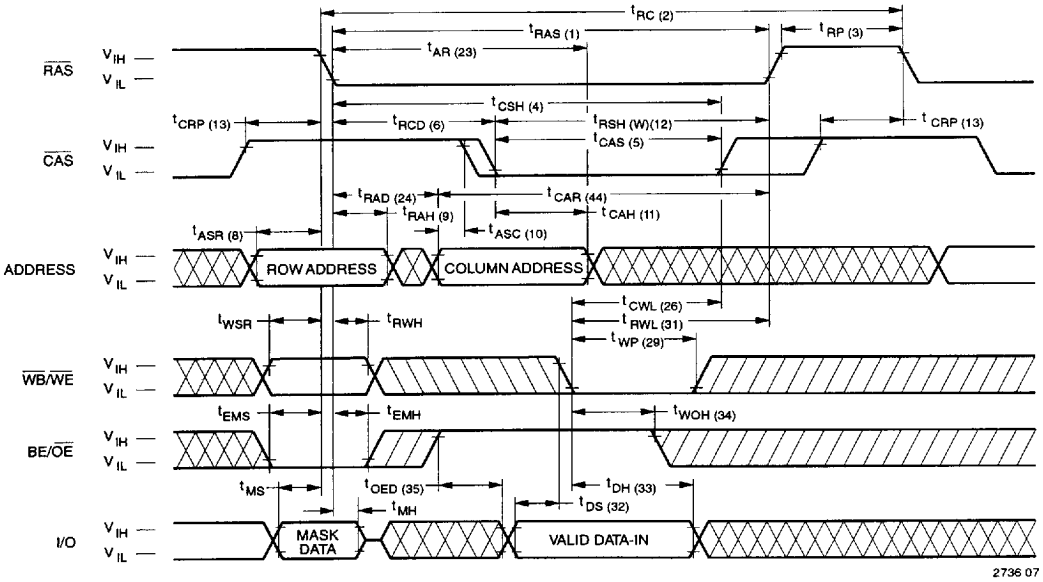


Waveforms of Early Write Cycle

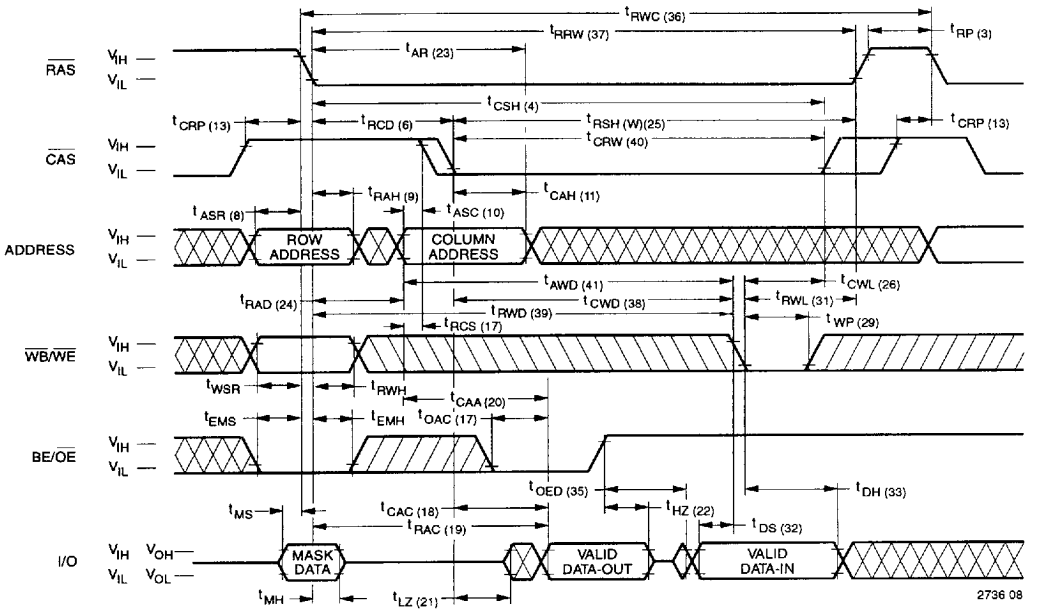


V53C8257H Rev. 1.0 January 1995

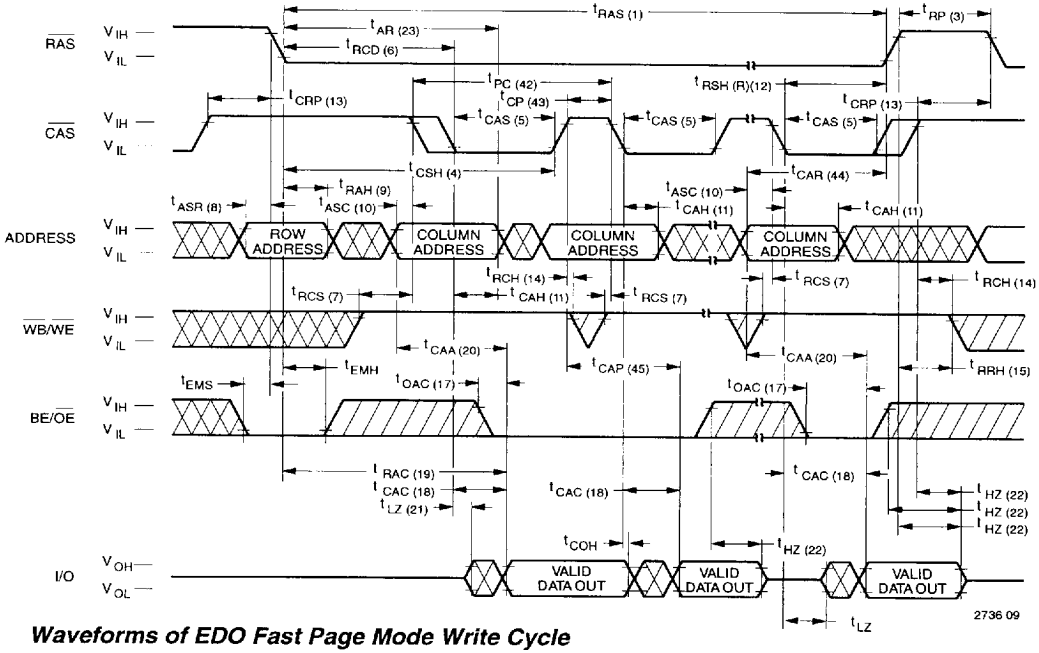
Waveforms of $\overline{OE}$-Controlled Write Cycle



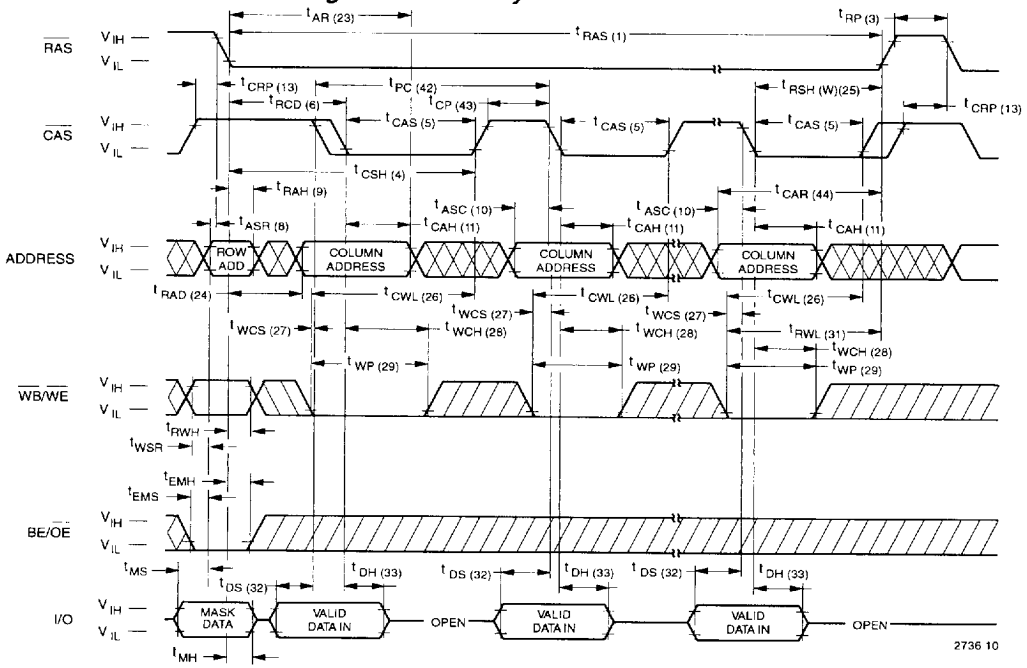
Waveforms of Read-Modify-Write Cycle



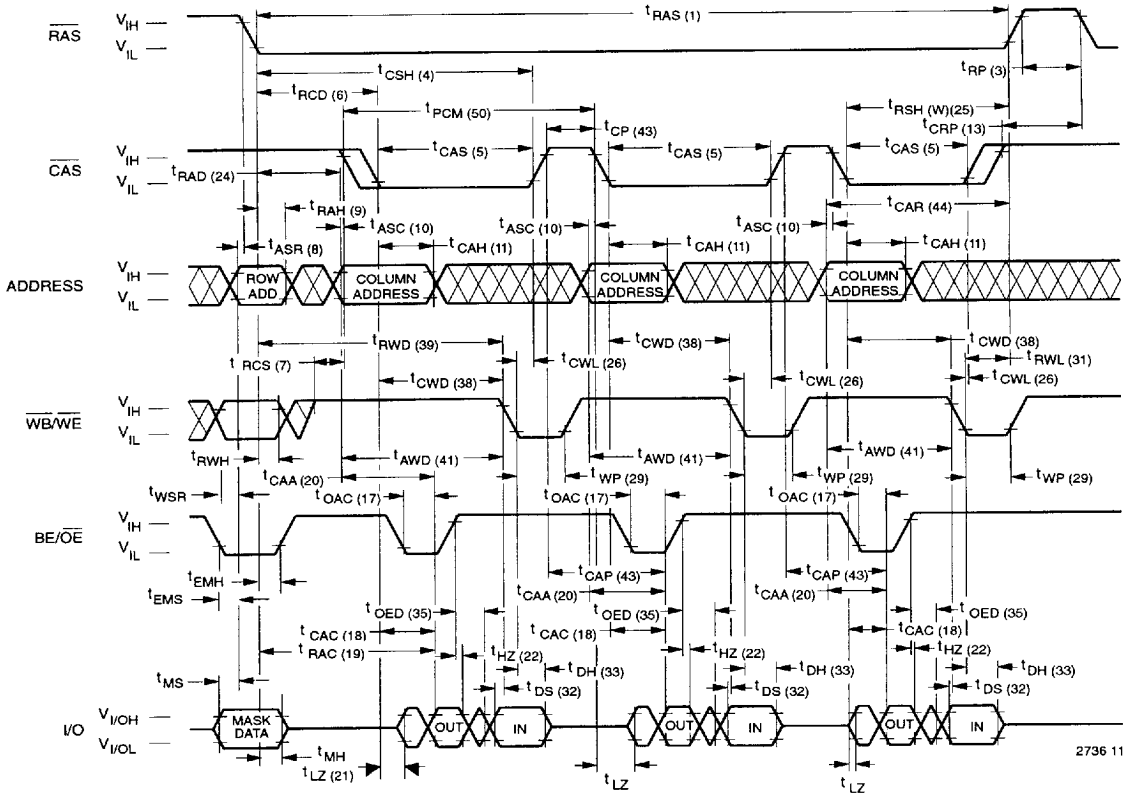
Waveforms of EDO Fast Page Mode Read Cycle



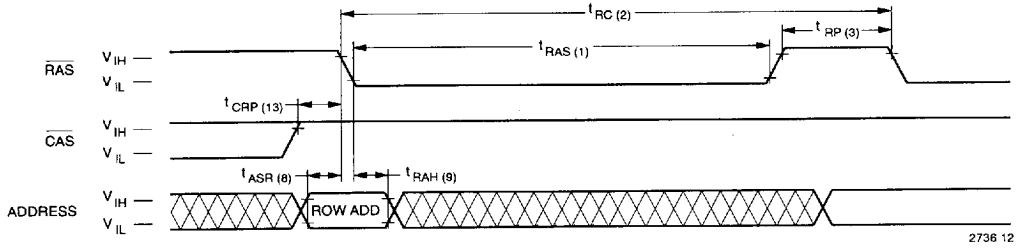
Waveforms of EDO Fast Page Mode Write Cycle



Waveforms of EDO Page Mode Read-Write Cycle

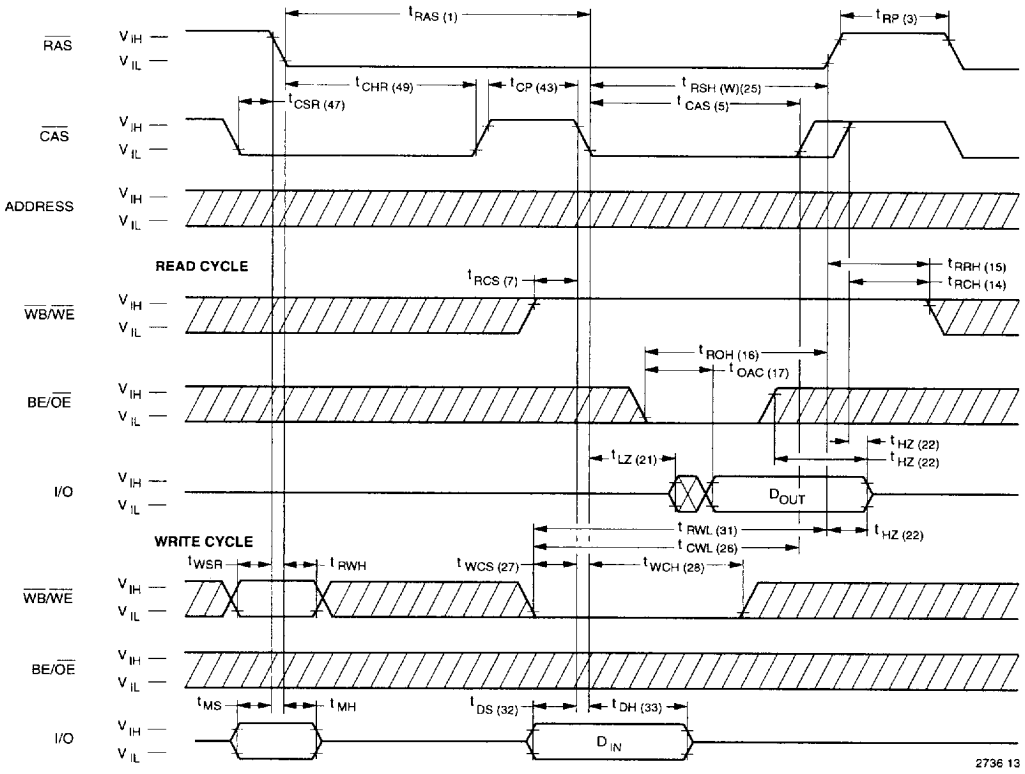


Waveforms of $\overline{RAS}$-Only Refresh Cycle

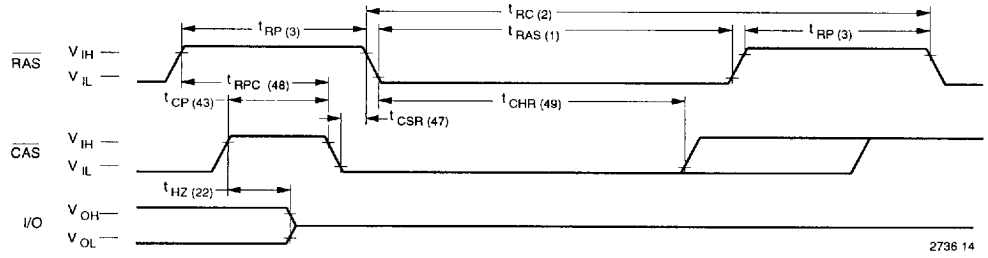


NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

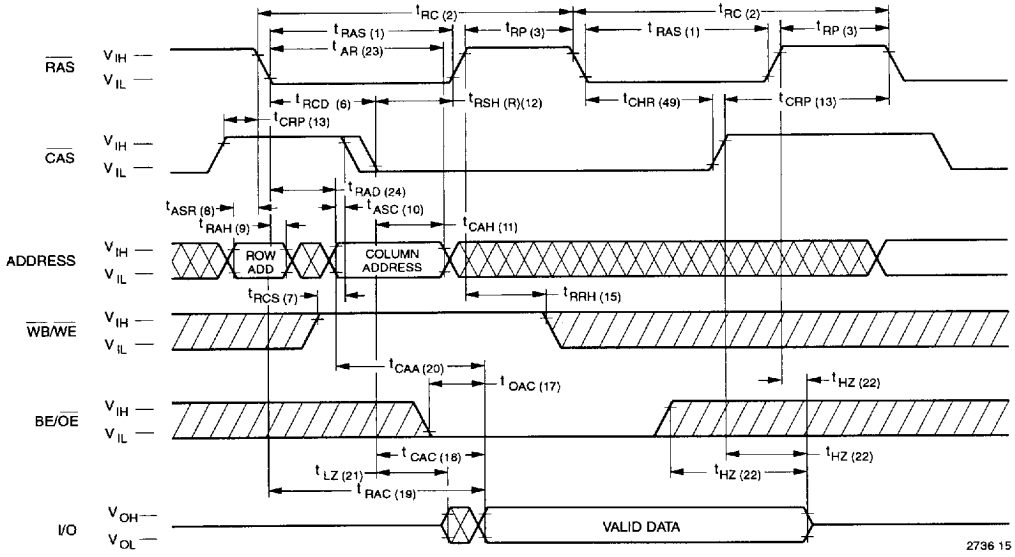


Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

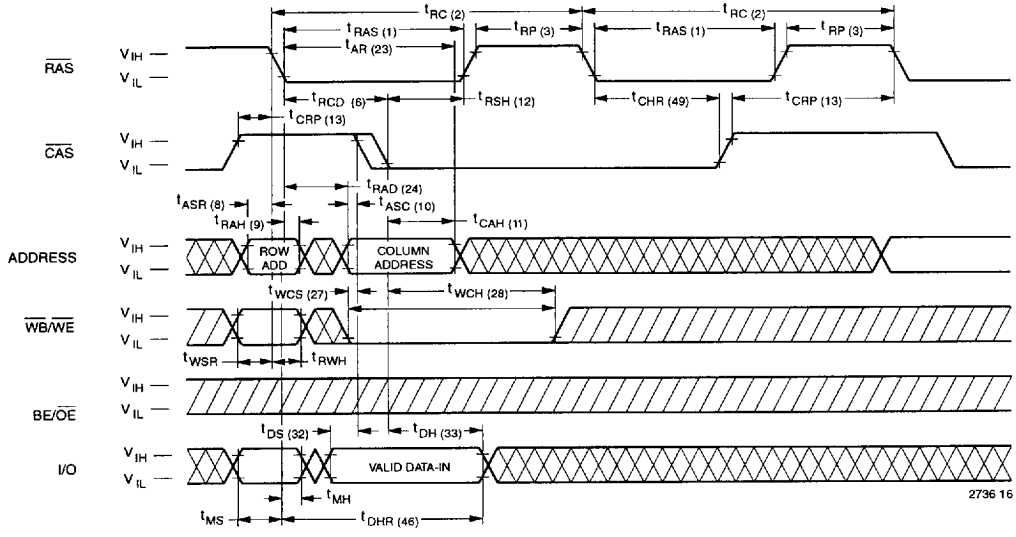


NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

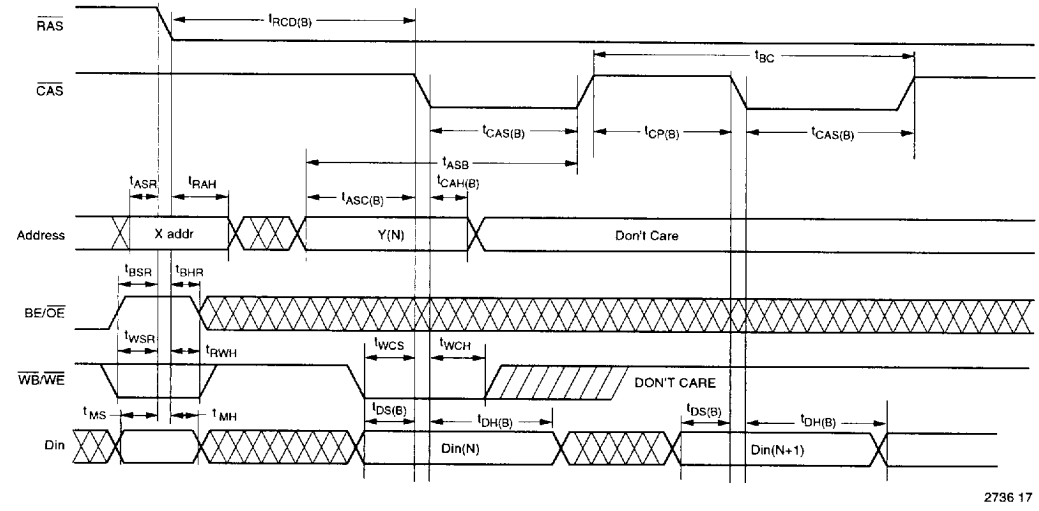
Waveforms of Hidden Refresh Cycle (Read)



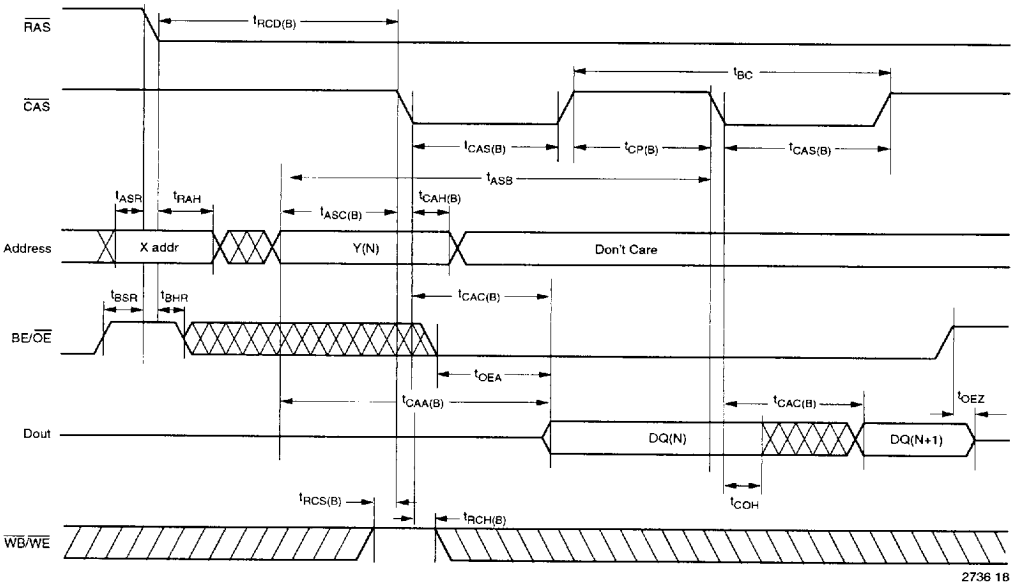
Waveforms of Hidden Refresh Cycle (Write)



Waveforms of Burst Write



Waveforms of Burst Read



Functional Description

The V53C8257H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C8257H reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WB}/\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WB}/\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WB}/\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WB}/\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WB}/\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WB}/\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

V53C8257H also offers a write-per-bit function. When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$. The Write-per-bit function is enabled. The mask data on I/O pins is latched into the write mask register. Data is written into the DRAM on data lines where the Write-Mask data is a logic "1". Writing is inhibited on data lines where the Write-Mask data in logic "0". The Write-Mask data is valid for only one cycle.

Extended Data Output Page Mode

The V53C8257H offers fast access within a row. Unlike ordinary fast page mode DRAM, the V53C8257H output remains active and valid even after $\overline{CAS}$ goes high and it will stay valid for 5 ns after $\overline{CAS}$ changes low. This feature allows the V53C8257H to $\overline{CAS}$ cycle faster than ordinary page mode DRAM since the cycle time can be short as data access time.

The outputs are disabled at the t_{HZ} time after $\overline{RAS}$ and $\overline{CAS}$ are high. The t_{HZ} time is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$ whichever occurs last. In addition, high on $\overline{OE}$ input and activation of the write-cycle will also disable the outputs.

The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Burst Mode Operation

Low-to-High transition on a $\overline{CAS}$ toggles on-chip column burst counter and provides the fastest data access. The burst mode can be activated when a high on a $BE/\overline{OE}$ input sensed by a high-to-low transition on a $\overline{RAS}$. No address information is required during burst mode operation. The burst range can be extended all page boundary. Read-Modify-Write operation is not permitted during burst mode operation since the burst mode offers sequential read or write. Mix read and write operation accomplished by EDO page mode operation.

Data Output Operation

The V53C8257H Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition enables the internal I/O path. A $\overline{CAS}$ high transition or $\overline{RAS}$ high transition, whichever occurs later, disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers. During a Write cycle, if $\overline{WE}$ goes low at a time when the $\overline{CAS}$ is low, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C8257H uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C8257H offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C8257H power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C8257H is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C8257H Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{WE}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{OE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
EDO Page Mode Read	Data from Addressed Memory Cell
EDO Page Mode Write Cycle (Early Write)	High-Z
EDO Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z