SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MK5025 DAISY CHAIN DMA

INTRODUCTION

The SGS-Thomson MK5025 X.25 Link Level Controller is a VLSI device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. The MK5025 also supports X.32 (XID) and X.75 as well as single channel LAPD for ISDN with its UI frames and extended addressing capabilities.

PURPOSE

Although the MK5025 Data Sheet and Technical Manual provide detailed timing diagrams that specifiy the relationships of the host interface signals to one another for the sole requestor DMA configuration, the designer may find it helpful to know the timing for the MK5025 as an element in a DMA daisy chain. The purpose of this application brief is to provide a description of the MK5025 host interface in a daisy chain configuration, and some suggestions on how to implement the daisy chain.

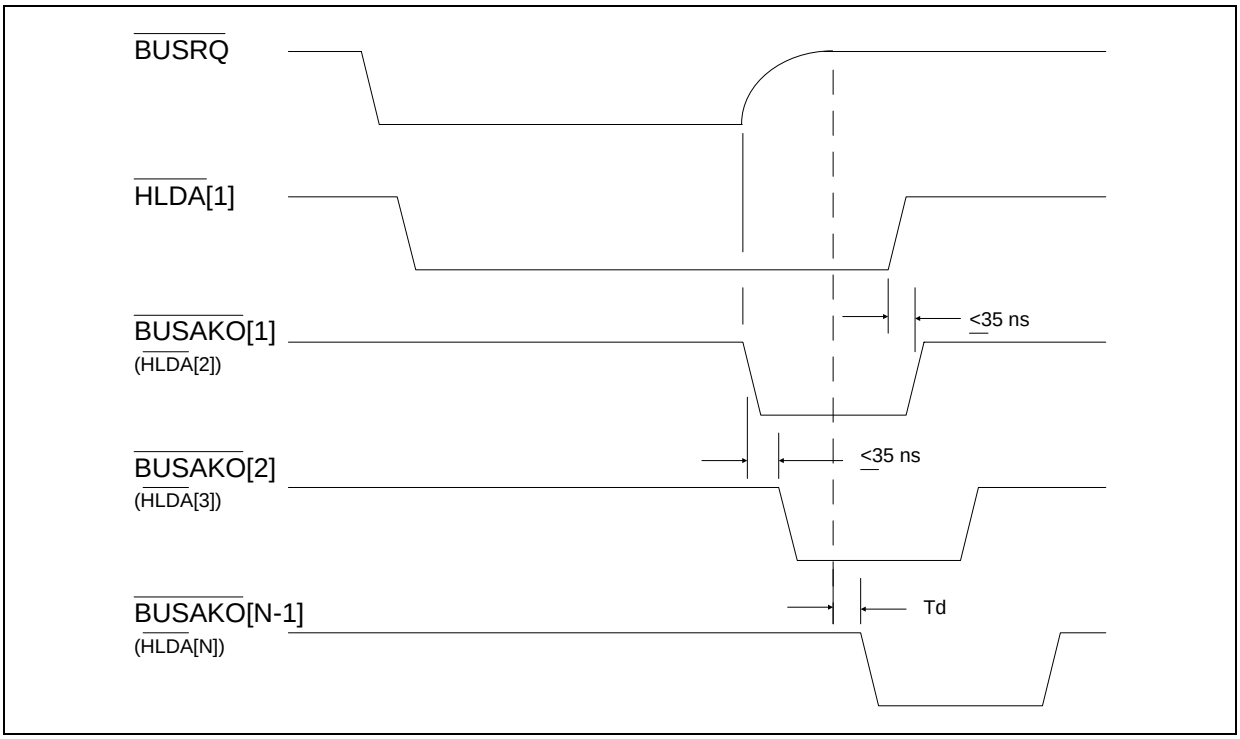
It should be also be noted that although the timing diagrams in this document are provided to facilitate the design process, the timing requirements in the Data Sheet must still be met to ensure proper operation.

DAISY CHAIN OPERATION

The daisy chain operation of the MK5025 is selected by setting the BCON bit of CSR4 so that pins 15, 16, and 17 are redefined as BYTE, BUSAKO, and BUSRQ respectively.

In the daisy chain mode the MK5025 DMA operation is still the same in that it still requests the bus by asserting HOLD/BUSRQ (pin 17), but it will not do so unless both BUSRQ and HLDA are inactive (de-asserted). Also, the granting of the bus to the MK5025 should still consist of asserting HLDA (pin 19) as indicated in the timing diagrams in the Technical Manual. However, if the MK5025 receives HLDA when it is not requesting the bus, the BUSAKO output (pin 16) will be driven low.

Figure 1: Daisy Chain Bus Master Timing



Additionally, if HLDA is still asserted after BUSRQ is deasserted by the MK5025, then the BUSAKO output will be driven low until HLDA is deasserted. Figure 1 provides the typical timing relationships for this mode of operation.

As can be seen in this diagram, there is a possibility of the BUSAKO output being asserted at the end of a DMA cycle from the time BUSRQ is deasserted until HLDA is deasserted. This pulse will not cause any problems unless it is delayed (by propagating through a large daisy chain) such that Td (shown in Figure 1) is sufficiently long to allow an oportunity to request the bus and see this pulse as a HLDA acknowledging the bus request.

SUGGESTED DAISY CHAIN CONFIGURATION

In order to resolve the possibility of a problem resulting from the propagation of the end of DMA cycle BUSAKO pulse, it is suggested that a daisy chain arragement such as that shown in Figure 2 or 3 be used for daisy chains of more than 2 MK5025 devices. In the arrangement shown in Figure 2, a latch is added to the end of the daisy chain for the purpose of latching BUSRQ low (asserted) until BUSAKO has propagated through the daisy chain. In this manner another MK5025 will not request the bus until BUSAKO has propagated through the entire chain, resetting the latch and allowing BUSRQ to go inactive. It should be noted that the output of the latch drives the enable of a tri-statable inverter to avoid contention on BUSRQ.

The solution suggested in Figure 2 could of course also be implemented with a PLD device such as an SGS-THOMSON GAL 20V8. The PLD device should be programmed such that it

Figure 2: Suggested Daisy Chain Configuration

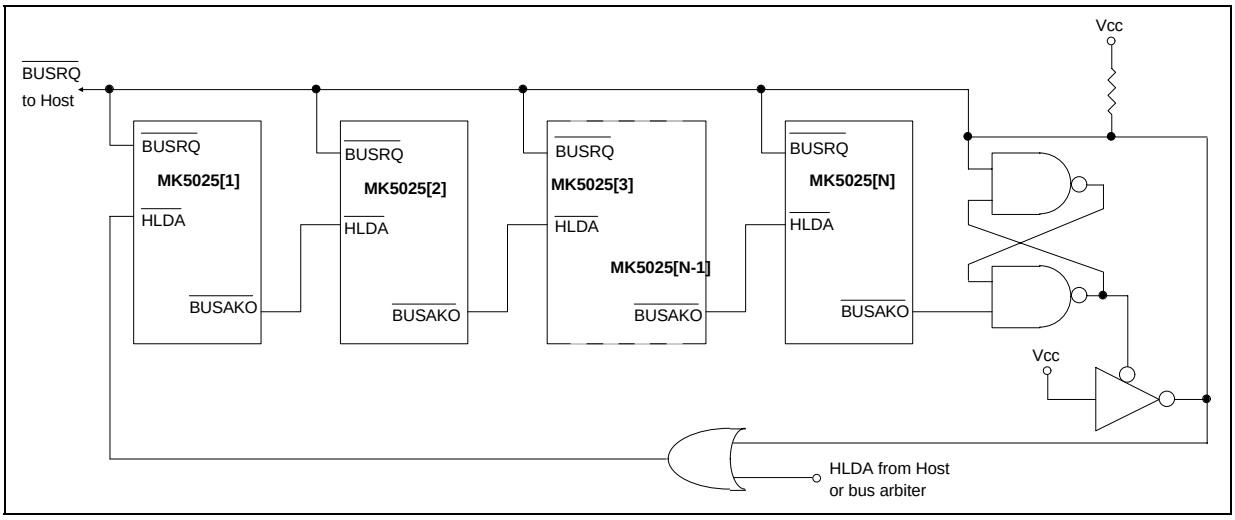
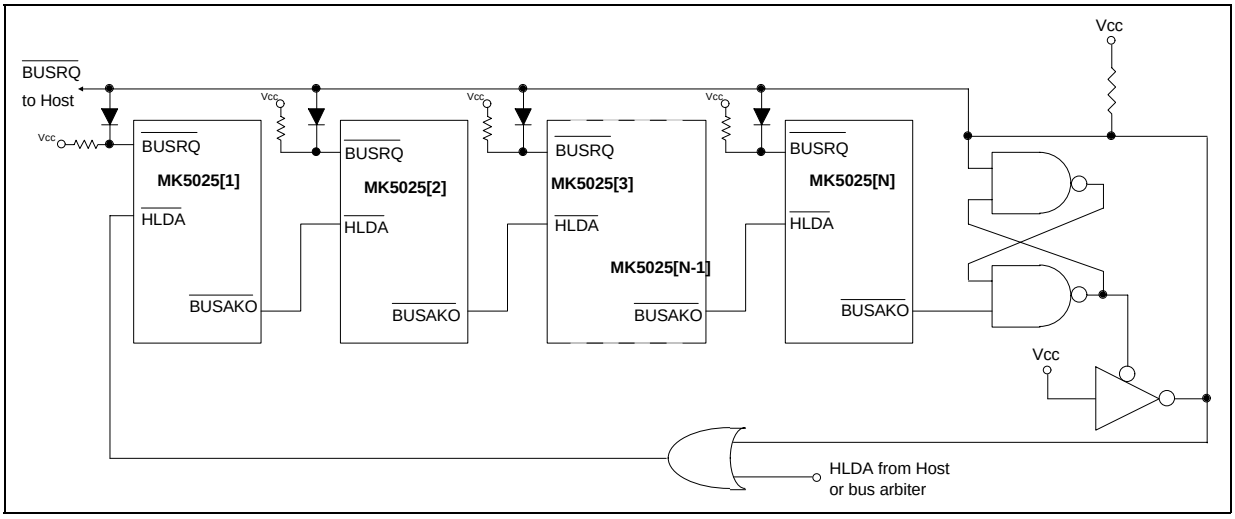


Figure 3: Round-Robin Daisy Chain Configuration



implements the following set of conditions:

IF BUSRQ=0
LATCH BUSRQ=0 AND HLDA=0
IF BUSAKO[N]=0
RELEASE BUSRQ

where BUSAKO[N] is from the last device in the daisy chain.

With this configuration the bus will typically be relenquished by the daisy chain in between each MK5025 bus master cycle or burst. The exception to this is when two or more MK5025 devices request the bus simultaneously, in which case the devices would each obtain the bus in order of priority as bus acknowledgement (HLDA to BUSAKO) propagates through the daisy chain.

A variation to the suggested daisy chain operation is shown in Figure 3. To each MK5025 there is added a pull-up resistor and a schottky diode in series with BUSRQ. This allows each MK5025 in the chain to request the bus regardless of whether or not another MK5025 has already requested or posseses the bus at the time. However, each device will not get the bus until the bus acknoledgement (HLDA) is passed on to the next device in the chain (through BUSAKO). Thus, in a Round-Robin fashion, each MK5025 gets an equal opportunity to obtain the bus, whereas in Figure 2 the MK5025[1] has first priority, followed by MK5025[2], if both request the bus simultaneously.

The decision on which approach to use depends upon the task required of each MK5025 and the available bus bandwidth. If the Figure 2 scheme is used, it would be prudent to place the devices operating at the higher data rates in the higher priority positions in the daisy chain. If the Round-Robin approach is used it is important to realize that once bus mastership is granted by the host, it is possible that the bus may not be relinquished until all devices in the chain have had at least one DMA cycle of bus mastership.

BUS RELEASE OPERATION

In the daisy chain or sole requestor configuration the use of the Bus Release function may be useful to allow the designer to force the MK5025 to relinquish the bus prior to completeion of a DMA burst. The Bus Release function is programmed by setting bit BUSR in CSR4<06>. Setting this bit causes pin 15 to be defined as BUSREL. The purpose of the BUSREL (pin 15) function is to allow an orderly abort to a MK5025 DMA burst after completion of the current bus transfer cycle.

It is important to note that the MK5025 has programmable burst size of 2 bytes, 16 bytes, or unlimited (typically 64-66 bytes), and that DMA bursting is only used for transfers of received and transmitted data. All buffer management functions are performed by the MK5025 using single word DMA cycles. This includes reading the Initialization Block, updating the Status Buffer, managing the descriptor rings, etc.

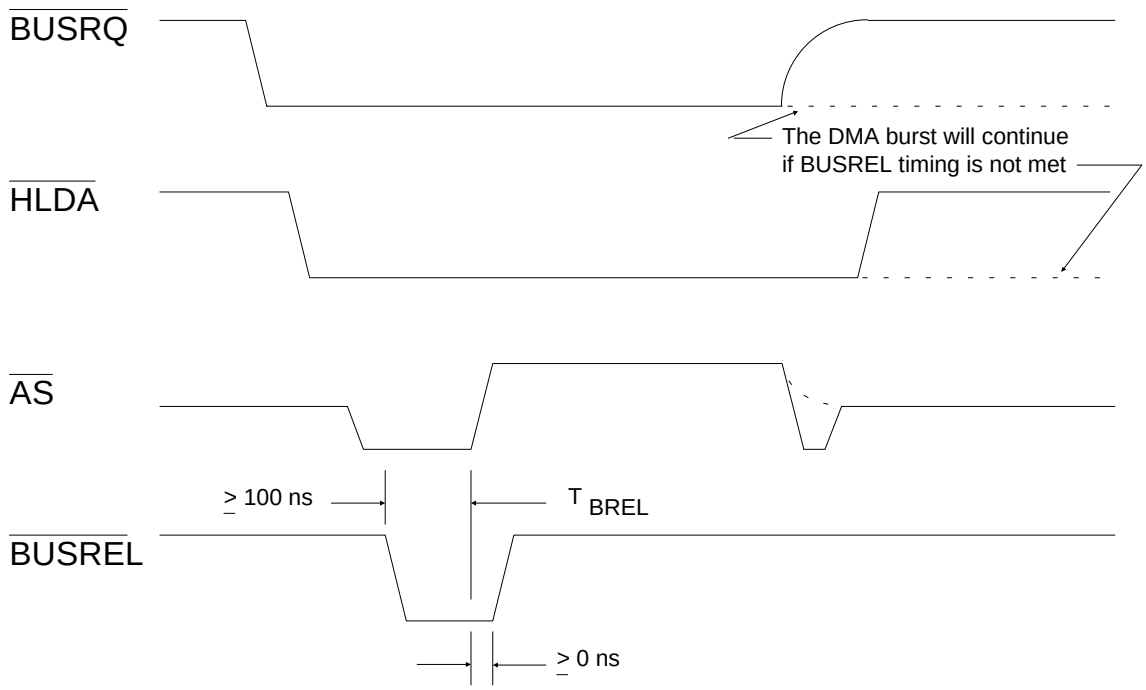
Although the MK5025 does support transmission and reception of odd-byte frames (MCNT, Message Byte Count may be odd), it is important to note that it does only word wide DMA transfers (no single byte transfers). It is because of this that the MK5025 requires that all data structures (including BCNT, Buffer Byte Count) and buffers be word aligned. Therefore the BYTE, BM0 and BM1 signals are never used by the MK5025 to indicate single upper or lower byte transfers. So there should be no concern about redefining these pins as BUSAKO and BUSREL.

From the timing diagrams in Figure 4, it should be seen that BUSREL must be asserted at least 100 ns prior the rising edge of AS (or falling edge of ALE) in order for BUSREL to be recognized within that DMA cycle. BUSREL can be deasserted coincident with the rising edge of AS. If BUSREL is asserted too late to be recognized within in the current DMA cycle, then it should be held asserted (or be re-asserted at least 100 ns prior) to the rising edge of AS of the following DMA cycle, in order for that cycle to be the last in the burst.

CONCLUSION

The MK5025 offers great flexibility to the data communications system designer. The on-chip protocol processing may be used to save the designer much time in implementing standard protocols such as X.25, LAPB, ISDN LAPD, X.32, and X.75, and the daisy chain information with associated timing diagrams are provided to further facilitate the design process.

Figure 4: Bus Release Timing



NOTE: The T_{BREL} setup time must be met in order for BUSREL to be recognized within that DMA cycle (causing the DMA burst to end on that cycle).