



## INTERFACING BETWEEN LVDS AND HIGH SPEED DIFFERENTIAL LOGIC FAMILIES

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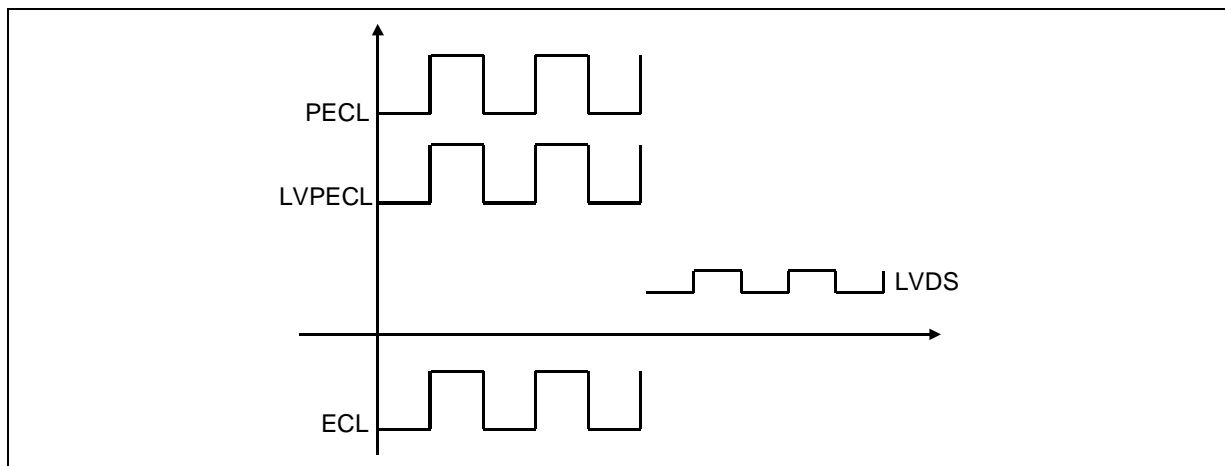
### 1. ABSTRACT

This application note provides interfacing solutions between some of the popular standard differential logic families and LVDS technology.

### 2. INTRODUCTION.

LVDS signals are differential signal technologies with a swing of 250 to 400mV and a DC offset of 1.2V. They are used today to interface between CMOS and BICMOS ASICs supplied with 3.3V or cell. LVDS, LVPECL, PECL and ECL are all differential technologies but with different swings and offsets (see figure 1).

**Figure 1: Voltage Levels**



This application note will show the possible interface between the LVDS device and the other differential signal levels listed above. It will also give suggestions on how to interface supplied positive and negative devices.

Due to its speed capability, the application board requires a proper technical high speed layout, otherwise the system performance will be reduced.

As a general guideline to get better performance from the PCB, the transmission striplines should be adapted as specified:

- The input line must be routed away from the output lines or separated from the larger swings;
- the lines must be as short as possible;
- the termination line resistors must be the nearest to the receiver;
- the use of surface mount components are recommended.

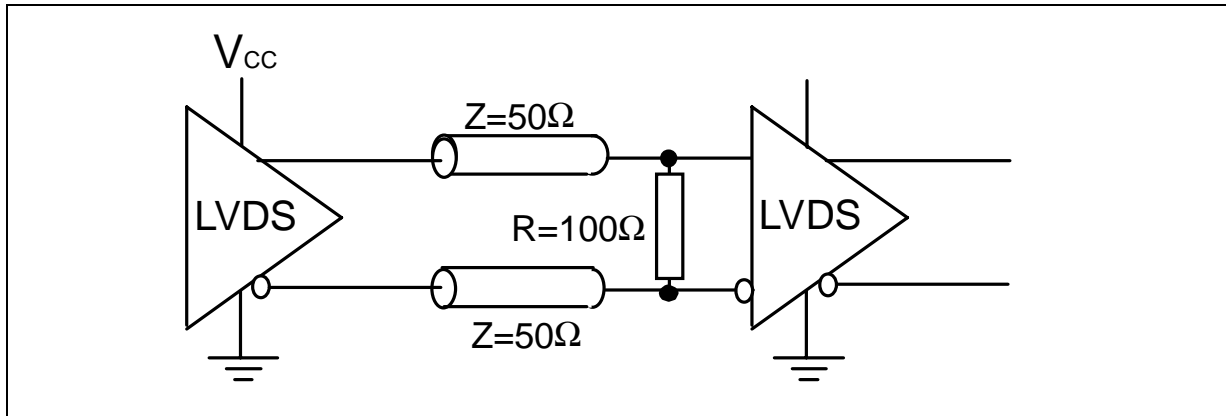
3. OVERVIEW OF FAMILIES.

3.1 LVDS.

LVDS outputs always require a 100Ohm load between the differential output because they work like a 100Ohm current source of 3.2mA. This load also terminates the 50Ohm controlled impedance line.

LVDS technology is not dependent on a specific power supply, meaning that there is an easy migration path to lower supply voltages, such as 3.3V or even 2.5V, while still maintaining the same performance.

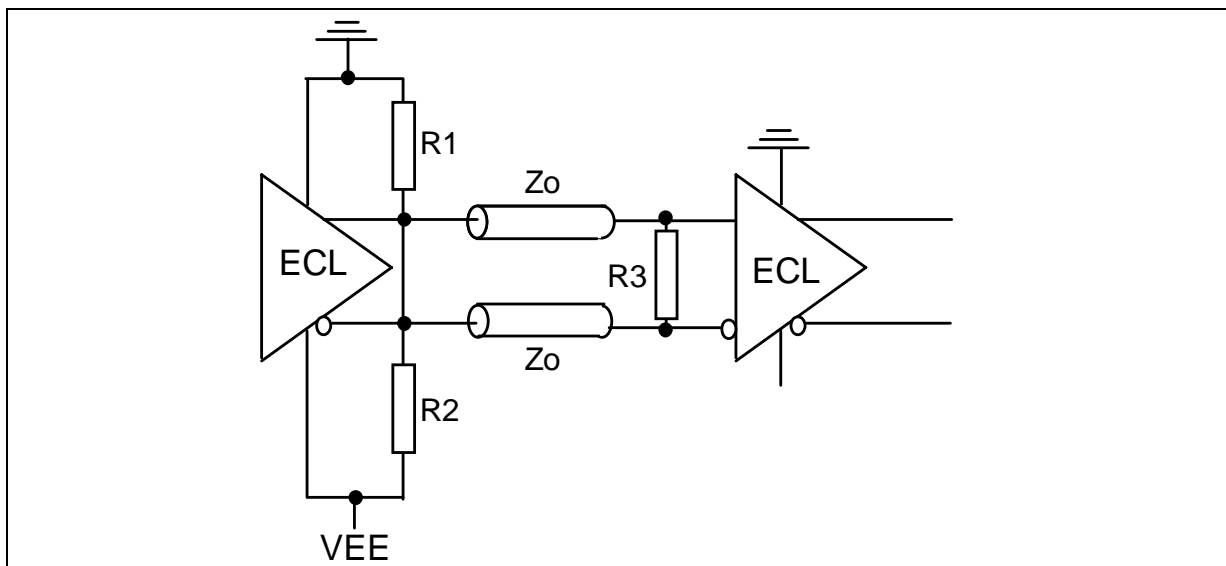
Figure 2: LVDS Output Configuration



3.2 ECL.

This is the first differential high speed logic family ever introduced and one of today's fastest digital logics. However, the drawback of this technology is the negative voltage needed in relation to the actual supply voltage commonly used. ECL outputs are open emitter outputs, requiring a DC path with a more negative supply than VOL.

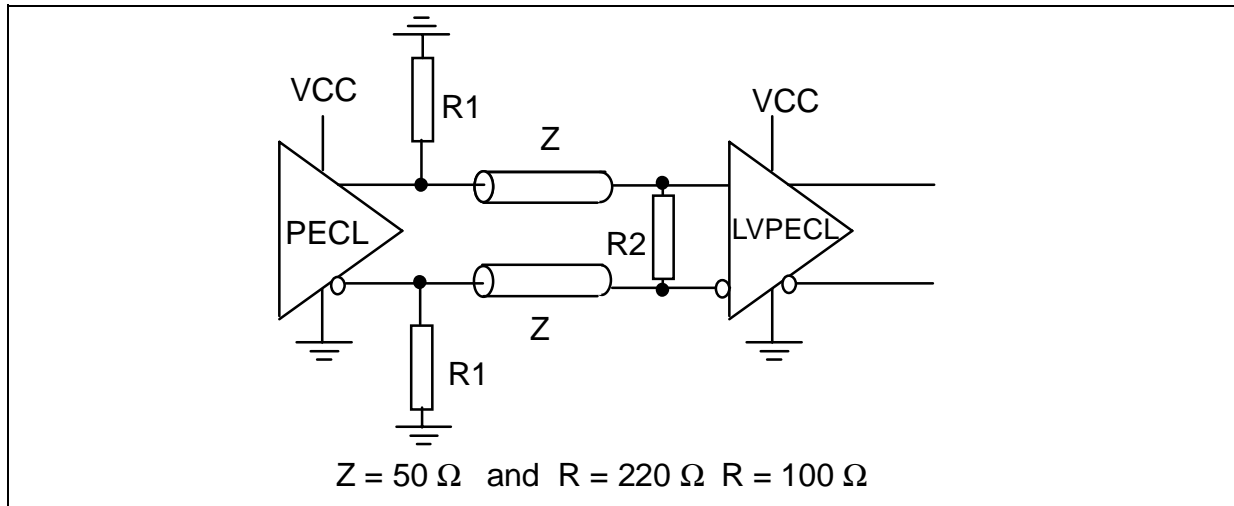
Figure 3: ECL Output Configuration



**3.3 PECL.**

The positive supply voltage of this family is a remedy to the disadvantages of the negative supply voltage of ECL technology. The PECL technology works at  $5V \pm 5\%$ , while for low voltage applications the LVPECL should be used, which has a 3.3V supply.

**Figure 4: PECL Output Configuration**



**4. LVDS FAMILY SPECIFICATIONS.**

**Table 1: LVDS driver DC characteristics (Driver cells are terminated with 100Ohm built-in)**

Symbol	Parameter	Minimum	Maximum
Vod	Output diff voltage	250mV	450mV
Vos	Output offset	1125mV	1375mV
$\Delta  Vod $	Change in  Vod  between 0 and 1		50mV
$\Delta  Vos $	Change in Vos between 0 and 1		50mV
Isa / Isb	Output current drivers shorted to GND		24mA
Isab	Output current drivers shorted together		12mA
Ixa / Ixb	Power off output leakage Vcc=0V		1μA

**Table 2: LVDS receiver DC characteristics (Receiver cells must be adapted with an external 100Ohm)**

Symbol	Parameter	Minimum	Maximum
Vi	Input voltage range V iA or V iB	0V	2.4V
Vidth	Input differential threshold	-0.100V	0.100V
Vhyst	Input differential hysteresis	0.025V	

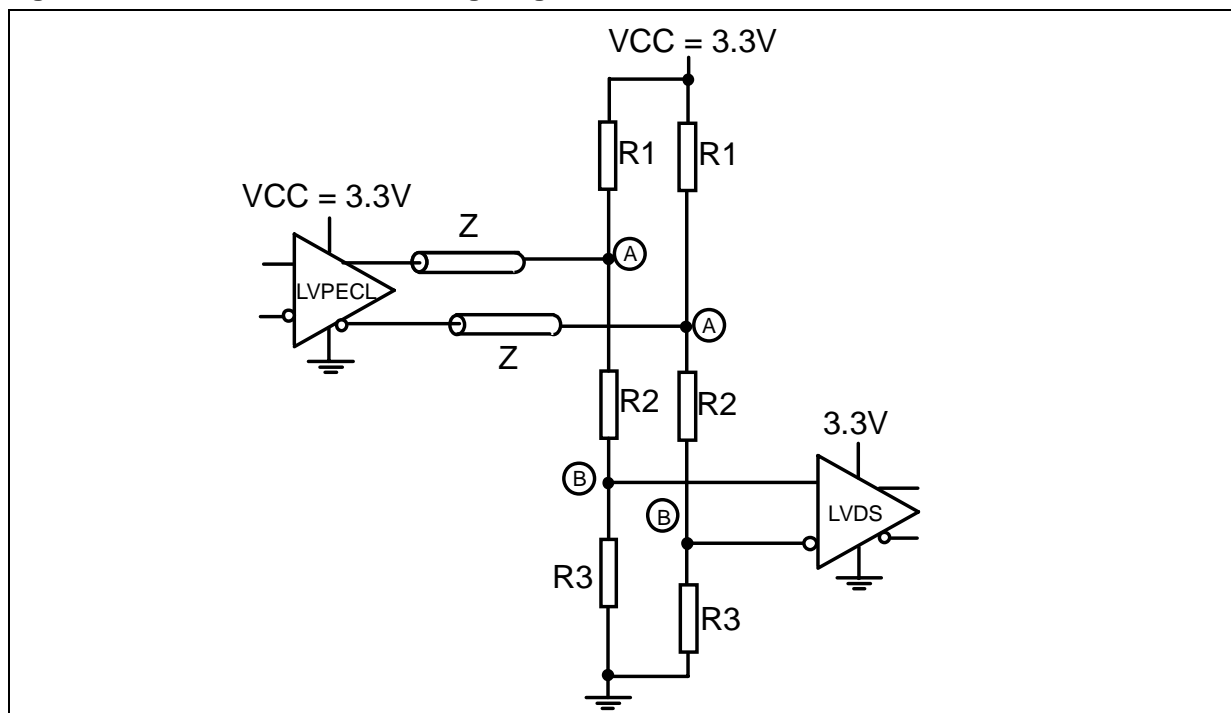
**Table 3: Electrical characteristics comparison of the differential logic families**

Symbol	Parameter	LVDS	LVPECL	PECL	ECL
VCC		3.3V	3.3V	5.0V	GND
VEE		GND	GND	GND	-5.2V, -4.5V or -3.3V
VOH	Minimum Output High Level	1.250V	2.275V	3.975V	-1.030V
VOH	Typical Output High Level	1.375V	2.345V	4.045V	-0.955V
VOH	Maximum Output High Level	1.600V	2.420V	4.120V	-0.880V
VOL	Minimum Output Low Level	0.900V	1.490V	3.190V	-1.810V
VOL	Typical Output Low Level	1.025V	1.595V	3.295V	-1.705V
VOL	Maximum Output High Level	1.250V	1.680V	3.380V	-1.620V

**5. INTERFACING LVPECL TO LVDS.**

To accomplish LVPECL to LVDS interfacing the proposal scheme uses the Thevenin Equation to fix the static level of the LVDS input. The LVPECL differential output swing will surely go over the LVDS input circuitry level.

**Figure 5: LVPECL to LVDS Interfacing Diagram**



This schematic is supplied by 3.3V, the termination of the transmission line Z can be calculated with the Thevenin equation.

- The characteristic line impedance:

$$Z = R1 \parallel (R2 + R3)$$

- The DC condition for point A is VCC -2V

- The DC levels at the LVDS input B are located within the LVDS input common mode range

$$PointA \quad (R1)/(R1 + R2 + R3) = (2V)/(VCC)$$

$$PointB \quad (R3)/(R1 + R2 + R3) = (VIL)/(VCC)$$

The LVDS input swing decreases depending on R2 and R3

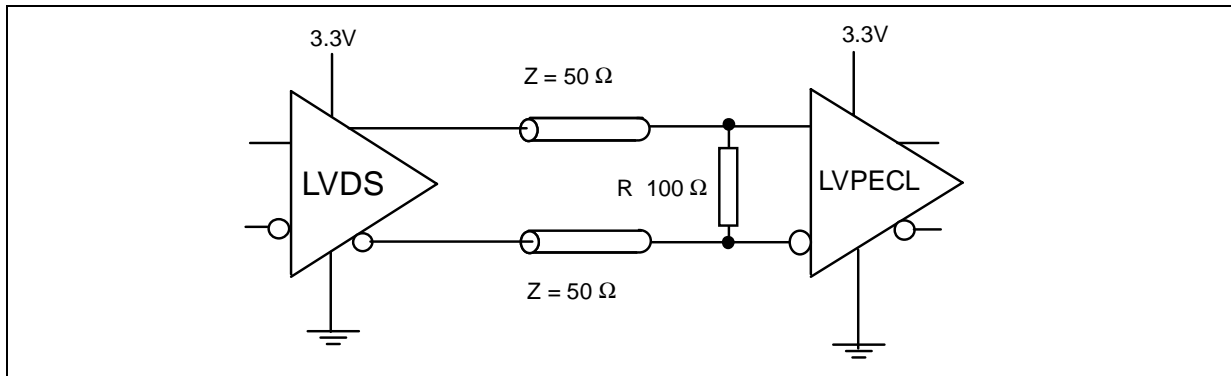
$$V_{swing \text{ in } pointB} = (R3)/(R2 + R3) * V_{swing \text{ in } pointA}$$

$$V_{ih} < 2.0V \quad \text{and} \quad V_{il} > 0V$$

**6. INTERFACING LVDS TO LVPECL.**

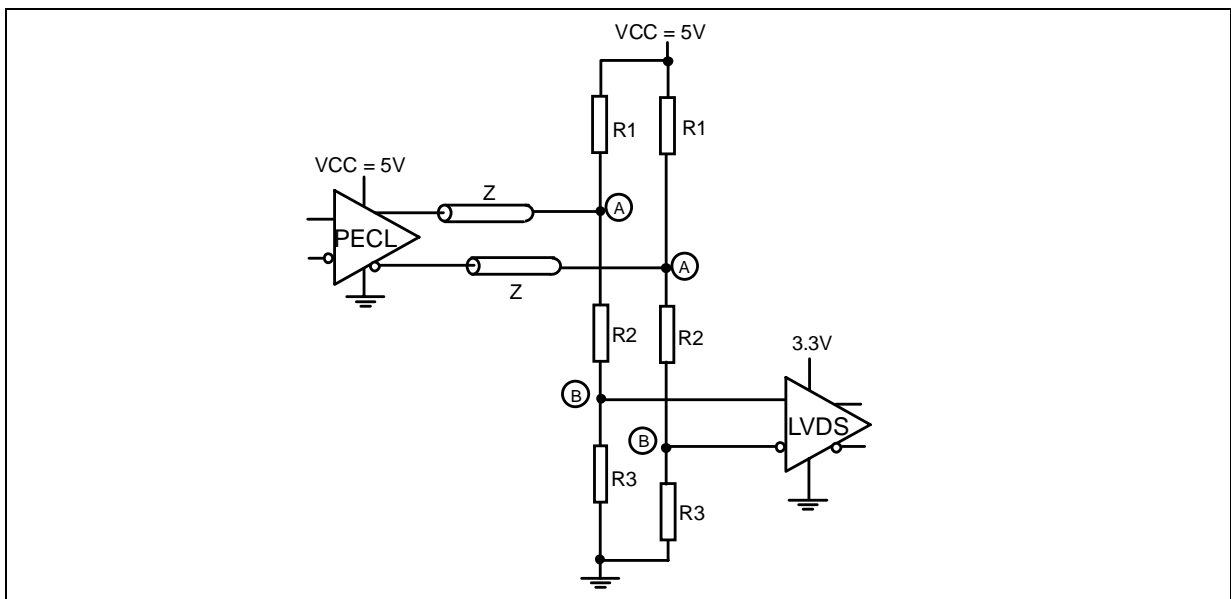
Direct interface is possible because of the common mode range of the LVPECL line receiver that is wide enough to process LVDS signals. The differential input voltage range of the LVPECL line receivers are specified wide enough to process LVDS signals.

**Figure 6: LVDS to LVPECL Interfacing Diagram**



**7. INTERFACING PECL TO LVDS.**

**Figure 7: Interfacing PECL to LVDS in the Thevenin Equation**



As described for LVPECL to interface from PECL to LVDS a thevenin equation should be applied. The Thevenin equation resistor terminates the transmission line Z near the receiver.

- The line characteristics impedance is:

$$Z = R1 \parallel (R2 + R3)$$

- The DC condition in point A is  $VCC - 2V$

- The DC levels at the LVDS input B are located within the LVDS input common mode range.

$$\text{pointA} \quad (R1)/(R1 + R2 + R3) = (2V)/(VCC)$$

$$\text{pointB} \quad (R3)/(R1 + R2 + R3) = (VIL)/(VCC)$$

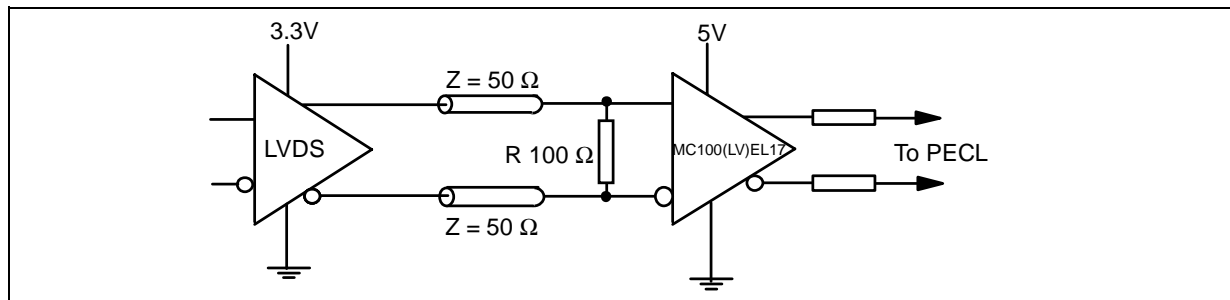
The LVDS input swing decreases depending on R2 and R3

$$V_{\text{swing in pointB}} = (R3)/(R2 + R3) * V_{\text{swing in pointA}}$$

### 8. INTERFACING LVDS TO PECL.

The direct translation between LVDS and PECL/LVPECL signals is not possible. This is because the LVDS output common mode and differential voltage are not compatible with PECL input levels. Devices like MC100(LV)EL17 should be used to translate these signals.

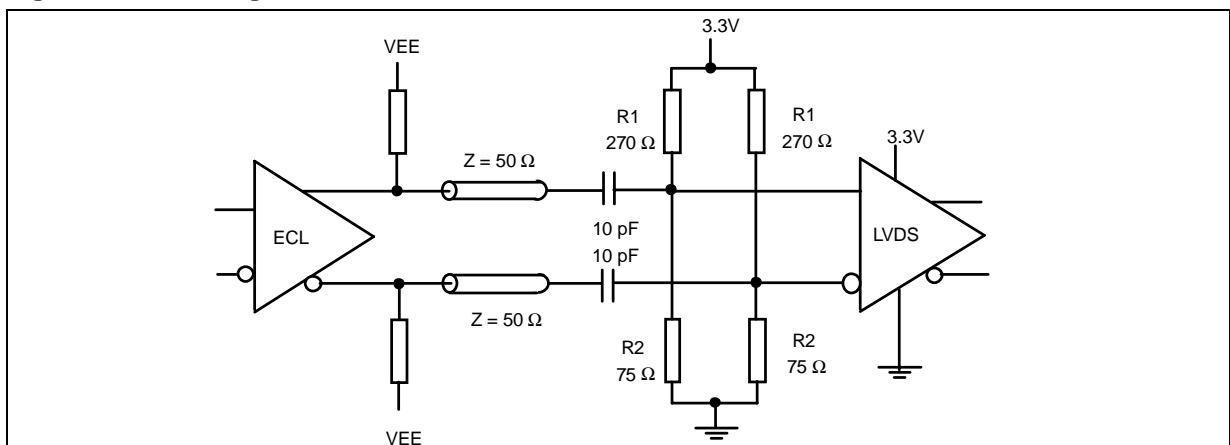
Figure 8: Interfacing LVDS to PECL/LVPECL Using the MC100(LV)EL17 device



### 9. INTERFACING ECL TO LVDS.

The ECC output requires a DC path to VEE. The pull down resistors are connected to VEE. The Thevenin resistor pair represents the termination of the transmission line Z ( $R1 \parallel R2$ ). For example,  $R1=270\Omega$  and  $R2=75\Omega$  making a parallel of  $50\Omega$  and generates a DC level of 1.2V in the static entry point of the LVDS circuitry.

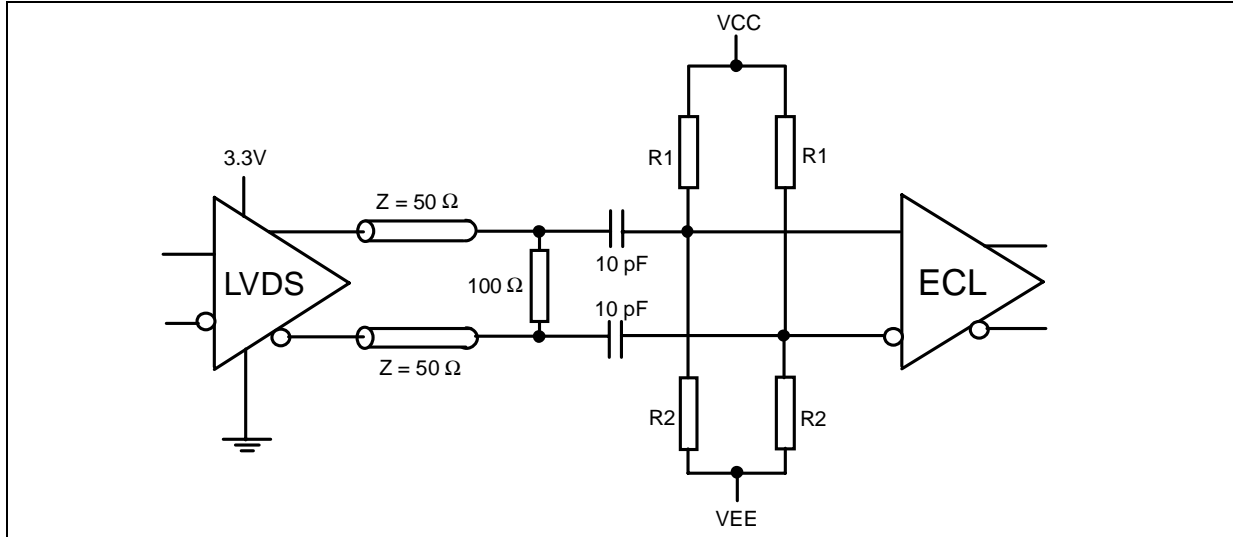
Figure 9: Interfacing ECL to LVDS



Note: In the board layout both parallel resistor terminations should be located as close as possible to the coupling capacitors.

**10. INTERFACING LVDS TO ECL.**

**Figure 10: Interfacing LVDS to ECL**



DC voltage can be generated with a resistor divider depending on the VCC value.

Examples:  $VCC=GND$  and  $VEE=-5V \Rightarrow R1=1.2k\Omega$  and  $R2=3.4k\Omega$   
 $VCC=GND$  and  $VEE=-3.3V \Rightarrow R1=680\Omega$  and  $R2=1k\Omega$

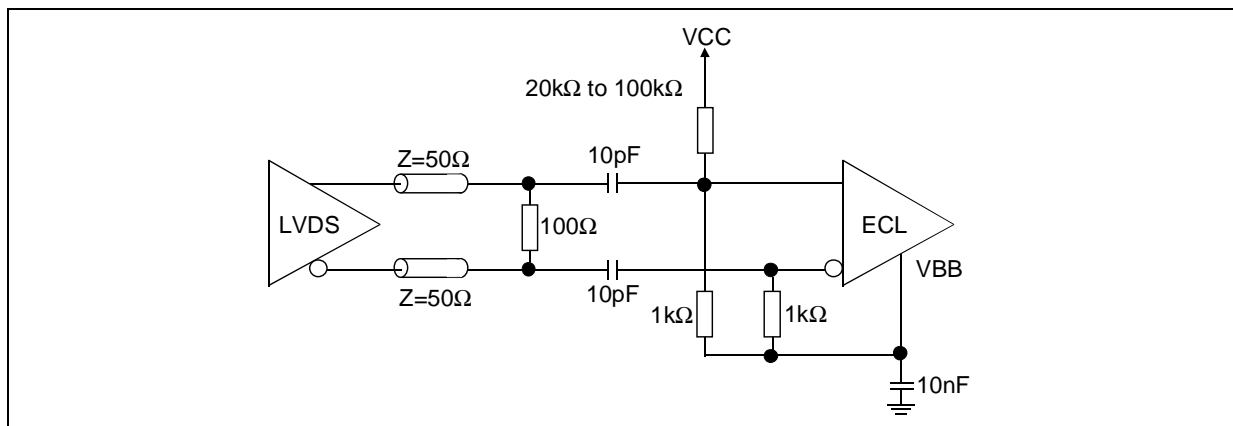
Note: In the board layout for both interfaces the resistors and capacitors should be located as close as possible to the ECL input.

**11. CAPACITIVE COUPLING LVDS TO ECL.**

Several ECL devices supply a VBB ( $VBB-VCC-1.3V$ ) reference voltage. It can be used for differential capacitive coupling.

The 100kOhm gives stable determined output states during null signal conditions.

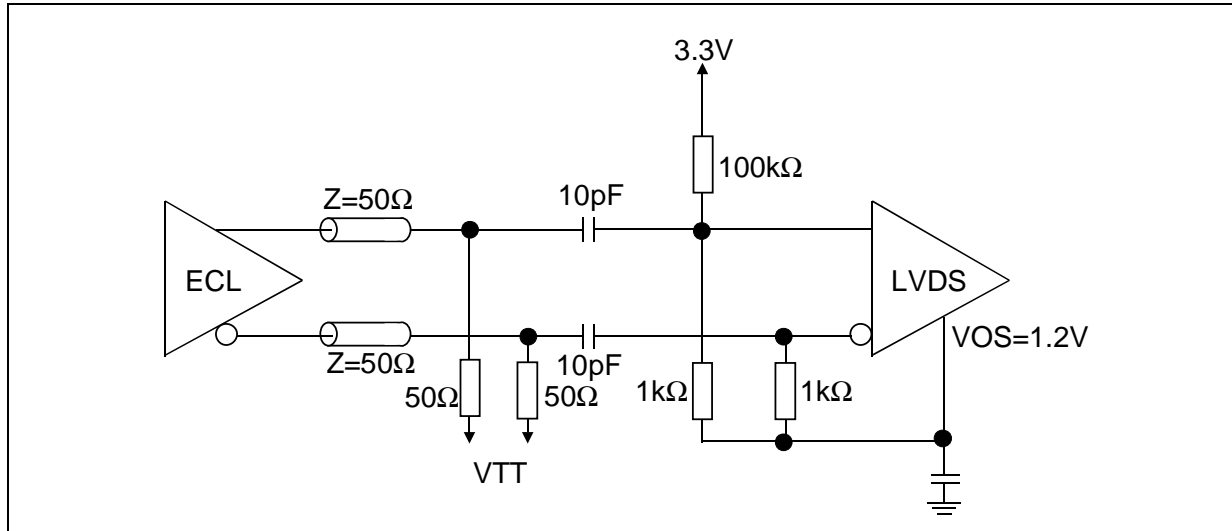
**Figure 11: Capacitive Coupling LVDS to ECL Using VBB**



**12. CAPACITIVE COUPLING ECL TO LVDS USING VOS REFERENCE VOLTAGE.**

Some devices with LVDS interfaces supply VOS reference voltage, like the STLV111. This can be used for capacitive coupling. When the transmission line length is very short, a parallel termination should be used and replaced as close as possible to the coupling capacitors.

**Figure 12: Capacitive Coupling ECL to LVDS Using VOS Reference Voltage**





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