AN-683

FAIRCHILD
SEMICONDUCTOR™

300 MHz Dual Eight-Way Multiplexer/Demultiplexer

INTRODUCTION

High speed multiplexing and demultiplexing is an integral part of the fast expanding telecommunications market, and can be used successfully in inter-computer and intra-computer wide-path communications. The Fairchild family of F100K ECL components provides an excellent solution to this design problem. This applications note describes a data transmission scheme that can transfer information at the rate of 75 Mbytes per second using only four twisted pair transmission lines.

Using 100341 8-Bit Shift Registers as parallel to serial and serial to parallel converters it is possible to design a simple mux/demux that can operate at speeds as high as 300 MHz (Figure 1). The data to be multiplexed onto the transmission lines are applied as 16 bits (2 bytes) in parallel to the inputs of the 100341s where they are loaded into the registers under control of a synchronization pulse (SYNC). The mode of the 100341s is then changed to shift right and the data is transmitted on the output lines at the clock rate. When the last bit has been shifted out, the register is loaded with the next data to be transmitted.
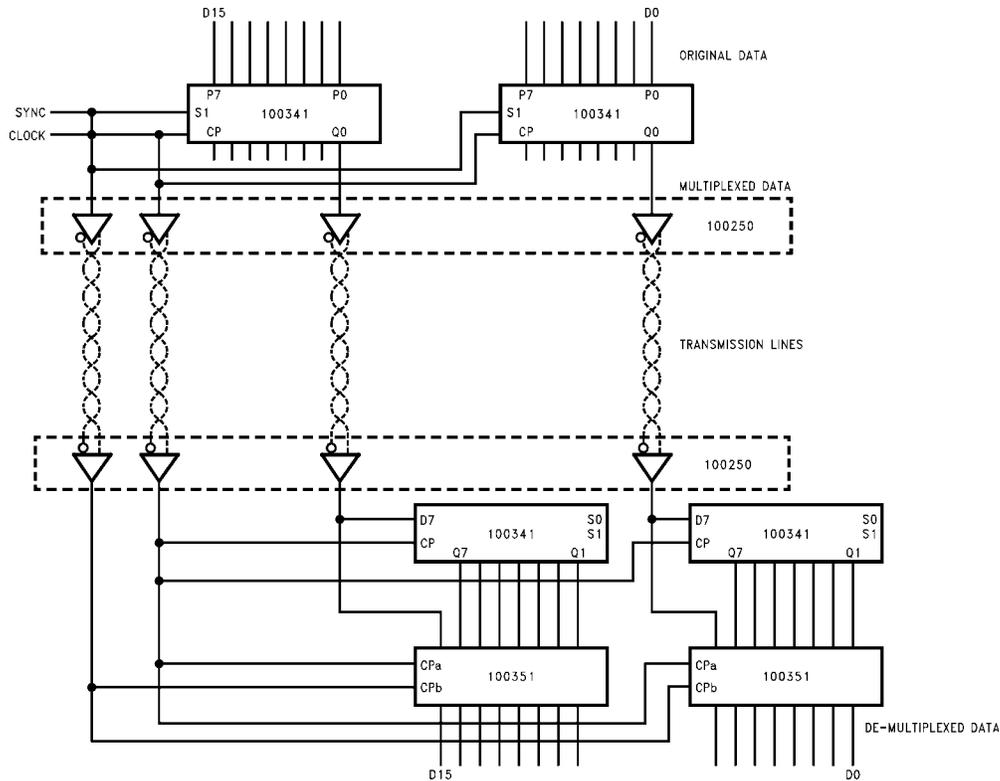

FIGURE 1. 300 MHz Dual Eight-Way Multiplexer/Demultiplexer

The clock signal (CLOCK) is a free-running 300 MHz square wave and the synchronization signal (SYNC) goes low for one clock cycle in every eight. These two signals are transmitted along with the data to facilitate synchronized reception at the other end.

At the receiving end, the 100341s are used as simple shift registers that accomplish the task of demultiplexing the data. The SYNC signal controls the loading of the 100351 receiver registers.

CLOCK AND SYNC GENERATION

The CLOCK signal in this application is a 300 MHz square wave generated with a voltage controlled oscillator coupled with a phase-locked loop. However, any available clock signal may be used at a frequency of DC to 300 MHz.

The SYNC signal is generated with the use of another 100341 connected as in Figure 2. This circuit is self start-ing, requiring no initialization for proper operation. When the SYNC signal is LOW, the data present at the parallel load inputs (P0–P7) are loaded into the register on the next clock pulse. When SYNC goes HIGH (as a result of loading the high value on P0), the mode of the 100341 is changed to shift right and the low loaded from P7 is shifted across the 100341 and appears on the SYNC wire eight cycles later. This in turn causes the 100341 to load again and the cycle repeats. The SYNC signal is HIGH for seven clock cycles and LOW for one cycle, allowing it to be used as the synchronization pulse for the mux/demux circuit.
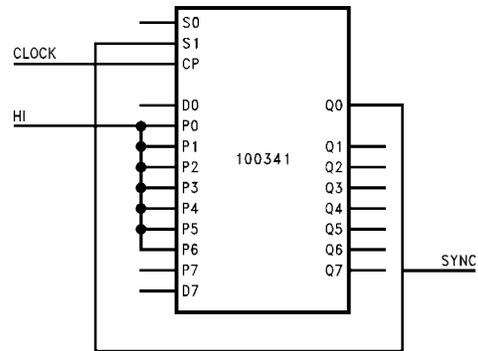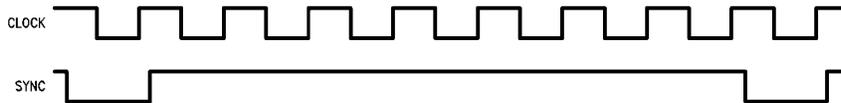
FIGURE 2. SYNC Pulse Generator

CLOCK AND SYNC WAVEFORMS

LIFE SUPPORT POLICY