EM MICROELECTRONIC-MARIN SA
A company of SMH

V 6010

LED Display Decoder / Driver

Features

- 4 digit multiplexed LED common cathode driver
- 7-segment Hex and code B decoders, pin selectable
- Decimal point and flag on each digit
- Programmable segment driver outputs 0...30mA
- Current variation across segment driver outputs typically 2%
- Fully operational from 2.4 to 6V
- −40°C to +85°C temperature range
- Low current consumption, typically 40μA
- Brightness input allows direct control of LED segment current with a single potentiometer
- Automatic blanking of leading zeros
- Device reset, display blanking, and standby facilities
- 3 wire serial data interface, data, clock and strobe
- Cascadable
- Non overlapping digit strobe
- Packages DIP28 with 1.0W dissipation and SO28 with 0.8W dissipation

Description

The V 6010 LED display driver interfaces microprocessors to 4 digit, 7 segment, common cathode, numeric LED displays. Included on chip are hexadecimal and code B decoders, multiplex scan circuitry, programmable segment drivers, and a 2 x 24 bit static memory.
The V 6010 is fully operational from 2.4 to 6V. Display brightness is controlled by a single potentiometer connected to the R_{REF} pin. Data is loaded serially as a 24 bit word into the internal shift register. A low on the $\overline{STR}$ pin parallel loads the internal 24 bit display latch with the shift register contents. The hexadecimal or code B decoder, pin selectable, decodes the 24 bit latched word, 16 bits are used for the 4 digits, and 8 bits for decimal points and flags.
The multiplex frequency is controlled by the signal applied to the CLK2 input. The digit outputs provide non overlapping drive signals to external transistors. The RESET input when active blanks the display, resets the multiplex scan circuitry, and clears the internal 24 bit display latch. When active the RESET input also puts the V 6010 into the standby mode giving a lower current consumption.

Applications

- Instrumentation readouts
- White and brown goods
- Large LED segment displays
- Alarm systems
- Panel meters and timers
- Microprocessor displays

Typical Operating Configuration

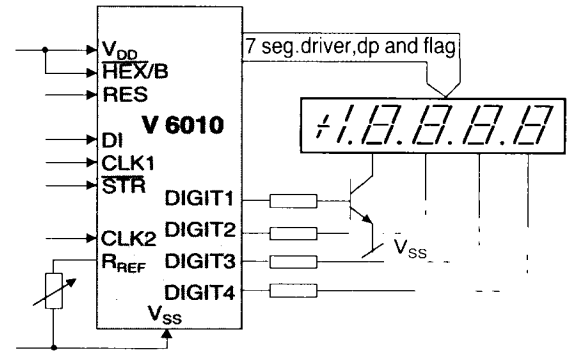

Fig. 1

Pin Assignment

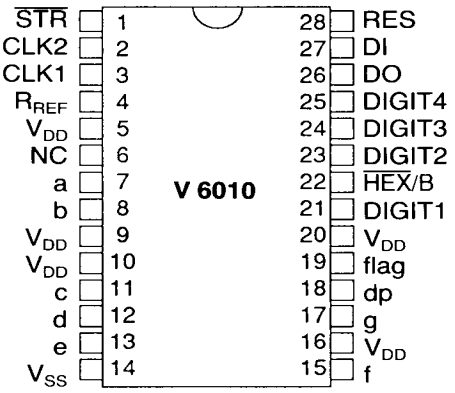

Fig. 2

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Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD} [1]	V_{max}	V_{SS} + 7.0V
Minimum voltage at V_{DD} [1]	V_{min}	V_{SS} − 0.3V
Maximum voltage at remaining pins	V_{pinmax}	V_{DD} + 0.3V
Minimum voltage at remaining pins	V_{pinmin}	V_{SS} − 0.3V
Maximum storage temperature	$T_{STOREmax}$	+125°C
Minimum storage temperature	$T_{STOREmin}$	− 65°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{STTmax}	1000V
Maximum segment output current	I_{SEG}	100mA
Maximum power dissipation [2]		
DIP28	P_{max}	1.3W
SO28	P_{max}	1.0W
Maximum lead temperature (10 s)	T_{SOLDER}	250°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_A	−40		+85	°C
Supply voltage [1] [3]	V_{DD}	2.4	5.0	6.0	V
O/P LED segment current [4]	I_{SEG}	0	20	30	mA
Power dissipation [2]					
DIP28	P			1	W
SO28	P			0.8	W
Derating factor (derate above 40°C)	P_{DERATE}	16			mW/°C

Table 2

Electrical Characteristics

V_{DD} = 5.0V ± 10%, V_{SS} = 0V and T_A = −40°C to +85°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply current static	I_{SS}	R_{REF} pin open, all other inputs at V_{DD}, all outputs open		30	70	μA
Supply current dynamic	I_{SS}	See note 7		40	100	μA
DI, CLK1, CLK2, RES, $\overline{STR}$, DO, DIGIT 1...4						
Input logic low	V_{IL}		0		0.8	V
Input logic high	V_{IH}		2.4		V_{DD}	V
Input leakage	I_{IN}	$V_{SS} < V_{IN} < V_{DD}$		1	100	nA
Input capacitance	C_{IN}				8	pF
Output logic low	V_{OL}	I_{OL} = 2mA			0.4	V
Output logic high	V_{OH}	I_{OH} = 2mA	2.4			V
$\overline{HEX/B}$						
Input logic low	V_{IL}				V_{SS}+0.4	V
Input logic high	V_{IH}		V_{DD}−0.4			V
R_{REF}						
Voltage at R_{REF} pin	V_{REF}			0.675		V
a, b, c, d, e, f, g, dp and flag O/Ps						
Current variation across O/Ps at 25°C	O/P_{VAR}	V_{OUT} = 2.3V, R_{REF} = 11kΩ [5]		2	6	%
Current @ R_{REF} = 22kΩ	I_a	V_{DD} = 5V, V_{OUT} = 2.3V [6]	5.6	7	8.4	mA
Current @ R_{REF} = 11kΩ	I_a	V_{DD} = 5V, V_{OUT} = 2.3V [6]	10.9	13.5	16.4	mA
		V_{DD} = 3V, V_{OUT} = 2.3V [6]	8.5	10.7	12.9	mA
Current @ R_{REF} = 5.6kΩ	I_a	V_{DD} = 5V, V_{OUT} = 2.3V [6]	20.3	25	30.5	mA

Table 3

[1] Always connect pins 5, 9, 10, 16 and 20 to V_{DD}. Functionality is guaranteed over the operating voltage range with the timings specified in Table 4 multiplied by 10. V_{IH} min. = V_{DD}−0.4 V, V_{IL} max. = V_{SS}+0.4 V.

[2] Derate above 40°C by the derating factor specified in Table 2. To achieve these package dissipation levels all packages have copper leadframes.

[3] Connect a minimum of 0.1μF between V_{DD} and V_{SS}. This capacitor should be placed in close proximity to the V 6010 to reduce the power supply disturbance caused by the 140mA (typical) multiplexed LED display drive current.

[4] The limits refer to the LED segment outputs a, b, c, d, e, f, g, dp, and flag. See also section "Programming LED Segment Current".

[5] V_{OUT} = V_{LED}. V_{LED} is the LED forward voltage. R_{REF} is the external resistor connected between pin R_{REF} and V_{SS} (see Fig. 1). The percentage value given is based on each segment being active one at a time and is with respect to the largest current measured. It implies that all the LED segment outputs are within typically 2% of the largest value measured.

[6] LED O/P segment "a" only is measured (see also Fig. 8, 9 10 and 11), all other outputs unloaded, V_{OUT} = LED forward voltage.

[7] RES @ V_{SS}, CKL2 = 300Hz, R_{REF} open, all outputs open, all other inputs @ V_{DD}.

Timing Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V and T_A = −40°C to +85°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		500			ns
Clock low pulse width	t_{CL}		500			ns
Clock rise and fall times[1]	t_{CR}				200	ns
	t_{CF}				200	ns
Data input setup time	t_{DS}		250			ns
Data input hold time	t_{DH}		10			ns
Data output propagation	t_{PD}	C_{LOAD} = 50 pF	20		300	ns
$\overline{STR}$ pulse width	t_{PS}		500			ns
$\overline{STR}$ pulse delay	t_{SD}		10			ns
RES pulse width	t_{RP}		250			ns
Multiplex frequency CLK2[2]	f_{mux}			250	100k	Hz

[1] $\overline{STR}$, CLK2 and $\overline{HEX/B}$ rise and fall times are also specified by t_{CR} and t_{CF}

[2] The LED display refresh rate is at the CLK2 frequency divided by 4.

Table 4

Timing Waveforms

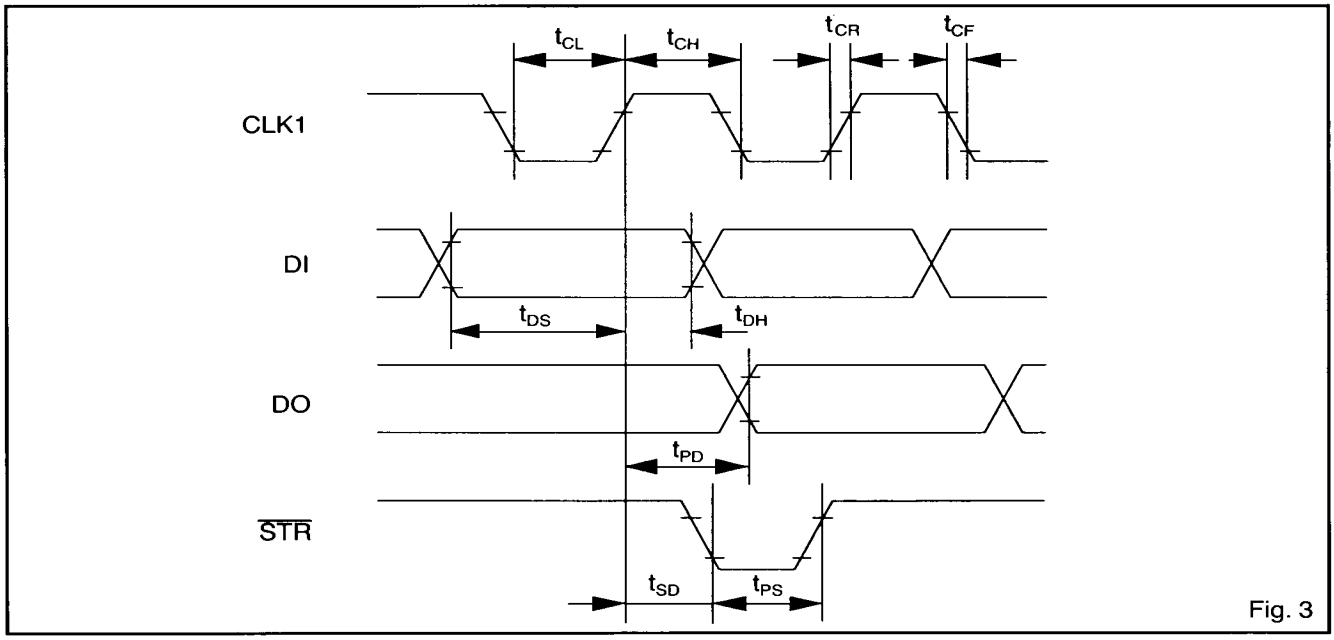
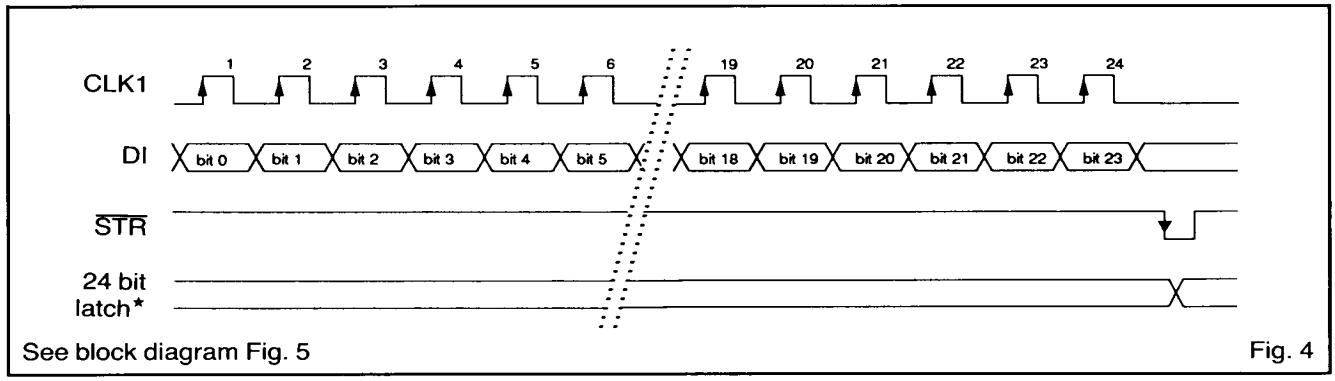


Fig. 3

Communication Cycle



See block diagram Fig. 5

Fig. 4

Block Diagram

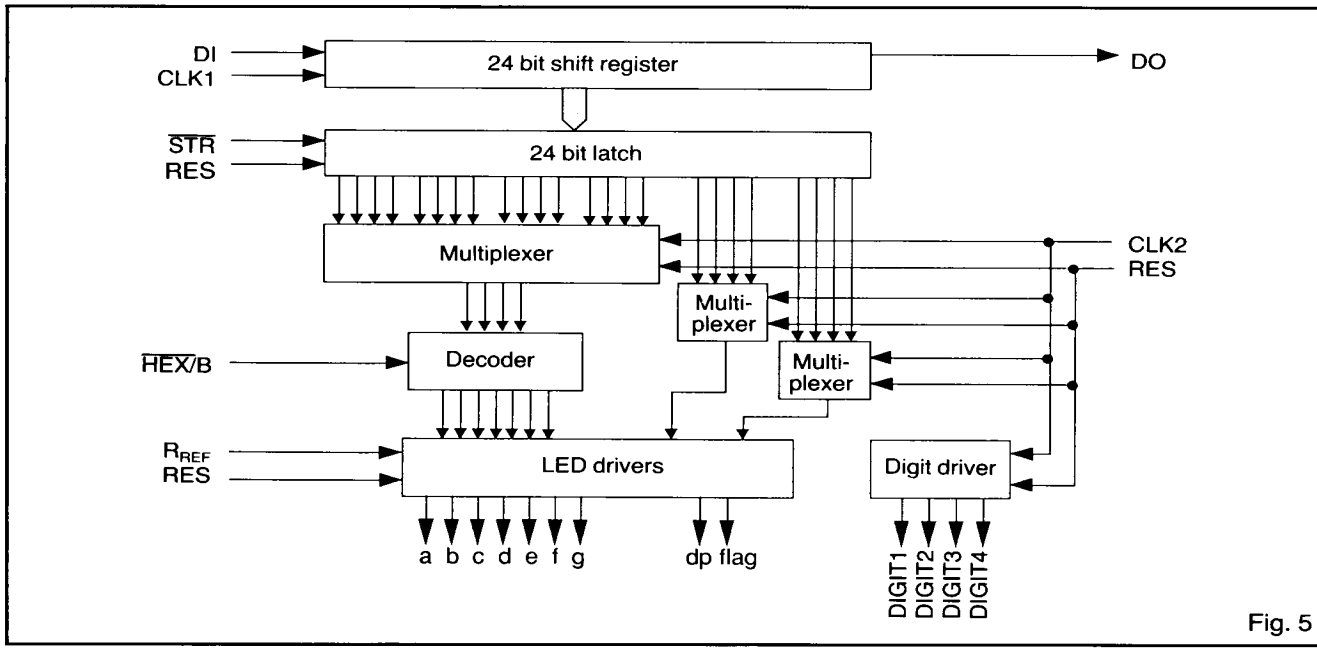


Fig. 5

Multiplex Waveforms

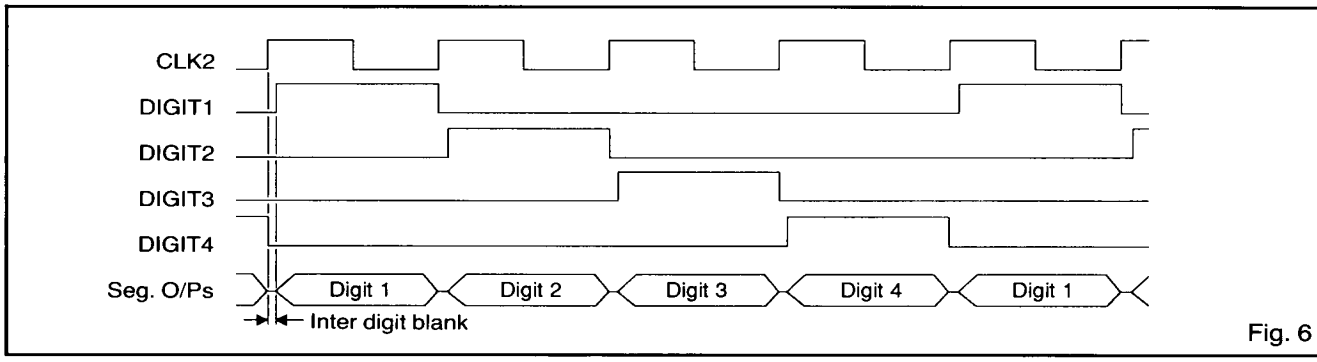


Fig. 6

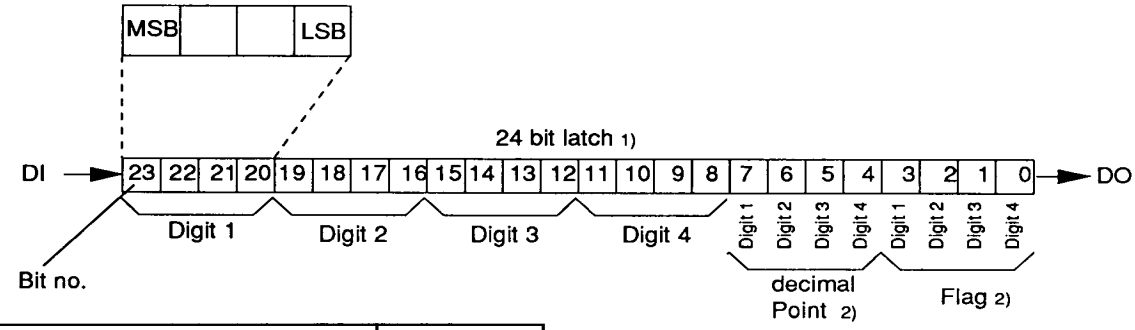
Pin Description

Pin	Name	Description
1	$\overline{STR}$	Data strobe I/P
2	CLK2	LED multiplex clock I/P
3	CLK1	Data clock I/P
4	R_{REF}	LED segment programming I/P
5	V_{DD}	Positive voltage supply for the logic
6	NC	No connection internally
7	a	LED segment O/P a
8	b	LED segment O/P b
9	V_{DD}	Positive voltage supply for LED O/Ps
10	V_{DD}	Positive voltage supply for LED O/Ps
11	c	LED segment O/P c
12	d	LED segment O/P d
13	e	LED segment O/P e
14	V_{SS}	Negative voltage supply – GND

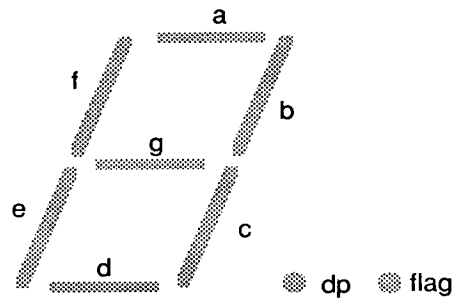
Pin	Name	Description
28	RES	Reset, display blank and standby I/P
27	DI	Data I/P
26	DO	Data O/P
25	DIGIT4	LED digit 4 O/P
24	DIGIT3	LED digit 3 O/P
23	DIGIT2	LED digit 2 O/P
22	$\overline{HEX}$/B	Hexadecimal or code B I/P
21	DIGIT1	LED digit 1 O/P
20	V_{DD}	Positive voltage supply for logic
19	Flag	LED segment O/P flag
18	dp	LED segment O/P dp
17	g	LED segment O/P g
16	V_{DD}	Positive voltage supply for LED O/Ps
15	f	LED segment O/P f

Table 5

Data Input Format and Decoding



					Display	
Digit 1 ◆	Bit 23	Bit 22	Bit 21	Bit 20		
Digit 2 ◆	Bit 19	Bit 18	Bit 17	Bit 16		
Digit 3 ◆	Bit 15	Bit 14	Bit 13	Bit 12		
Digit 4 ◆	Bit 11	Bit 10	Bit 9	Bit 8	Code B	HEX
	(MSB)			(LSB	$\overline{\text{HEX/B}}$ high	$\overline{\text{HEX/B}}$ low
	0	0	0	0	0	0
	0	0	0	1	1	1
	0	0	1	0	2	2
	0	0	1	1	3	3
	0	1	0	0	4	4
	0	1	0	1	5	5
	0	1	1	0	6	6
	0	1	1	1	7	7
	1	0	0	0	8	8
	1	0	0	1	9	9
	1	0	1	0	-	A
	1	0	1	1	E	B
	1	1	0	0	H	C
	1	1	0	1	L	D
	1	1	1	0	P	E
	1	1	1	1	Blank	F



1. See Communication Cycle (Fig. 4), and Block Diagram (Fig. 5).
2. The flag and decimal point bits (bit 0 to bit 3 and bit 4 to bit 7) are not decoded. A set bit corresponds to an "ON" LED segment.

Fig. 7

Typical Performance Characteristics

LED Segment Current as a Function of R_{REF}

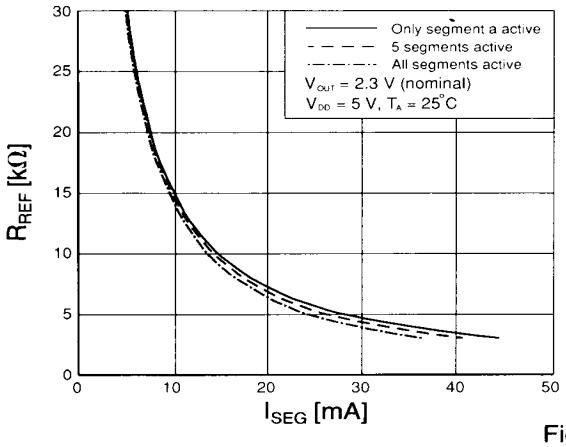


Fig. 8

LED Segment Current as a Function of V_{OUT}

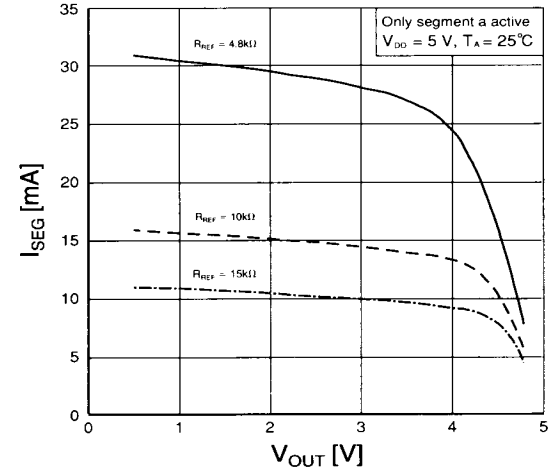


Fig. 9

LED Segment Current as a Function of V_{DD}

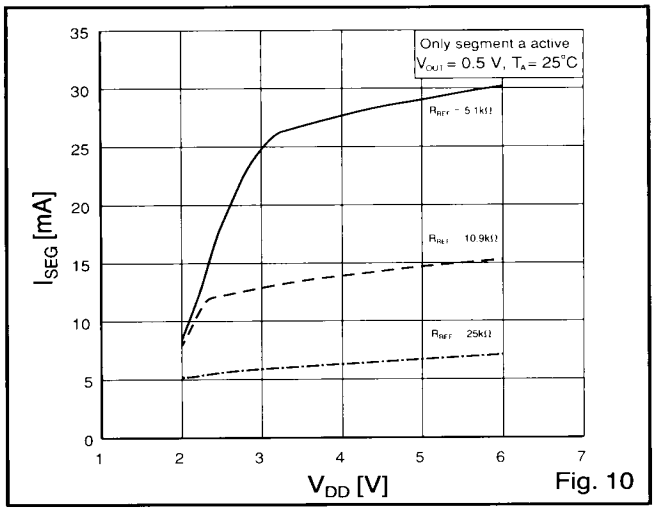


Fig. 10

LED Segment Current as a Function of Temperature

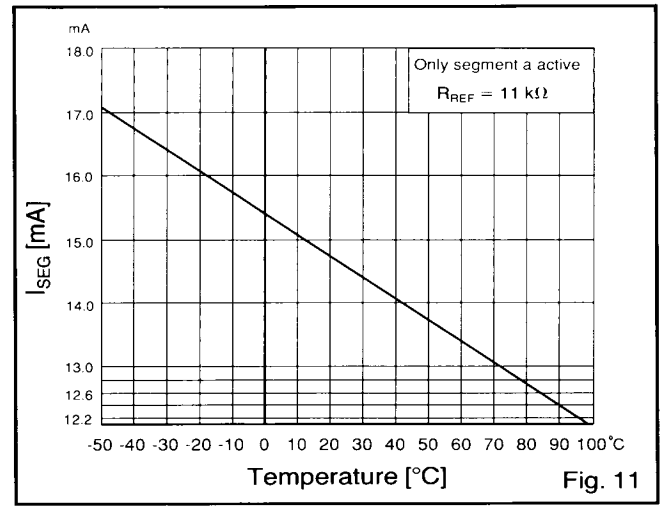


Fig. 11

Functional Description

Supply Voltages V_{DD} and V_{SS}

The V 6010 is powered by the voltage between the V_{DD} pins and the V_{SS} pin. V_{DD} pins 5 and 20 are the positive voltage supply for the logic and interface and V_{DD} pins 9, 10 and 16 are the positive voltage supply for the LED segment outputs. Connect the supply voltage to all the V_{DD} pins (5, 9, 10, 16 and 20) to ensure correct operation. A capacitor (minimum 0.1 μF) must be connected to V_{DD} and V_{SS}, in close proximity to the V 6010, to reduce power supply disturbance caused by the 140mA (typical) multiplexed LED display drive current (see Fig. 13 and 14). The V 6010 is operational from 2.4 to 6V. If the V 6010 is operated at high temperatures (> 40°C), the power dissipation within the V 6010 will need to be reduced to prevent excessive chip temperatures. The maximum power dissipation and the derating factor above 40°C is given in Table 2. Power dissipation for the device is given by:

$$P = (V_{DD} - V_{OUT})\ (I_{SEG})\ (n_{SEG})$$

where

P is the power dissipation,
V_{OUT} is the LED display forward voltage drop,
I_{SEG} is the programmed LED segment current,
n_{SEG} is the average number of "ON" LED segments.

If the V 6010 is to be used above 40°C then the programmed LED segment current must respect the maximum power rating for the highest operating temperature likely to be encountered in the application (see section "R_{REF} and the LED Segment Outputs").

Data Input/Output

The V 6010 is loaded with serial data via the input pin DI. The serial data word length is 24 bits. Data is loaded in numerical order with the data for bit 0 loaded first and the data for bit 23 last (see Fig. 4 and Fig. 7). The flag data bits (bit 0 to 3) are loaded first, followed by the decimal point bits (bits 4 to 7), the digit 4 bits (bits 8 to 11), the digit 3 bits (bits 12 to 15), the digit 2 bits (bits 16 to 19) and lastly the digit 1 bits (bits 20 to 23) (see Fig. 7). The data is clocked in at a rate determined by the clock 1 input frequency (CLK1) (see Fig. 4). The data output pin DO is used in cascaded applications (see Fig. 12). To the microprocessor, cascaded V 6010s act as one device. The data present at the V 6010's DO pin is the data loaded at the DI pin delayed by 24 clock periods. In order to cascade devices, DO of one chip must be connected to DI of the following chip (see Fig. 12).

CLK1 Input

The CLK1 input is used as the data clock and loads the serial input data on the DI pin into the V 6010's 24 bit shift register (see Fig. 5). Loading, shifting and outputting (via the DO pin) of the serial data occurs at the rising edge of the CLK1 signal. When cascading devices, all clock lines must be tied together (see Fig. 12).

CLK2 Input and the Digit Outputs

CLK2 is the LED display multiplex clock input. Fig. 6 shows how the CLK2 input is used to provide 4 non overlapping pulses to the 4 digit driver outputs, DIGIT1, DIGIT2, DIGIT3, and DIGIT4. DIGIT1 is the most significant digit on the display and DIGIT4 is the least significant digit (see Fig. 1).

The CLK2 signal is divided by 4 internally and an inter digit blank is introduced to ensure that the drive pulses to the digit outputs do not overlap causing display ghosting (see Fig. 6). For a display refresh rate of 50Hz the CLK2 frequency must be 200Hz.

It is recommended that data transfer to the V 6010 should be synchronized to the CLK2 signal to avoid a rising edge on the CLK2 input while writing data to the V 6010. On the rising edge of the CLK2 signal the active digit driver output is turned off and after the inter digit blank time (typically < 1μs) the next digit driver output is taken active. Typically the digit current is 140mA and so some power supply disturbance may be experienced when switching one digit off and another on. If the supply

lines to the V 6010 have a high impedance then voltage spikes will appear when switching. These voltage spikes could interfere with data loading on the DI and CLK1 pins. Data transfer to the V 6010 should be synchronized to the falling edge of the CLK2 signal and should be finished prior to the following rising edge (see Fig. 6 and Fig. 13).

Strobe Input

A falling edge on the $\overline{STR}$ input transfers the data contained in the 24 bit shift register to the 24 bit latch (see Fig. 4 and Fig. 5). The 24 bit latch remains open while $\overline{STR}$ is at logic "0" and the 24 bit latch is driven by the data in the 24 bit shift register. On the $\overline{STR}$ rising edge the 24 bit shift register is disabled from driving the 24 bit latch. The data held in the 24 bit latch is decoded to drive the LED display (see Fig. 7). When cascading devices the $\overline{STR}$ lines must be connected together (see Fig. 12).

Reset / Display Blanking / and Standby

The RES input when active blanks the display, resets the multiplex scan circuitry, clears the 24 bit latch and puts the V 6010 into standby (see Fig. 5). The current consumption when RES is active is typically 30μA without R_{REF} connected. The voltage at pin R_{REF} is typically 0.675V. When a resistor is connected to pin R_{REF}, a reference current will flow through the resistor in proportion to the voltage drop. This current must be added to the static current consumption to give the value for standby. On taking RES inactive the display will show "0" for digit 4 and the remaining digits will be blank. The multiplex scan circuitry will also be re-enabled. Note when RES is active it is still possible to load data into the 24 bit shift register, but it is not possible to transfer this data to the 24 bit latch.

R_{REF} and the LED Segment Outputs

The LED segment outputs on the V 6010 (pins a, b, c, d, e, f, g, dp and flag) are programmable current sources. The current source level, for all of the LED segment outputs, is programmed by a single resistor connected between pin R_{REF} and V_{SS} and has the range 0 to 30mA. The LED segment current source level is a function of the R_{REF} resistor, the output voltage (the LED forward voltage), and the voltage supply magnitude, as shown in Fig. 8, 9 and 10. The output voltage of an LED segment output is the forward voltage of the LED display, refer to the LED display's data sheet. A display brightness control can be implemented with a single potentiometer connected between pin R_{REF} and V_{SS} (see Fig. 1). The voltage at pin R_{REF} is typically 0.675V. When a resistor is connected to pin R_{REF}, a reference current will flow through the resistor in proportion to the voltage drop.

Segment, Decimal Point and Flag Decoding

The V 6010 has a data word length of 24 bits. Once the data in the 24 bit shift register is transferred to the 24 bit latch, it is decoded and used to drive the display. The V 6010 has two decoders and the selection of decoder is made via the $\overline{HEX}$/B input pin. Hexadecimal decoding is enabled when the $\overline{HEX}$/B pin is low and code B decoding when high. Fig. 7 shows how the data in the 24 bit latch is decoded depending on the status of the $\overline{HEX}$/B pin. The flag and decimal point bits (bits 0 to 3 and bits 4 to 7) are not decoded. A set flag or decimal point bit corresponds to an "ON" LED segment. The most significant digits, that are decoded to zero, are automatically blanked, DIGIT1 is the most significant digit on the display and DIGIT4 is the least significant digit (see Fig. 1). To display "0" on a 4 digit display, load "0000" for digits 1, 2 and 3 and "0000" for digit 4, digits 1, 2 and 3 will be automatically blanked and digit 4 will display "0". When $\overline{HEX}$/B is high any digit can be blanked by loading "1111" as the digit data (see Fig. 7). In cascaded applications leading digits should be blanked by loading "1111" as the digit data and enabling the code B decoder. The LED display can also be blanked by taking the RES input active.

Power up

On power up the data in the 24 bit shift register and the 24 bit display latch are undefined. The RES input should be taken high on power up to reset the V 6010 and blank the display (see Fig. 13). On taking RES inactive the display will show "0" for digit 4 and the remaining digits will be blank.

Typical Applications

2 V6010s Cascaded to Drive 8 1/2 Digits

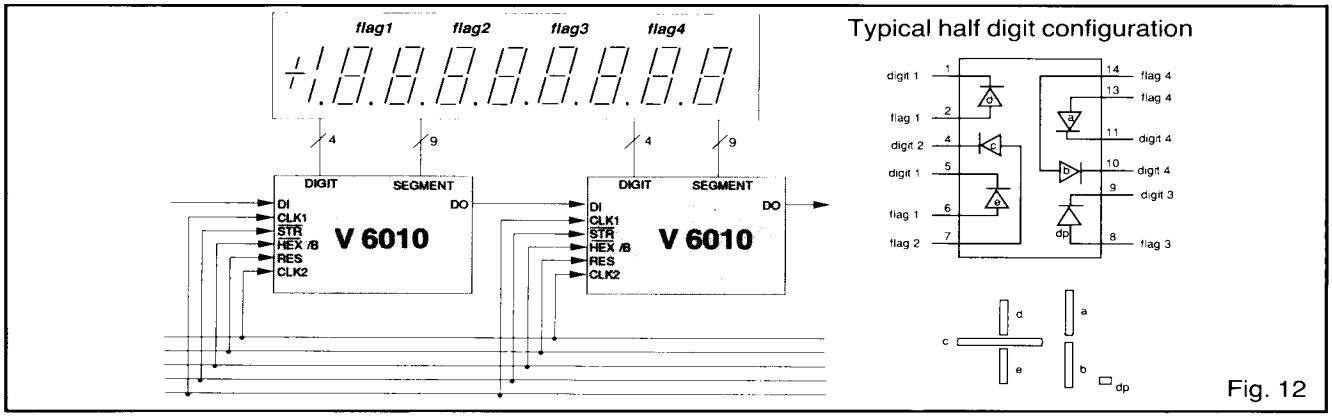
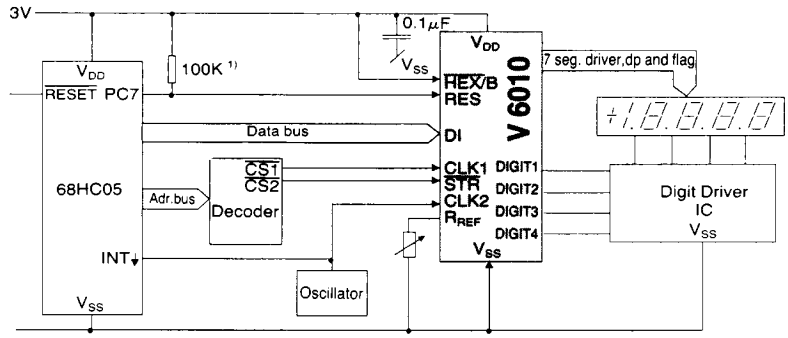


Fig. 12

V 6010 interfaced with Parallel Bus Control Lines and Data Transfer Synchronized to CLK2



1) When the microprocessor is reset, the port pin will be configured as an input and so the RES line would float. The pullup resistor will ensure that the display is blank while the system reset line is active and after until the port pin is setup by software. The RES input can also be used by software to blank the display and to hold the V 6010 in standby.

Fig. 13

V 6010 Interfaced with the Serial Peripheral Port on an 8051

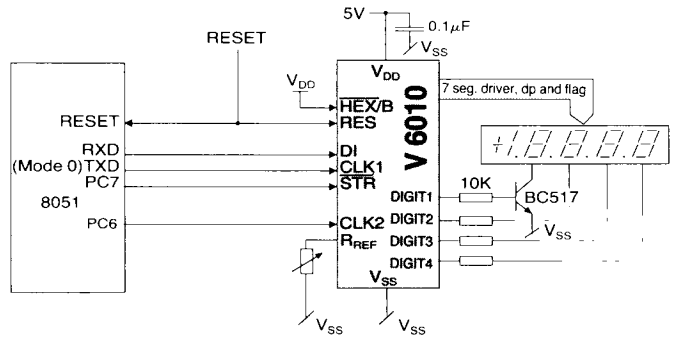
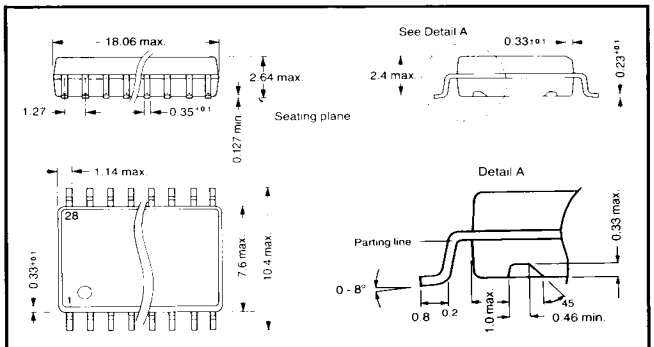


Fig. 14

Packages and Ordering Information

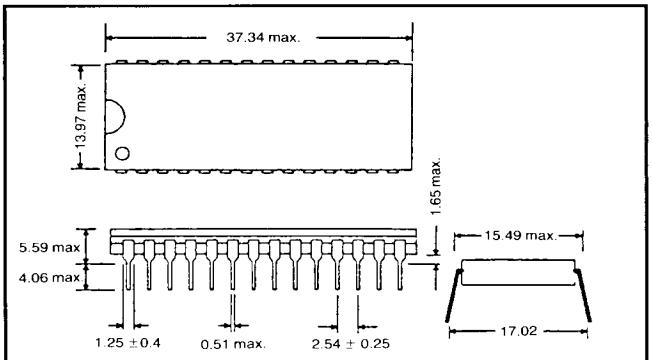
Dimensions of SO28 Package



Dimensions in mm

Fig. 15

Dimensions of DIP28 Package



Dimensions in mm

Fig. 16

Ordering Information

The V 6010 is available in the following packages:

DIP 28 pin plastic package	V 6010 28P
SO 28 pin plastic package	V 6010 28S

Chip form and others on request.
When ordering, please specify the complete part number and package.

E.&O.E. Printed in Switzerland, Th

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