SONY

CXA1875AP/AM

8-bit D/A Converter Compatible with I²C Bus

Description

The CXA1875AP/AM is developed as a 8-bit 5 ch D/A converter compatible with I²C bus.

Features

- Serial control through I²C bus
- 5 channels of 8-bit D/A converter
- 4 built-in general purpose I/O ports (Digital I/O)
- I/O can be specified to respective ports independently
- Selection of 8 slave addresses possible through address select pins (3 pins)

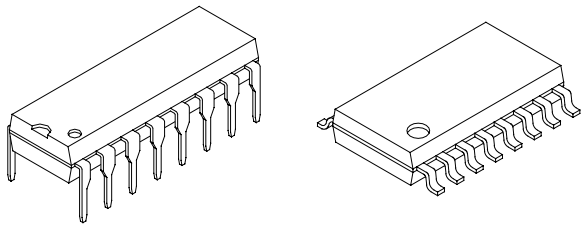
Applications

I²C bus can control ICs that do not correspond to I²C bus by connecting the DC control pins of them.

Structure

Bipolar silicon monolithic IC

16 pin DIP (Plastic) 16 pin SOP (Plastic)



Absolute Maximum Ratings (Ta=25°C)

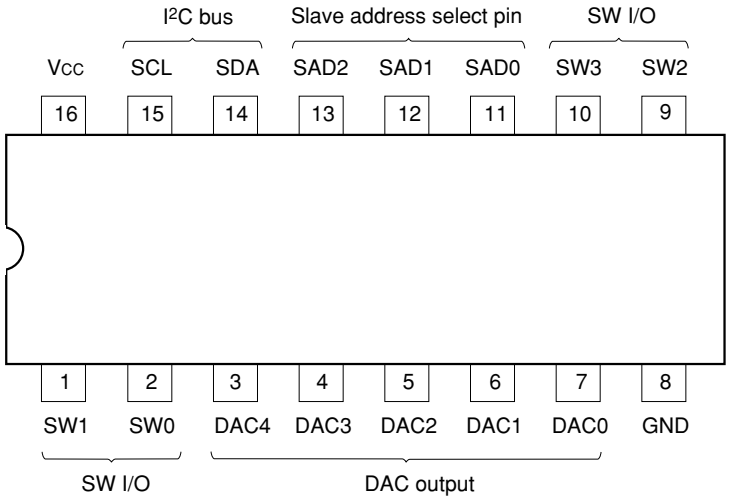
• Supply voltage	V_{CC}	7	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	960	mW

Operating Conditions

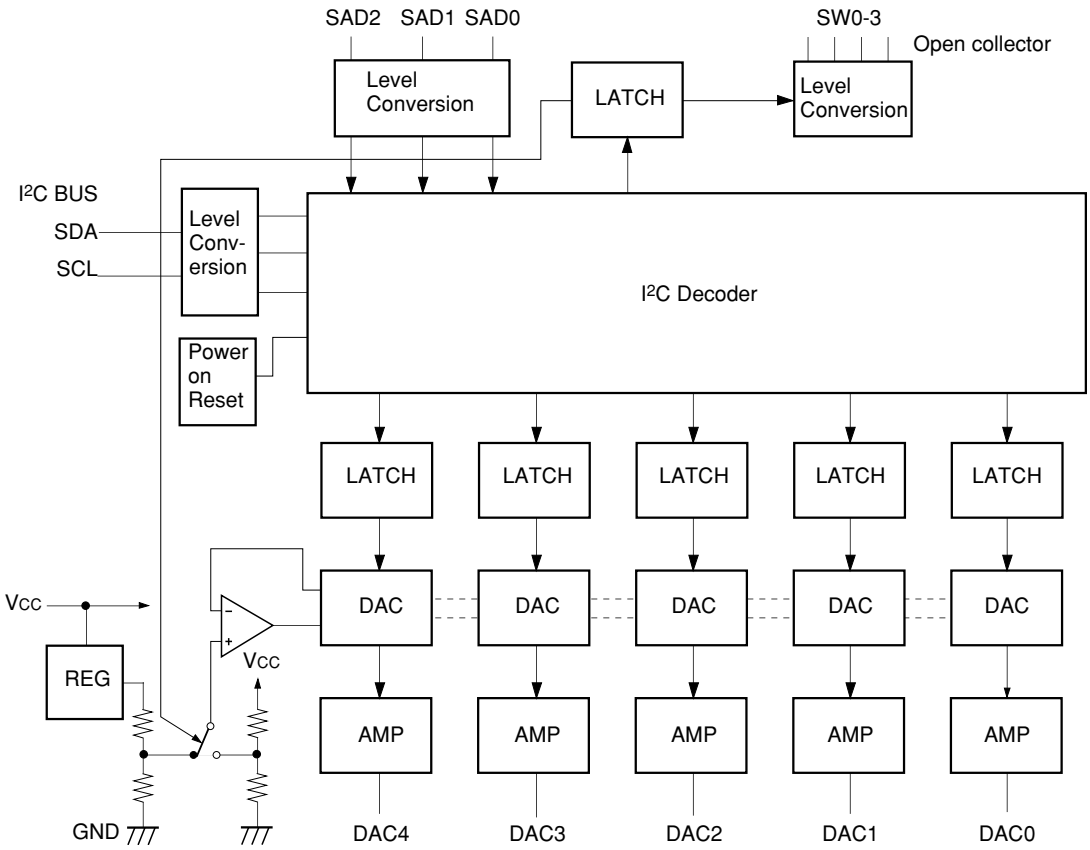
• Supply voltage	V_{CC}	5±0.5	V
• Operating temperature	Topr	–20 to +75	°C

E94X27C1Y-TE

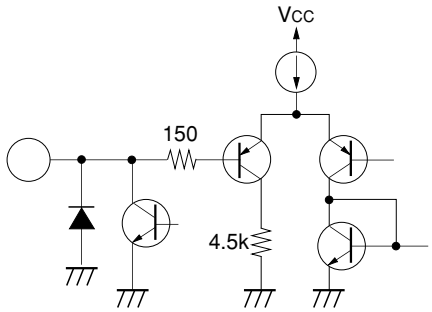
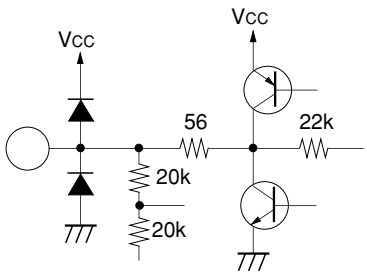
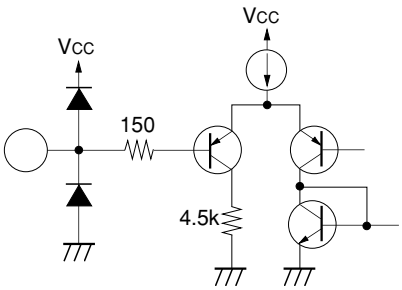
Pin Configuration (Top View)



Block Diagram



Pin Description

No.	Symbol	Equivalent circuit	Description
1 2 9 10	SW1 SW0 SW2 SW3		I/O pin for general purpose I/O port VILmax: 1.5 V VIHmin: 3 V VOLmax: 0.4 V
14 15	SDA SCL		SDA I/O pin for I²C bus
3 4 5 6 7	DAC4 DAC3 DAC2 DAC1 DAC0		D/A converter output pin
8	GND		GND pin
11 12 13	SAD0 SAD1 SAD2		Slave address input pin Input at positive logic VILmax: 1.5 V VIHmin: 3 V
16	Vcc		Power supply pin

Electrical Characteristics (Ta=25 °C, Vcc=5 V)

D/A Converter Block

No.	Item	Symbol	Test circuit	Test contents	Min.	Typ.	Max.	Unit
1	Circuit current	Icc	1	DAC 0 to 4=127	6	9	12	mA
2	Differential linearity	DLE	1	$\frac{V(DAC0\ to\ 4=n+1)-V(DAC0\ to\ 4=N)}{V(DAC0\ to\ 4=191)-V(DAC0\ to\ 4=63)}\times 128-1$ n=0 to 127	–1	0	+1	LSB
3	Minimum output voltage	Vmin	1	DAC 0 to 4=0	0.1	0.4	0.7	V
4	Maximum output voltage	Vmax	1	DAC 0 to 4=255	4.3	4.6	4.9	V
5	Output current	Iout	2	Current that can be flowed from Pins 3 to 7	–1		+1	mA
6	Output impedance	Z0	2	DAC 0 to 4=127, $\frac{V(-1\ mA)-V(1\ mA)}{2\ mA}$	0	3	6	Ω

SW, SAD Pins

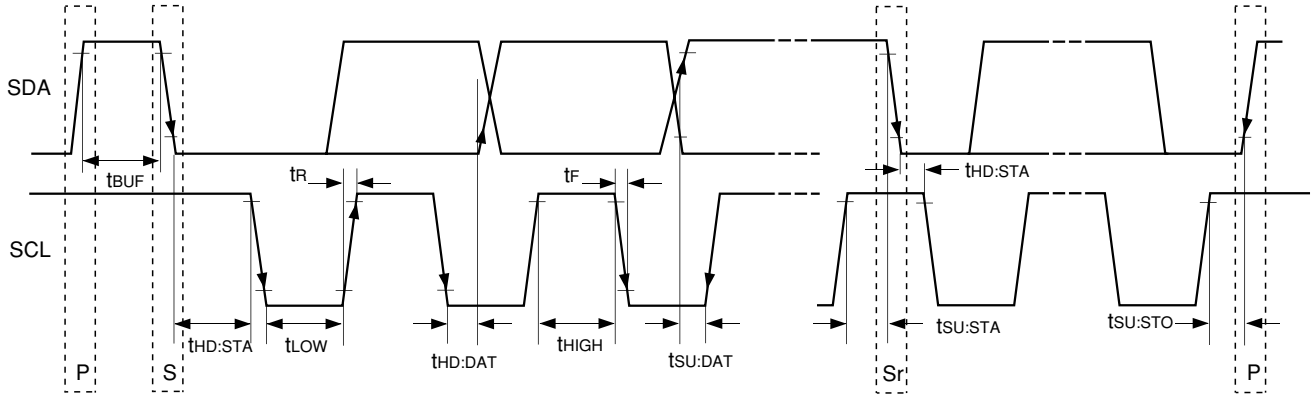
No.	Item	Symbol	Text circuit	Test contents	Min.	Typ.	Max.	Unit
7	Low level input voltage	V_{IL}	3	ST 0 to 3 an input voltage that turns to '0'	—	—	1.5	V
8	High level input voltage	V_{IH}	3	ST 0 to 3 an input voltage that turns to '1'	3.0	—	—	V
9	Low level input current	I_{IL}	3	Input current when 0.4 V is applied	–10	0	+10	µA
10	High level input current	I_{IH}	3	Input current when 4.5 V is applied	–10	0	+10	µA
11	Low level input voltage	V_{OL}	4	SW 0 to 3=1, Output voltage when 1 mA flows in	0	0.2	0.4	V

I²C Bus Block Items (SDA, SCL)

No.	Item	Symbol	Min.	Typ.	Max.	Unit
12	High level input voltage	V_{IH}	3.0	—	5.0	V
13	Low level input voltage	V_{IL}	0	—	1.5	V
14	High level input current	I_{IH}	—	—	10	µA
15	Low level input current	I_{IL}	—	—	10	µA
16	Low level output voltage At 3 mA flow to SDA (Pin 14)	V_{OL}	0	—	0.4	V
17	Maximum flowing current	I_{OL}	3	—	—	mA
18	Input capacitance	C_I	—	—	10	pF
19	Maximum clock frequency	f_{SCL}	0	—	100	kHz
20	Data change minimum waiting time	t_{BUF}	4.7	—	—	µs
21	Data transfer start minimum waiting time	$t_{HD:STA}$	4.0	—	—	µs
22	Low level clock pulse width	t_{LOW}	4.7	—	—	µs
23	High level clock pulse width	t_{HIGH}	4.0	—	—	µs
24	Minimum start preparation waiting time	$t_{SU:STA}$	4.7	—	—	µs
25	Minimum data hold time	$t_{HD:DAT}$	5	—	—	µs
26	Minimum data preparation time	$t_{SU:DAT}$	250	—	—	ns
27	Rise time	t_R	—	—	1	µs
28	Fall time	t_F	—	—	300	ns
29	Minimum stop preparation waiting time	$t_{SU:STO}$	4.7	—	—	µs

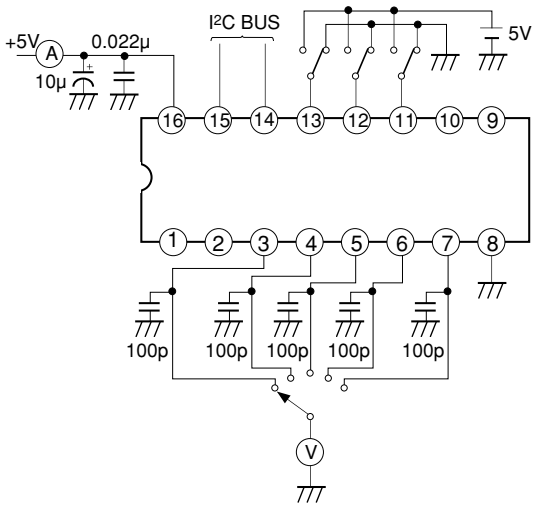
I²C bus load conditions: Pull up resistance 4 kΩ (Connected to +5 V)
Load capacitance 200 pF (Connected to GND)

I²C Bus Control Signal

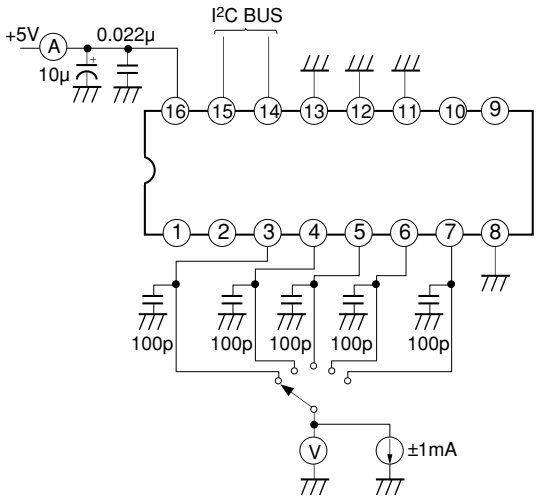


Electrical Characteristics Test Circuit

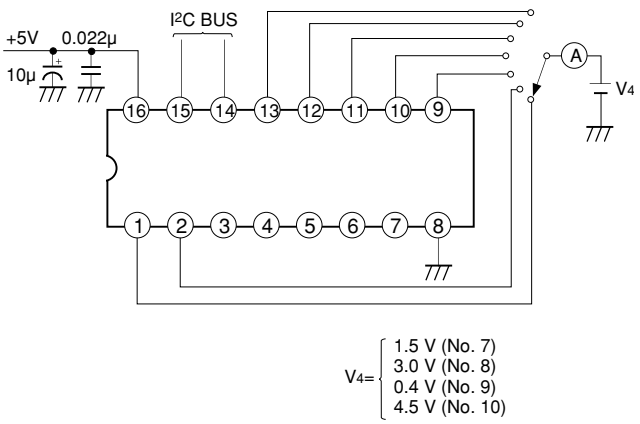
Test circuit 1



Test circuit 2

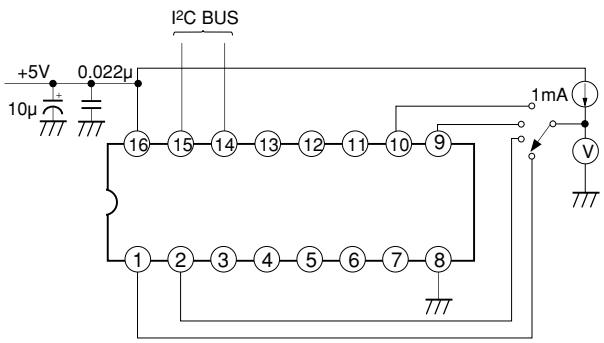


Test circuit 3



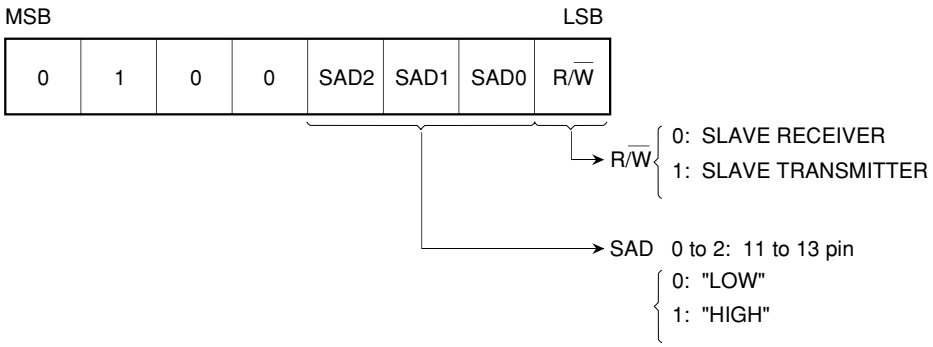
V_4= { 1.5 V (No. 7) / 3.0 V (No. 8) / 0.4 V (No. 9) / 4.5 V (No. 10) }

Test circuit 4



Definition of I²C Register

<Slave address>



<Register table>

- With the IC reset all registers are reset to 0
- ∗: Not defined
- ×: Don't care
- Sub address is auto incremented
- It can be used as a 6-bit D/A converter by setting the lower two bits of DAC 0-4 registors to 0, but take care that the max. voltage of DA output will lower about 100 mV compared with the use of 8 bits.

Control Register

Sub address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
××××× 000	REF	∗	∗	∗	SW3	SW2	SW1	SW0
××××× 001	DAC0 (8)							
××××× 010	DAC1 (8)							
××××× 011	DAC2 (8)							
××××× 100	DAC3 (8)							
××××× 101	DAC4 (8)							

Status Register

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PONRES	0	0	0	ST3	ST2	ST1	ST0

<Registers> In brackets ( ) number of bits

REF (1): Switches D/A converter reference voltage
0:Standardizes the inner regulator
1:Standardizes voltage resistance divided from V_{CC}

SW0 to 3 (1): Selects ON/OFF of Pins 1, 2, 9 and 10
(Each pin is the open collector output of NPN transistor)
0:OFF
1:ON

DAC0 to 4 (8): Digital data input register of D/A converter
0:Output voltage turns to minimum
255:Output voltage turns to maximum

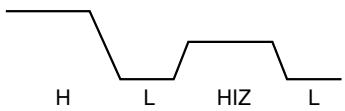
PONRES (1): Detects POWER ON RESET
0:Master passes from the bus and is reset to 0 after having read this status
1:Set to 1 when power supply is turned on or when there has been a power dip

ST0 to 3 (1): Detects and registers the voltage condition of Pins 1, 2, 9 and 10
0:1.5 V and below
1:3.0 V and above
Note) SW0 to 3 effective during 0

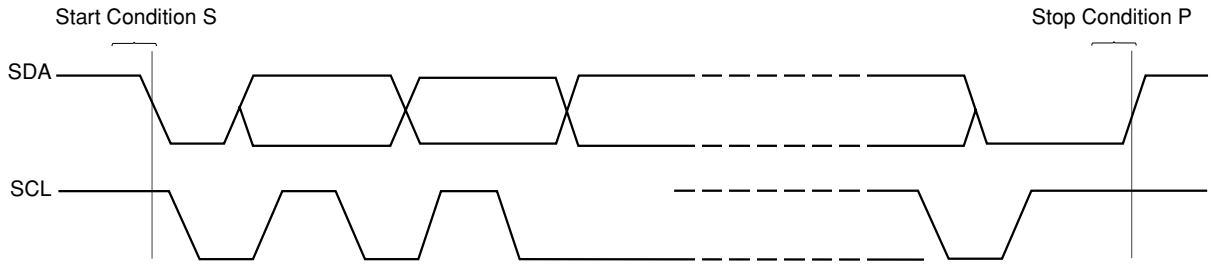
I²C Bus Signal

There are 2 signals in I²C bus. SDA (Serial DAta) and SCL (Serial Clock).
SDA is double-way.

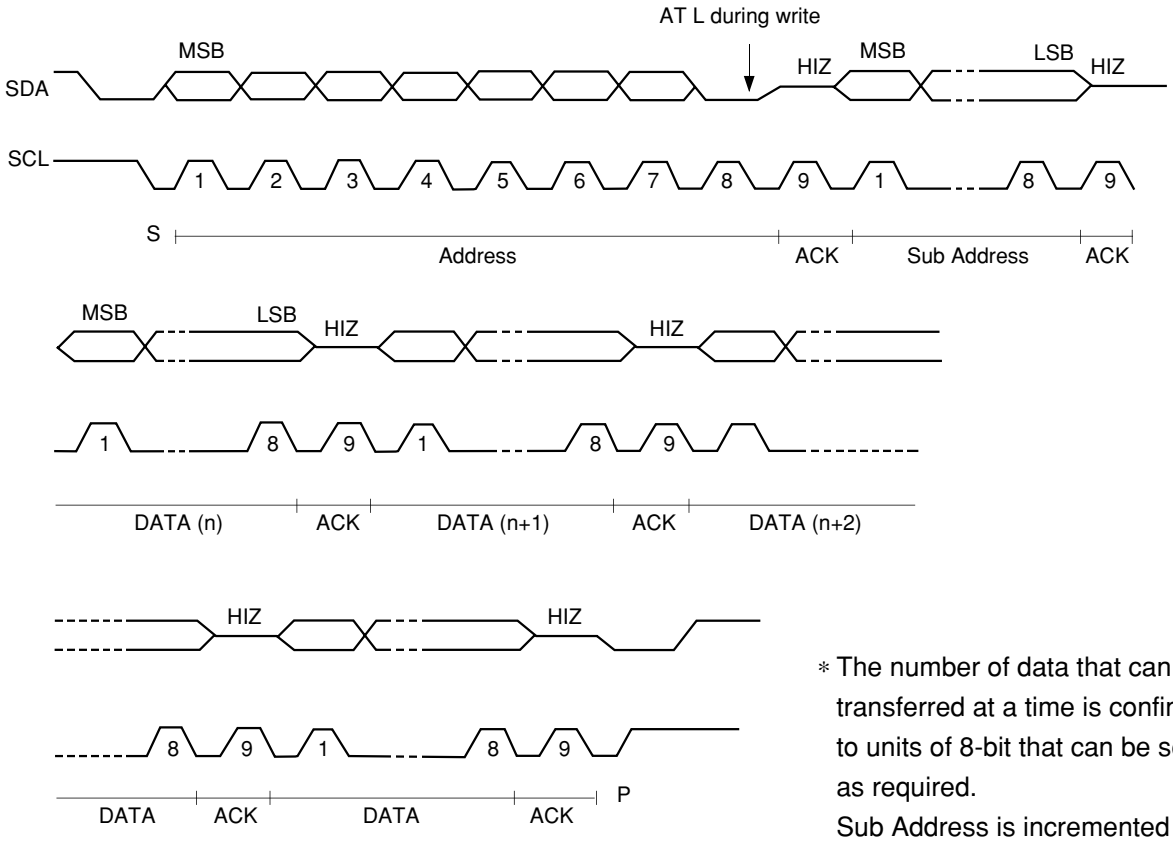
• As SDA is double-way it has 3 state outputs, H, L and HIZ.



• I²C transfer begins with Start Condition and ends with Stop Condition.

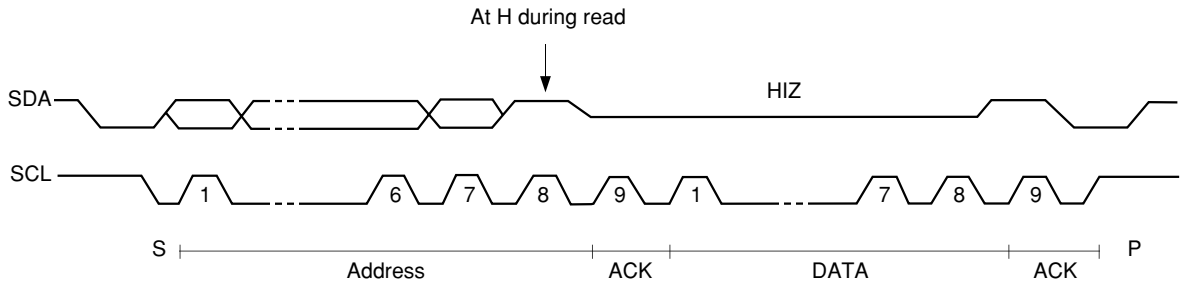


• I²C data write (Write from I²C controller to IC)

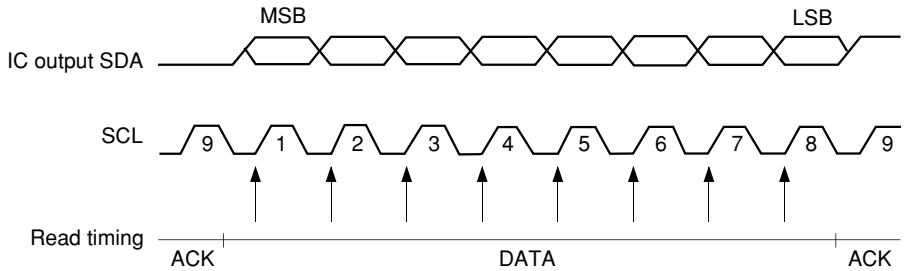


∗ The number of data that can be transferred at a time is confined to units of 8-bit that can be set as required.
Sub Address is incremented automatically.

• I²C data read (Read from IC to I²C controller)

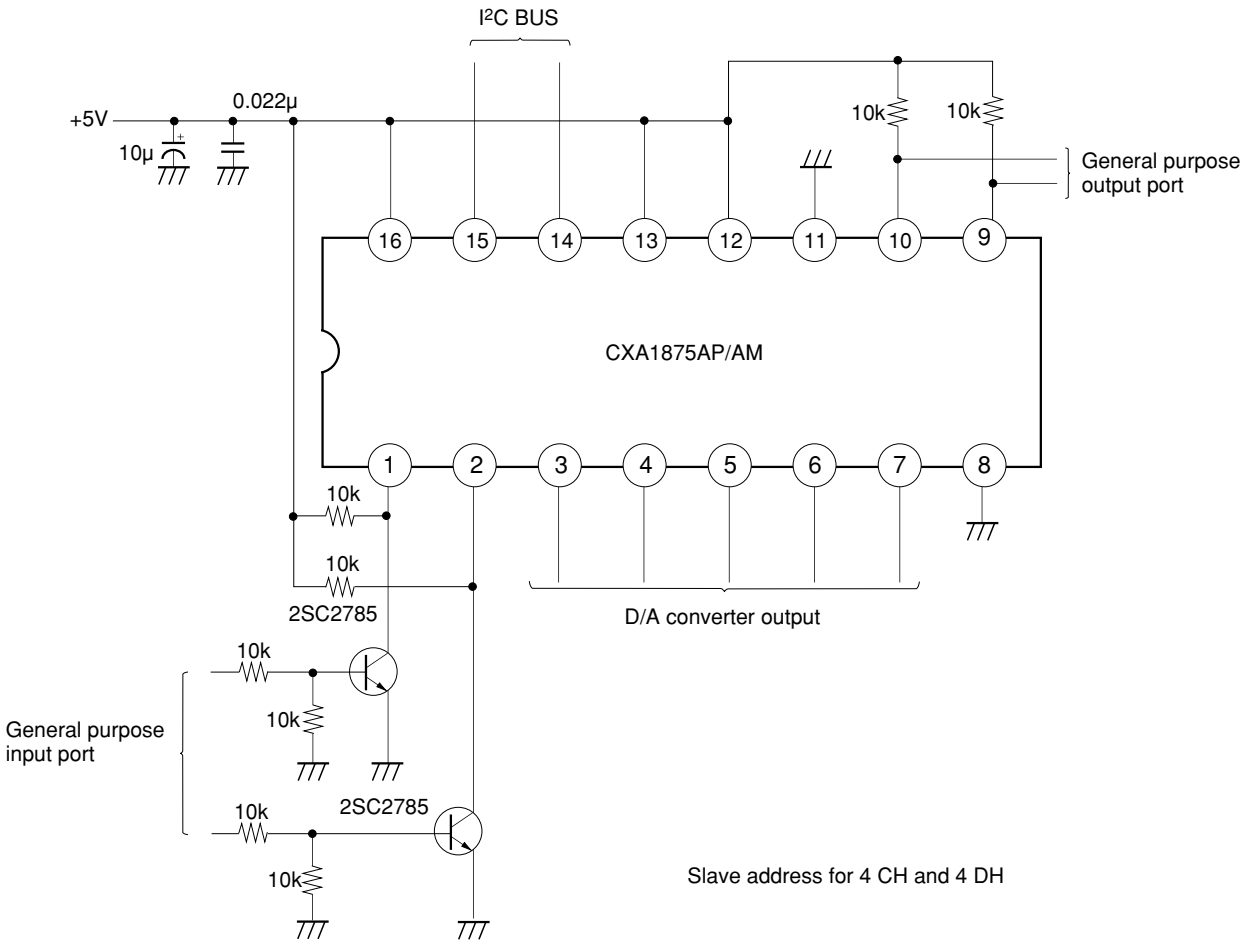


• Read timing



∗ Data read is performed with SCL rise.

Application Circuit

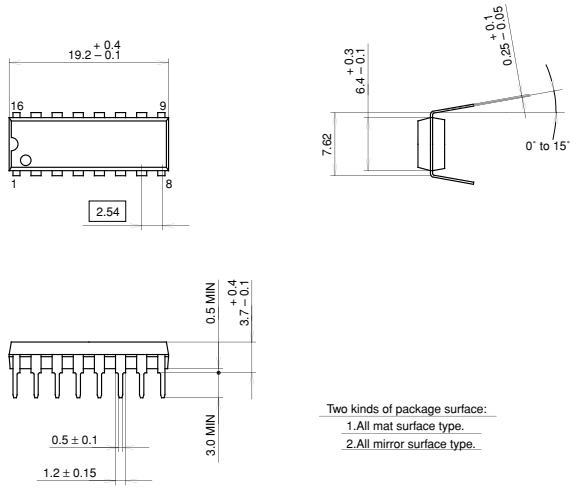


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

CXA1875AP

16PIN DIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

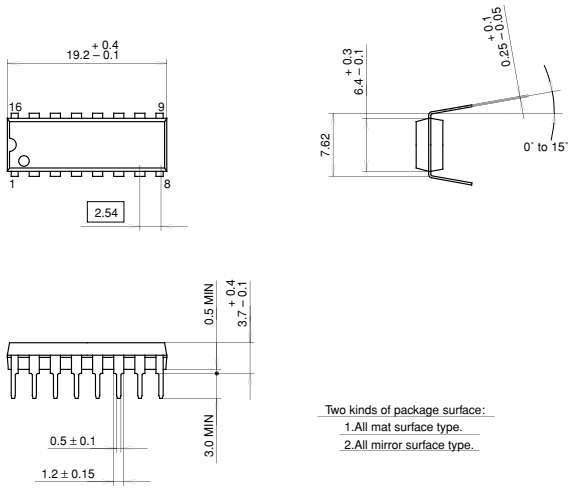
SONY CODE	DIP-16P-01
EIAJ CODE	DIP016-P-0300
JEDEC CODE	Similar to MO-001-AE

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.0 g

CXA1875AP
Kokubu Ass'y

16PIN DIP (PLASTIC)



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LEAD TREATMENT	SOLDER PLATING
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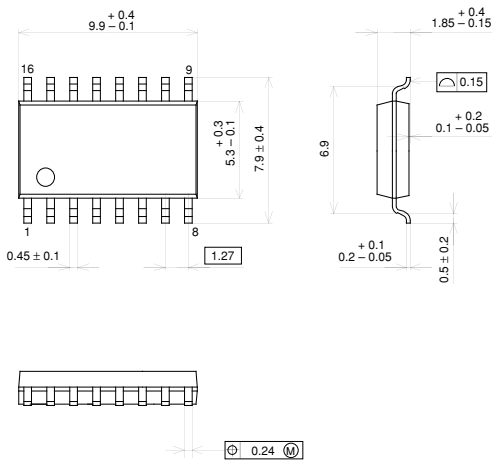
PACKAGE MASS	1.0 g

Package Outline Unit : mm

CXA1875AM

16PIN SOP (PLASTIC)



PACKAGE STRUCTURE

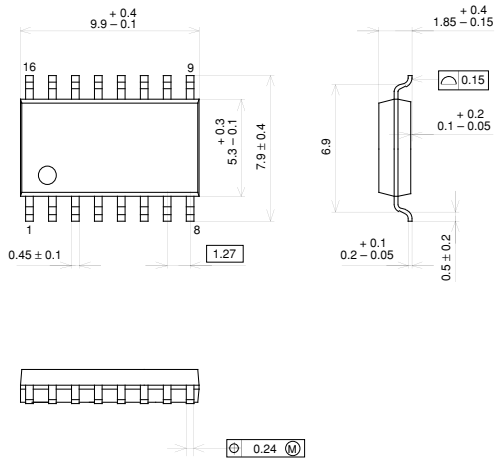
SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

CXA1875AM

SCT Ass'y

16PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm

Purchase of Sony's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.