NOV 9 1992

PRELIMINARY

Am85C230A

Enhanced Serial Communication Controller with LocalTalk™ Support (ESCC/LT)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements the following LocalTalk requirements:**
  - Generation of SYNC pulse before the SDLC opening FLAG
  - Generation of two SDLC opening FLAGs
  - Generation of an abort sequence at the end of LocalTalk packet
  - Automatic Receive Disable during Transmit
- **8-byte Receive and 4-byte (extendable to 8-byte) Transmit FIFO**
- **Retains the following Am85C30 enhancements:**
  - Deactivation of $\overline{RTS}$ pin after the SDLC ending flag
  - Automatic transmission of the SDLC beginning flag
  - Automatic reset of Tx underrun/EOM latch
  - Complete CRC reception
  - TxD pin automatically forced high in NRZI encoding mode
  - Rx FIFO unlock after special condition interrupt when Status FIFO is used
  - Write registers WR3, WR4, WR5 and WR10 being readable
  - DTR/REQ pin timing reduced
  - Faster interrupt response
  - Software interrupt acknowledge mode
  - Addition of new register WR7′
- **Plug compatible and a functional superset of Z85230**
- **Generation of 'End of Packet' DMA Request**
- **Fast data rates; up to 20 MHz/5Mb/s**
- **Sleep mode for reduced power**
- **Addition of Schmitt Trigger Circuit on Rx and Tx clock inputs**
- **Ready function added to reflect valid access recovery time (available in PLCC package only)**
- **Tx Clock divider (X16, X32 and X64) in Synchronous modes**
- **Latching of RR0 during Read Cycle**
- **Availability of the die revision ID information**
- **Available in both 40-pin DIP and 44-pin PLCC packages**

GENERAL DESCRIPTION

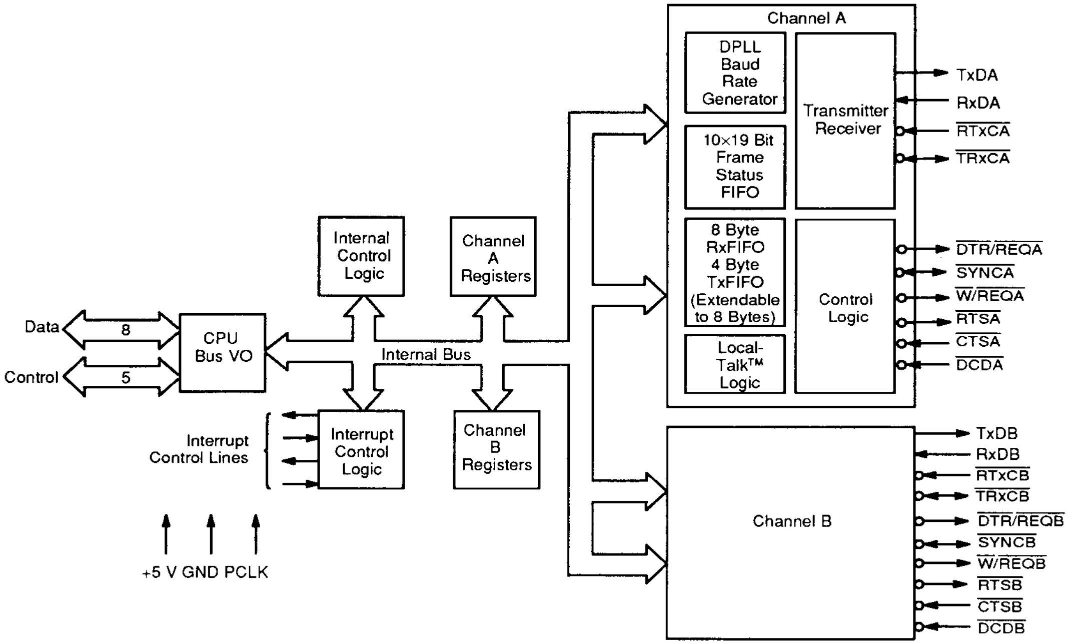
The Enhanced Serial Communications Controller with LocalTalk Support (ESCC/LT), Am85C230A is a functionally enhanced product of the original Am85C30. The Am85C230A is a dual-channel, full duplex data communications controller capable of supporting a wide range of popular protocols. The ESCC/LT retains all the SDLC/interface enhancements from the original Am85C30. It is easier to interface to popular CPUs. The Am85C230A also has faster data rate, up to 20MHz/5Mb/s.

The ESCC/LT is also pin and software compatible and a functional superset of Z85230. Enhancements to the Z85230 include, hardware implementation of Apple LocalTalk protocol, 4 deep Transmit FIFO extension to total 8-byte Rx and 8-byte Tx FIFOs, Ready signal to reflect the write recovery time, sleep mode for reduced power, and addition of Schmitt trigger circuitry on Rx and Tx clock inputs. The implementation of LocalTalk features on silicon greatly reduces the software overhead, thus improves the overall system performance.

At power up, Am85C230A will look like the Z85230. The LocalTalk enhancements, Tx FIFO extension and die revision ID can be enabled using the new WR6′ register.

Publication# 16505 Rev. B Amendment /0
Issue Date: August 1992

BLOCK DIAGRAM



16505B-1

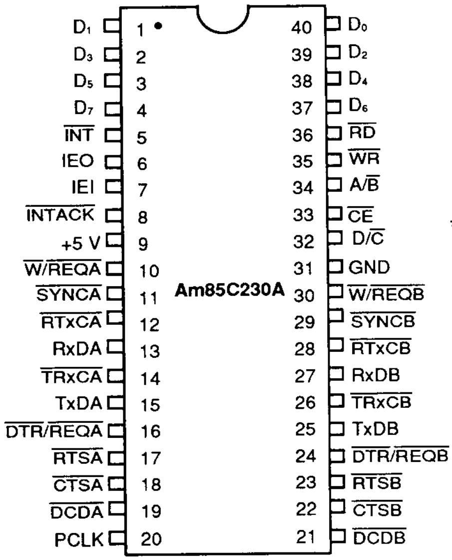
RELATED AMD PRODUCTS

Part No.	Description	Part No.	Description
7960	Coded Data Transceiver	9517A	DMA Controller
80186	Highly Integrated 16-Bit Microprocessor	53C80A	SCSI Bus Controller
80286, 80C286	High-Performance 16-Bit Microprocessor	80188	Highly Integrated 8-Bit Microprocessor
33C93A	Enhanced CMOS SCSI Bus Interface Controller	Am386™	High-Performance 32-Bit Microprocessor
53C94, 53C96	High Performance CMOS SCSI Controller	85C30	Enhanced Serial Communication Controller
26LSxx	Line drivers/receivers	85C80	Combination 53C80A SCSI and 85C30 ESCC

CONNECTION DIAGRAMS

Top View

DIP



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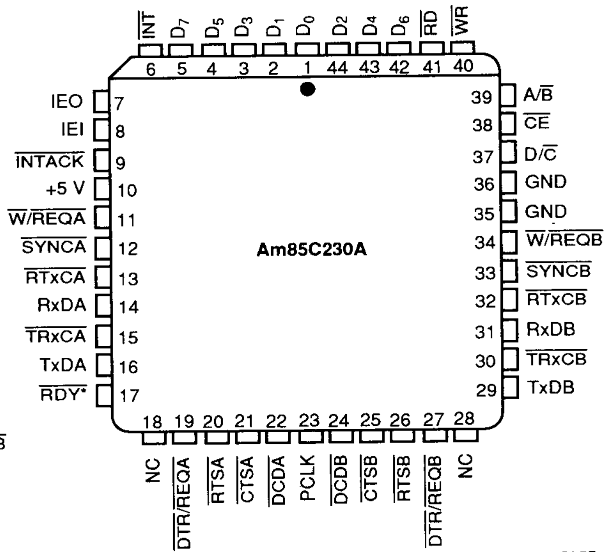
PLCC



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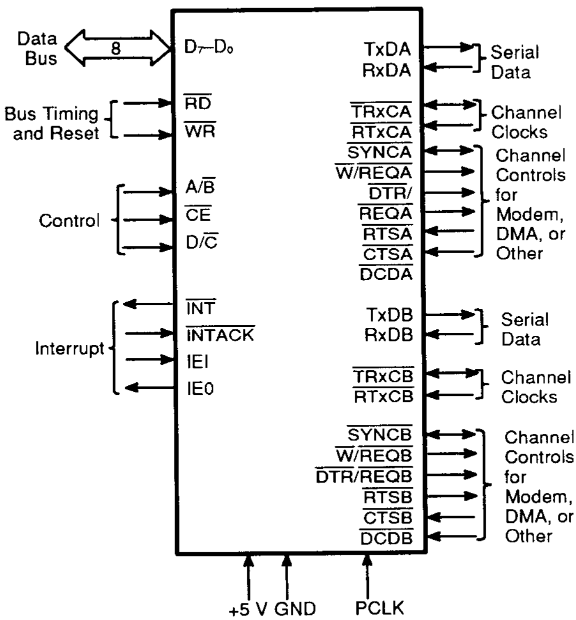
Note:
Pin 1 is marked for orientation.
*Option available in 44-pin PLCC package only

LOGIC SYMBOL



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ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM85C230A -10 P C

OPTIONAL PROCESSING
Blank = Standard Processing

TEMPERATURE RANGE
C = Commercial (0 to +70°C)

PACKAGE TYPE
P = 40-Pin Plastic DIP (PD 040)
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)

SPEED OPTION
-8 = 8.192 MHz
-10 = 10 MHz
-16 = 16.384 MHz
-20 = 20 MHz

DEVICE NUMBER/DESCRIPTION
Am85C230A
Enhanced Serial Communications Controller
with LocalTalk™ Support

Valid Combinations	
AM85C230A-8 AM85C230A-10 AM85C230A-16 AM85C230A-20	PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Bus Timing and Reset

RD
Read (Input; Active Low)

This signal indicates a Read operation and, when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.

WR
Write (Input; Active Low)

When the SCC is selected, this signal indicates a Write operation. The coincidence of RD and WR is interpreted as a reset.

RDY
Available in 44-pin PLCC package only
Ready (Output, Active Low)

RDY does active when ESCC/LT is ready for a 'Write' to one of its registers. The external CPU will have to wait for RDY to go low before it can write to one of the ESCC/LT write registers. The usage of RDY eliminates the need of using the parameter 49 for Write cycles presently specified in the ESCC (Am85C30) datasheet. If the RDY is not connected, the ESCC/LT will be pin-out compatible to 85C30.

Channel Clocks

RTxCA, RTxCB
Receive/Transmit Clocks (Inputs; Active Low)

These pins can be programmed in several different modes of operation. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock of the digital phase-locked loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

TRxCA, TRxCB
Transmit/Receive Clocks
(Inputs/Outputs; Active Low)

These pins can be programmed in several different modes of operation. TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode. Schmitt Trigger circuitry is added on these inputs to improve noise immunity.

Channel Controls for Modem, DMA, or Other

CTSA, CTSB
Clear to Send (Inputs; Active Low)

If these pins are programmed as Auto Enables, a Low on these inputs enables their respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and may interrupt the CPU on both logic level transitions.

DCDA, DCDB
Data Carrier Detect (Inputs; Active Low)

These pins function as receiver enables if they are programmed as Auto Enables; otherwise, they may be used as general-purpose input pins. Both are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and may interrupt the CPU on both logic level transitions.

DTR/REQA, DTR/REQB
Data Terminal Ready/Request
(Outputs; Active Low)

These outputs follow the inverted state programmed into the DTR bit in WR5. They can also be used as general-purpose outputs or as Request Lines for a DMA controller.

RTSA, RTSB
Request to Send (Outputs; Active Low)

When the Request to Send (RTS) bit in Write Register 5 is set, the RTS signal goes Low. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In SYNC mode, or in asynchronous mode with Auto Enable off, the RTS pins strictly follow the inverted state of the RTS bit. Both pins can be used as general-purpose outputs.

In SDLC mode, the AUTO RTS RESET enhancement described later in this document brings RTS High after the last 0 of the closing flag leaves the TxD pin.

SYNCA, SYNCB
Synchronization (Inputs/Outputs; Active Low)

These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to CTS and DCD. In this mode, transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, SYNC must be driven Low two receive clock cycles after the last bit in the SYNC character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of SYNC.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which SYNC characters are recognized. The SYNC condition is not latched, so these outputs are active each time a SYNC pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

$\overline{W/REQA}$, $\overline{W/REQB}$
Wait/Request (Outputs; Open drain when programmed for a Wait function, driven High or Low when programmed for a Request function)

These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

Control

A/$\overline{B}$
Channel A/Channel B Select (Input)

This signal selects the channel in which the Read or Write operation occurs.

$\overline{CE}$
Chip Enable (Input; Active Low)

This signal selects the SCC for a Read or Write operation.

D/$\overline{C}$
Data/Control Select (Input)

This signal defines the type of information transferred to or from the SCC. A High means data is transferred; a Low indicates a command is transferred.

Data Bus

D_7–D_0
Data Bus (Input/Output; Three State)

These lines carry data and commands to and from the SCC.

Interrupt

IEI
Interrupt Enable In (Input; Active High)

IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO
Interrupt Enable Out (Output; Active High)

IEO is High only if IEI is High and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$
Interrupt Request (Output; Active Low, Open Drain)

This signal is activated when the SCC requests an interrupt.

$\overline{INTACK}$
Interrupt Acknowledge (Input; Active Low)

This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of PCLK.

Serial Data

RxDA, RxDB
Receive Data (Inputs; Active High)

These input signals receive serial data at standard TTL levels.

TxDA, TxDB
Transmit Data (Outputs; Active High)

These output signals transmit serial data at standard TTL levels.

Miscellaneous

GND
Ground

PCLK
Clock (Input)

This is the master SCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock. PCLK is a TTL-level signal. Maximum transmit rate is 1/4 PCLK.

V_{cc}
+ 5 V Power Supply

ARCHITECTURE

The ESCC internal structure includes two full-duplex channels, two 10 × 19 bit SDLC/HDLC frame status FIFOs, two baud rate generators, internal control and interrupt logic, and a bus interface to a non-multiplexed bus. Associated with each channel are a number of Read and Write registers for mode control and status information, as well as logic necessary to interface with modems or other external devices (see Logic Symbol).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (Write) registers, two SYNC character (Write) registers, and four status (Read) registers. In addition, each baud rate generator has two (Read/Write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a Write register for the interrupt vector accessible through either channel, a Write-only Master Interrupt Control register, and three Read registers: one containing the vector with status information (Channel B only), one containing the vector without status (A only), and one containing the interrupt pending bits (A only).

The registers for each channel are designated as follows:

WR0–WR15—Write Registers 0 through 15. Two additional Write registers, WR6 Prime (WR6′) and WR7 Prime (WR7′), are available for enabling or disabling additional SDLC/HDLC/LocalTalk™ enhancements if bit D_0 of WR15 is set.

RR0–RR3, RR10, RR12, RR13, RR15—Read Registers 0 through 3, 10, 12, 13, and 15.

If bit D_2 of WR15 is set, then two additional Read registers, RR6 and RR7, are available. These registers are used with the 10 × 19 bit Frame Status FIFO.

Table 1 lists the functions assigned to each Read and Write register. The ESCC/LT contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

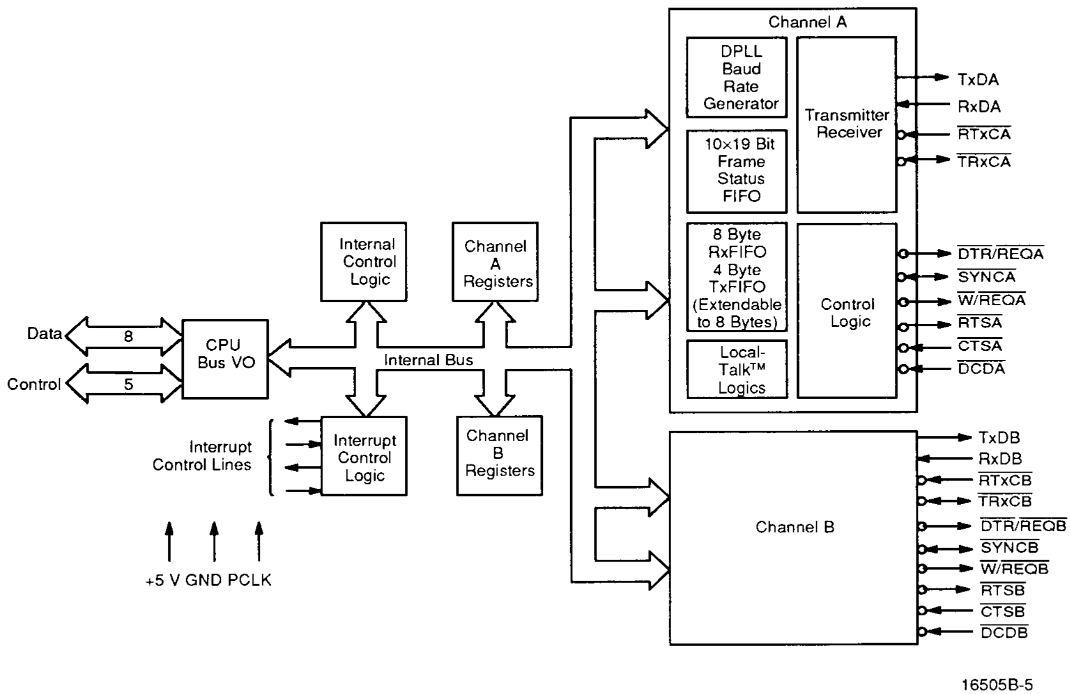

Figure 1. Block Diagram of ESCC/LT Architecture

Data Path

The transmit and receive data path illustrated in Figure 2 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data are routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and a 20-bit transmit shift register that can be loaded either from the sync-character registers or from the transmit data register. Depending on the operational mode, outgoing data are routed through one of four main paths before they are transmitted from the Transmit Data output (TxD).

Table 1. Read and Write Register Functions

Read Register Functions		Write Register Functions	
RR0	Transmit/Receive buffer status and External status	**WR1**	Interrupt conditions and data transfer mode definition
RR1	Special Receive Condition status (also 10 × 19 bit FIFO Frame Reception Status if WR15 bit D_2 is set)	**WR2**	Interrupt vector (accessed through either channel)
RR2	Modified interrupt vector (Channel B only) Unmodified interrupt vector (Channel A only)	**WR3**	Receive parameters and control
RR3	Interrupt Pending bits (Channel A only)	**WR4**	Transmit/Receive miscellaneous parameters and modes
RR6	LSB Byte Count (14-bit counter) (if WR15 bit D_2 set)	**WR5**	Transmit parameters and controls
RR7	MSB Byte Count (14-bit counter) and 10 × 19 bit FIFO Status (if WR15 bit D_2 is set)	**WR6**	Sync character or SDLC address field
RR8	Receive buffer	**WR6′**	LocalTalk™/ExtendedTx FIFO enhancements/ Revision ID Information (if bit D_0 of WR15 is set)
RR10	Miscellaneous XMTR, RCVR status	**WR7**	Sync character or SDLC flag
RR12	Lower byte of baud rate generator time constant	**WR7′**	SDLC/HDLC/FIFO Thresholds enhancements (if bit D_0 of WR15 is set)
RR13	Upper byte of baud rate generator time constant	**WR8**	Transmit buffer
RR15	External/Status interrupt information	**WR9**	Master interrupt control and reset (accessed through either channel)
		WR10	Miscellaneous transmitter/receiver control bits, data encoding
		WR11	Clock mode control, Rx and Tx clock source
		WR12	Lower byte of baud rate generator time constant
		WR13	Upper byte of baud rate generator time constant
		WR14	Miscellaneous control bits, DPLL control
WR0	Command Register, Register Pointers CRC initialize, initialization commands for the various modes, shift right/shift left command	**WR15**	External/Status interrupt control

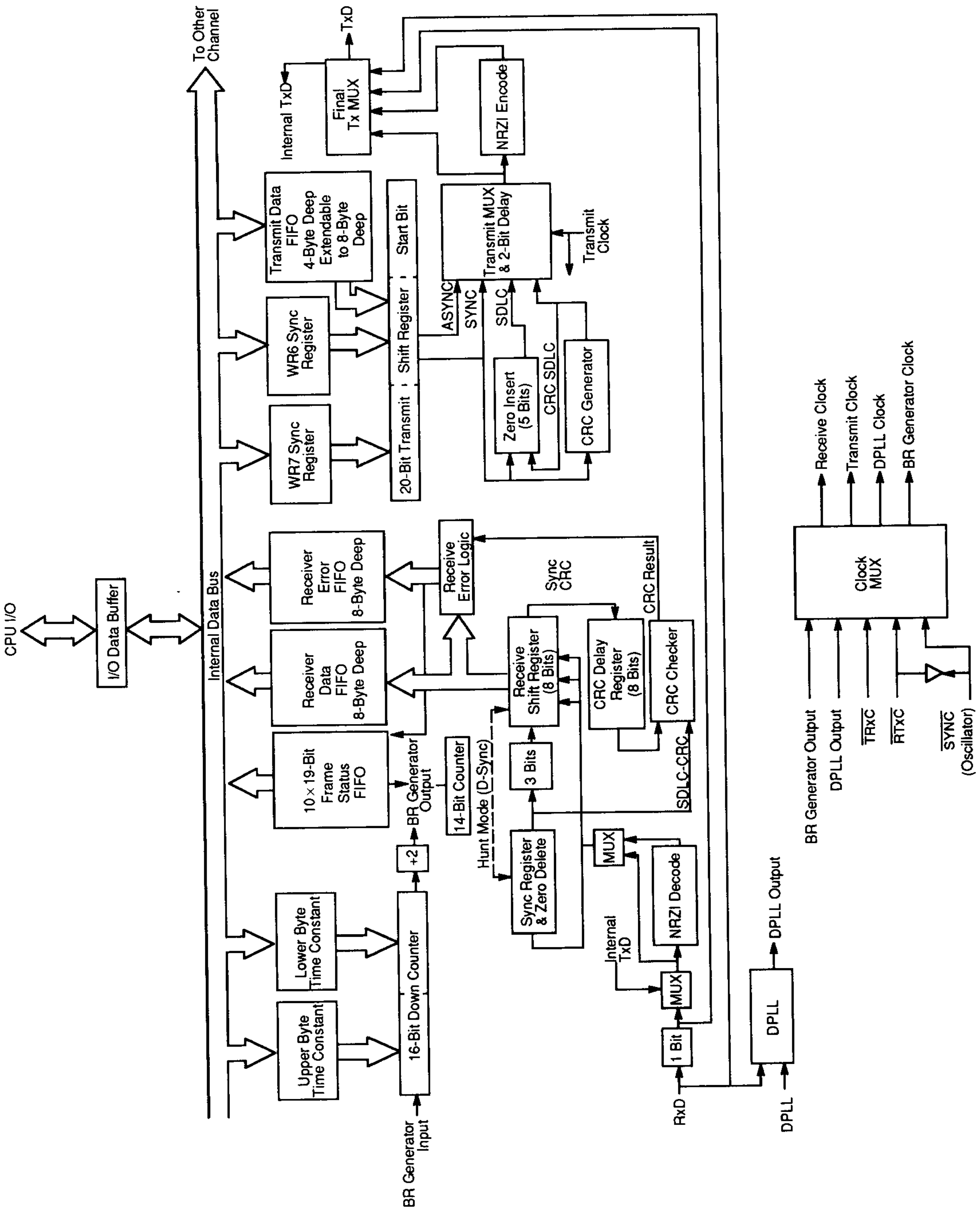

Figure 2. Data Path

DETAILED DESCRIPTION

The functional capabilities of the ESCC/LT can be described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, it interacts with the CPU and provides vectored interrupts and handshaking signals.

Deeper Tx and Rx FIFO Depth

The ESCC/LT has 8-byte FIFOs to buffer the received and transmitted data. The FIFOs can have two configuration modes; 8x4 or 8x8 FIFO modes. In 8x4 FIFO mode, an 8-byte Rx and 4-byte Tx FIFO are available in both channels A and B. In 8x8 FIFO mode, the Tx FIFO size is extended to 8-byte using the EFEN bit in WR6' making both Rx and Tx FIFO size equal to 8-byte deep.

At power-up, the ESCC/LT is defaulted to be in the 8x4 FIFO mode. If the extended FIFO mode is enabled, the additional 4-byte FIFO will sit between the CPU port and the 4-byte Tx FIFO. The combined depth will be 8. Data written to the ESCC/LT will bubble through this additional FIFO into the 4-byte Tx FIFO. When the extended FIFO mode is disabled, the transmit data path will bypass the extended FIFO and connect directly with the 4-byte Tx FIFO.

The extended FIFO mode can be enabled through by setting the relevant bits in the WR6' and WR7'. The extend Tx FIFO feature is enabled through a new control register, WR6'(Write Register 6 prime) for each channel. This register (WR6') can be written to in the same manner as the WR7' is on the Am85C30. This is done by setting the D0 of WR15 to 1 and then writing to register address 6. Please note that setting D0 of WR15 to 1 will enable both WR6' and WR7'. In order to read WR6', bit D2 of WR15 and bit D6 of WR7' are set to 1. Bits D0 and D1 in WR6' are read only. When D2 bit, the Extended FIFO Enable bit (EFEN) of the WR6' is set to 1, the Tx FIFO is extended to 8-byte deep and the ESCC/LT is in 8x8 FIFO mode. The D2 (EFEN) bit must be used in conjunction with the D5 (TXT) bit of the WR7'. The D2 (EFEN) bit is reset on a hardware or channel reset. The bit D3(RXT) and D5(TXT) in WR7' had been changed from the original 85C30 design to accommodate the deeper FIFO interrupt/DMA thresholds. The functions performed by D3 and D5 on the Am85C30, ESCC, are "hard wired" on the ESCC/LT. In the Am85C230A, the D5 bit represents the transmit threshold (TXT) and the D3(RXT) bit represents the receive threshold (RXT). If D5(TXT) bit of the WR7' is set, the ESCC/LT will either generated an interrupt or a DMA request when the transmit FIFO is completely empty in 8x4 FIFO mode or half empty in the 8x8 FIFO mode. If the D5(TXT) bit of the WR7' is not set, the ESCC/LT will generate an interrupt or DMA request when the top byte location in the transmit FIFO becomes empty in both 8x4 and 8x8 FIFO modes. The D5(TXT) bit of the WR7' is set to 1 after a hardware or channel reset. If the D3(RXT) bit of the WR7' is set, the ESCC/LT will either generate an interrupt or a DMA request when the receive FIFO is half full (i.e. has 4 bytes). If the D3(RXT) bit of the WR7' is not set, the ESCC/LT will generate an interrupt or a DMA request whenever only one byte is left in the receive FIFO. The D3(RXT) bit of the WR7' is reset after a hardware or channel reset.

READY Logic

The Am85C230A(ESCC/LT) improves its performance from the original Am85C30(ESCC) by implementing the Ready logic on silicon.

The Am85C30(ESCC) takes 3.5 to 4 PCLKs (known as the valid access recovery time) to complete a write operation to a register. If another write is attempted during this time, erroneous data can be written to the register. The purpose of adding READY logic is to keep external CPU informed about the internal write operation so that another write is not attempted before the valid access time is over. This feature is only available in the 44-pin PLCC package. A new pin/RDY is added on the ESCC/LT. The Ready function is asserted on power up.

Schmitt Trigger on inputs

To improve the ESCC/LT's noise immunity in the communication environment, Schmitt Trigger circuits are added to clock inputs TRxC and RTxC. Two of the inputs, CTS and DCD already have schmitt trigger circuits from the original Am85C30 (ESCC) core.

Sleep Mode

The Am85C230A, ESCC/LT supports sleep mode which is ideal for the low power/portable applications. The Am85C230A, can be put to sleep by stopping the PCLK. In the sleep mode, all registers values are saved.

Revision ID Information

The Am85C230A also provide information about various versions of SCC-type devices. This will allow the CPU to find out which device is in the system. The Revision ID information can be implemented using bits D0 and D1 of Write Register 6'. See WR6' descriptions in the Programming Information section for more details.

Data Communications Capabilities

The ESCC/LT provides two independent full-duplex channels programmable for use in any common asynchronous or SYNC data-communication protocol. Figure 3 and the following description briefly detail these protocols.

Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with 5 to 8 bits per character, plus optional even or odd parity. The transmitters can supply 1, 1 1/2, or 2 stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input. If the Low does not persist (as in the case of a transient), the character assembly process does not start.

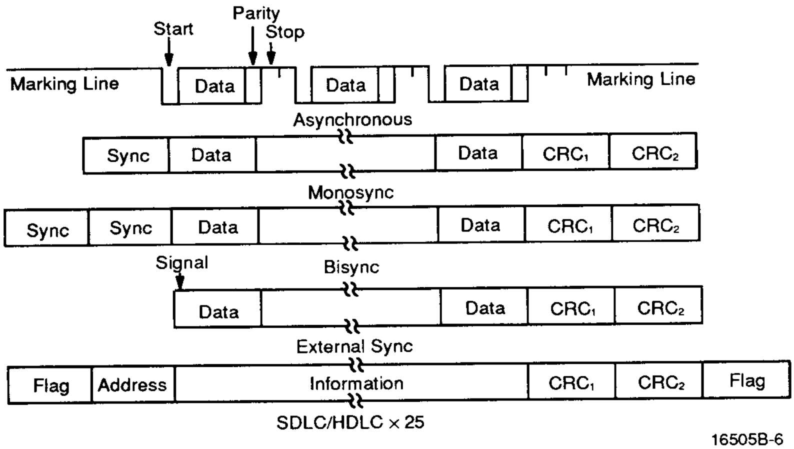

Figure 3. ESCC/LT Protocols

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of framing error as a new start bit; a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The ESCC/LT does not require symmetric transmit and receive clock signals—a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the $\overline{\text{SYNC}}$ pin may be programmed as an input used for functions, such as monitoring a ring indicator.

Synchronous Modes

The ESCC/LT supports both byte-oriented and bit-oriented synchronous communication. SYNC byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit SYNC character (Monosync), any 12-bit or 16-bit SYNC pattern (Bisync), or with an external SYNC signal. Leading SYNC characters can be removed without interrupting the CPU.

5- or 7-bit SYNC characters are detected with 8- or 16-bit patterns in the ESCC/LT by overlapping the larger pattern across multiple incoming SYNC characters as shown in Figure 4.

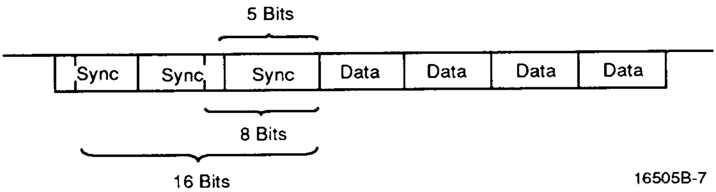

Figure 4. Detecting 5- or 7-Bit Synchronous Characters

CRC checking for Synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols, such as IBM BISYNC.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error-checking polynomials are supported. Either polynomial may be selected in BISYNC and MONOSYNC modes. Users may preset the CRC generator and checker to all 1s or all 0s. The ESCC also provides a feature that automatically transmits CRC data when no other data are available for transmission. This allows for high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there are no data or CRC to send in SYNC modes, the transmitter inserts 6-, 8-, or 16-bit SYNC characters, regardless of the programmed character length.

The ESCC/LT supports SYNC bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero-bit insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the ESCC/LT automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The ESCC/LT may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to 8 bits per character can be sent allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{SYNC}$ pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or 4 bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all 0s inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the ESCC/LT must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all 1s or all 0s. The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

NRZ, NRZI or FM coding may be used in any 1X mode. The parity options available in asynchronous modes are available in synchronous modes.

The ESCC/LT can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the ESCC/LT can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The ESCC then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the ESCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC Loop Mode

The ESCC/LT supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow and any number of secondary stations. In SDLC Loop mode, the ESCC/LT performs the functions of a secondary station while an ESCC/LT operating in regular SDLC mode can act as a controller (Figure 5).

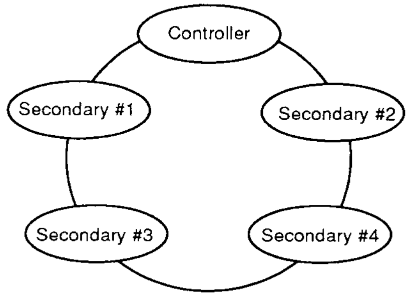

Figure 5. An SDLC Loop

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop and, in fact, must pass these messages to the rest of the loop by retransmitting them with a 1-bit time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations farther down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the ESCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

LocalTalk™ Implementation

The Am85C230A, ESCC/LT implements the entire LocalTalk™ SDLC packet format in the hardware. In addition, receive disable during transmit and end of packet DMA request are also implemented to improve system performance. The LocalTalk™ SDLC format shown in figure 6 contain three additional fields: a SYNC pulse, one additional beginning FLAG and an Abort Sequence. The SYNC pulse contains two bits without any transitions. This is a way of implementing collusion avoidance. The SYNC pulse transmission will set a bit in all listening ESCC/LTs, which will in turn prevent them from transmitting. In the receive mode, the DPLL detects SYNC pulse as 'missing clocks' and sets bits D6 and D7 in RR10. this will allow the CPU to prevent a ESCC/LT from transmitting. The additional opening FLAG field is used to meet the LocalTalk™ packet format. The LocalTalk™ protocol requires an abort sequence to be transmitted at the end of the information packet. the abort sequence is supposed to be minimum 12 bits of FM0 transmission. This data is required to "wake up" the transmitters that were deferring the transmission based on detecting the SYNC pulse prior to an attempt to transmit. The ESCC/LT will generate 13 FM0 transitions. Enabling the transmitter will automatically disable the receiver if the Am85C230A, ESCC/LT is in the LocalTalk™ mode. When the ESCC/LT is in the LocalTalk™ mode and the receive FIFO threshold is set for four, the device will generated a DMA request if the packet that is being received ends and there are less than 4 bytes in the FIFO. This will alert the CPU that there is data to be read from the receive FIFO. Furthermore, the DMA request generated will stay active until all data bytes are read from the receive FIFO. The LocalTalk™ module is implemented as a separate state machine monitoring the opration of the ESCC/LT and can be enabled through bit D3(LTEN) of the WR6'. When D3(LTEN) bit is set and the SDLC mode is enabled, the LocalTalk™ module will control the state transmission within the ESCC/LT transmitter, thereby generating the SYNC pulse and two FLAGs, and will close transmission with CRC, FLAG, and the ABORT sequence. In LocalTalk™ mode, values of auto flag (bit D0 in WR7') and mark idle/flag idle (bit D3 in WR10) will be preserved and treated as do'nt care. The D3(LTEN) bit is reset on a hardware or channel reset.

SYNC Pulse	Beginning FLAG1 01111110	Beginning FLAG2 01111110	Address 8 bits	DATA	CRC 16 bits	Ending FLAG 01111110	Abort Sequence

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Figure 6. LocalTalk™ SDLC Format

Baud Rate Generator

Each channel in the ESCC/LT contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On start-up, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching zero; the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{\text{TRxC}}$ pin, the output of the baud rate generator may be echoed out via the $\overline{\text{TRxC}}$ pin.

The following formula relates the time constant to the baud rate where PCLK or $\overline{\text{RTxC}}$ is the baud rate generator input frequency in Hz. The clock mode is X1, X16, X32, or X64 as selected in Write Register 4, bits D_6 and D_7. Synchronous operation modes should select X1 and asynchronous should select X16, X32, or X64.

$$\text{Time Constant} = \left[\frac{\text{PCLK or RTxC Frequency}}{2\,(\text{Baud Rate})(\text{Clock Mode})}\right] - 2$$

The following formula relates the time constant to the baud rate. (The baud rate is in bits/second and the BR clock period is in seconds given by Clock Mode/Clock Frequency.)

$$\text{baud rate} = \frac{1}{2\,(\text{Time Constant} + 2) \times (\text{BR Clock Period})}$$

Time Constant Values for Standard Baud Rates at BR Clock = 3.9936 MHz

Rate (Baud)	Time Constant (decimal/Hex notation)		Error
19200	102	(0066)	0
9600	206	(00CE)	0
7200	275	(0113)	0.12%
4800	414	(019E)	0
3600	553	(0229)	0.06%
2400	830	(033E)	0
2000	996	(03E4)	0.04%
1800	1107	(0453)	0.03%
1200	1662	(067E)	0
600	3326	(0CFE)	0
300	6654	(19FE)	0
150	13310	(33FE)	0
134.5	14844	(39FC)	0.0007%
110	18151	(46E7)	0.0015%
75	26622	(67FE)	0
50	39934	(98FE)	0

Digital Phase-Locked Loop

The ESCC contains a digital phase-locked loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

For NRZI encoding, the DPLL counts the 32X clock to create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1/0 or 0/1). As long as no transitions are detected, the DPLL output will be free running and its input clock source will be divided by 32, producing an output clock without any phase jitter. Upon detecting a transition the DPLL will adjust its clock output (during the next counting cycle) by adding or subtracting a count of 1, thus producing a terminal count closer to the center of the bit cell. The adding or subtracting of a count of 1 will produce a phase jitter of ±5.63° on the output of the DPLL. Because the SCC's DPLL uses both edges of the incoming signal to compare with its clock source, the mark-space ratio (50%) of the incoming signal should not deviate by more than ±1.5% if proper locking is to occur.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15/16 counting transition.

The 32X clock for the DPLL can be programmed to come from either the $\overline{\text{RTxC}}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the SCC via the $\overline{\text{TRxC}}$ pin (if this pin is not being used as an input).

Crystal Oscillator

When using a crystal oscillator to supply the receive or transmit clocks to a channel of the SCC, the user should:

1. Select a crystal oscillator that satisfies the following specifications:
   - 30 ppm @ 25°C
   - 50 ppm over temperatures of –20° to 70°C
   - 5 ppm/yr aging
   - 5-MW drive level
2. Place crystal across $\overline{\text{RTxC}}$ and $\overline{\text{SYNC}}$ pins.
3. Place 30-pF capacitors to ground from both $\overline{\text{RTxC}}$ and $\overline{\text{SYNC}}$ pins.
4. Set bit D_7 of WR11 to 1.

Data Encoding

The ESCC/LT may be programmed to encode and decode the serial data in four different ways (Figure 7). In NRZ encoding, a 1 is represented by a High level, and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level, and a 0 is represented by a change in level. In FM_1 (more properly, biphase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell, and a 0 is represented by no additional transition at the center of the bit cell. In FM_0 (biphase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the ESCC/LT can be used

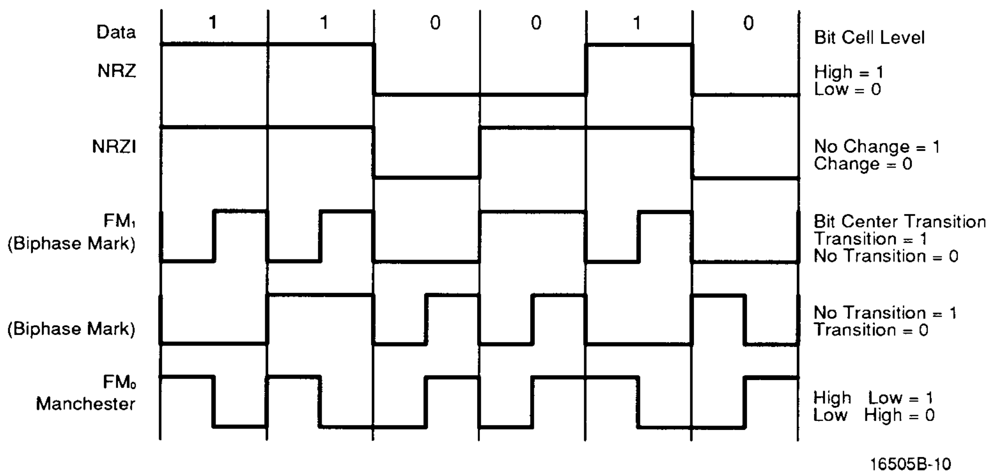

Figure 7. Data Encoding Methods

to decode Manchester (biphase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0/1, the bit is a 0. If the transition is 1/0, the bit is a 1.

Auto Echo and Local Loopback

The ESCC/LT is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes but works in SYNC and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{CTS}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed, and the programmer is responsible for disabling transmitter interrupts and $\overline{WAIT/REQUEST}$ on transmit.

The ESCC/LT is also capable of Local Loopback. In this mode, TxD is RxD just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data, and RxD is ignored (except to be echoed out via TxD). The $\overline{CTS}$ and $\overline{DCD}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in asynchronous, SYNC, and SDLC modes with NRZ, NRZI, or FM coding of the data stream.

I/O Interface Capabilities

The ESCC/LT offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

Polling

All interrupts are disabled. Three status registers in the ESCC/LT are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

Interrupts

When an ESCC/LT responds to an Interrupt Acknowledge signal (INTACK) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 9 and 10).

To speed interrupt response time, the ESCC/LT can modify 3 bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the ESCC/LT (Transmit, Receive, and External/Status interrupts in both channels) has 3 bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write-only.

The other 2 bits are related to the CPU-Bus interrupt priority chain (Figure 8). As a CPU-Bus peripheral, the ESCC/LT may request an interrupt only when no higher priority device is requesting one, for example, when IEI is High. If the device in question requests an interrupt, it pulls down $\overline{INT}$. The CPU then responds with $\overline{INTACK}$, and the interrupting device places the vector on the A/D bus.

In the old SCC, the IP bit signals a need for interrupt servicing. When an IP bit is set to 1 and the IEI input is High, the $\overline{INT}$ output is pulled Low, requesting an interrupt. In the ESCC/LT, if the IE bit is set for an interrupt, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the ESCC/LT and external to the ESCC/LT are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the ESCC/LT being pulled Low and

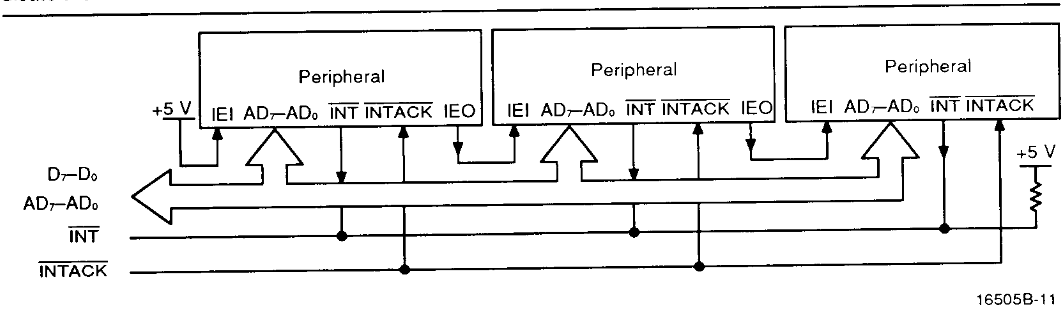

Figure 8. Z-Bus Interrupt Schedule

propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive, and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receive, Transmit, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the Receive can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive condition
- Interrupt on all Receive Characters or Special Receive condition
- Interrupt on Special Receive condition only

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in asynchronous mode, end-of-frame in SDLC mode, and optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary Receive Character Available interrupt only in the status placed in the vector during the Interrupt Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive Conditions any time after the first Receive Character Interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, and $\overline{\text{SYNC}}$ pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, a zero count in the baud rate generator, the detection of a Break (asynchronous mode), Abort (SDLC mode), or EOP (SDLC Loop mode) sequence in the data stream. The interrupt caused by the Abort or EOP has a special feature allowing the ESCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA Block Transfer

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the $\overline{\text{WAIT}}/\overline{\text{REQUEST}}$ output in conjunction with the Wait/Request bits in WR1. The $\overline{\text{WAIT}}/\overline{\text{REQUEST}}$ output can be defined under software control as a $\overline{\text{WAIT}}$ line in the CPU Block Transfer mode or as a $\overline{\text{REQUEST}}$ line in the DMA Block Transfer mode.

To a DMA controller, the ESCC $\overline{\text{REQUEST}}$ output indicates that the ESCC is ready to transfer data to or from memory. To the CPU, the $\overline{\text{WAIT}}$ line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{\text{DTR}}/\overline{\text{REQUEST}}$ can be used as the transmit request line, thus allowing full-duplex operation under DMA control.

PROGRAMMING INFORMATION

Each channel has fifteen Write registers that are individually programmed from the system bus to configure the functional personality of each channel. Each channel also has eight Read registers from which the system can read Status, Baud rate, or Interrupt information.

On the Am85C230A, only four data registers (Read and Write for Channels A and B) are directly selected by a High on the D/$\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$, and A/$\overline{B}$ pins. All other registers are addressed indirectly by the content of Write Register 0 in conjunction with a Low on the D/$\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$, and A/$\overline{B}$ pins. If bit D_3 in WR0 is 1 and bits 5 and 6 are 0, then bits 0, 1, and 2 address the higher registers 8 through 15. If bits 4, 5, and 6 contain a different code, bits 0, 1, and 2 address the lower registers 0 through 7 as shown in Table 2.

Writing to or reading from any register except RR0, WR0, and the data registers thus involves two operations:

First, write the appropriate code into WR0, then follow this by a Write or Read operation on the register thus specified. Bits 0 through 4 in WR0 are automatically cleared after this operation, so that WR0 then points to WR0 or RR0 again.

Channel A/Channel B selection is made by the A/$\overline{B}$ input (High = A, Low = B).

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set and, finally, receiver or transmitter enable.

Table 2. Register Addressing

D/$\overline{C}$	"Point High" Code In WR0:	D_2, D_1, D_0 In WR0:			Write Register	Read Register
High	Either Way	X	X	X	Data	Data
Low	Not True	0	0	0	0	0
Low	Not True	0	0	1	1	1
Low	Not True	0	1	0	2	2
Low	Not True	0	1	1	3	3
Low	Not True	1	0	0	4	(0)
Low	Not True	1	0	1	5	(1)
Low	Not True	1	1	0	6	(2)
Low	Not True	1	1	1	7	(3)
Low	True	0	0	0	Data	Data
Low	True	0	0	1	9	–
Low	True	0	1	0	10	10
Low	True	0	1	1	11	(15)
Low	True	1	0	0	12	12
Low	True	1	0	1	13	13
Low	True	1	1	0	14	(10)
Low	True	1	1	1	15	15

Read Registers

The ESCC contains eight Read registers [actually nine, counting the receive buffer (RR8) in each channel]. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). In addition, if bit D_2 of WR15 is set, RR6 and RR7 are available for providing frame status from the 10 × 19 bit Frame Status FIFO. Figure 9 shows the formats for each Read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring, for example, when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1). Please refer to Am85C30 Technical Manual for detailed descriptions of the read registers.

Write Registers

The ESCC contains 15 Write registers (16 counting WR8, the transmit buffer) in each channel. These Write registers are programmed separately to configure the functional "personality" of the channels. Two registers (WR2 and WR9) are shared by the two channels that can be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. In addition, if bit D_0 of WR15 is set, Write Register 7 prime (WR7′) and Write Register 6 prime (WR6′) are available for programming additional SDLC/HDLC/LocalTalk enhancements. When bit D_0 of WR15 is set, executing a write to WR7 and WR6 actually writes to WR7′ and WR6′ respectively to further enhance the functional "personality" of each channel. Figure 9 shows the format of each Write register. For detail descriptions of the registers, please refer to Am85C30 Technical Manual (execpt for WR6' and D3, 5 bits of WR7', refer to Figure 11).

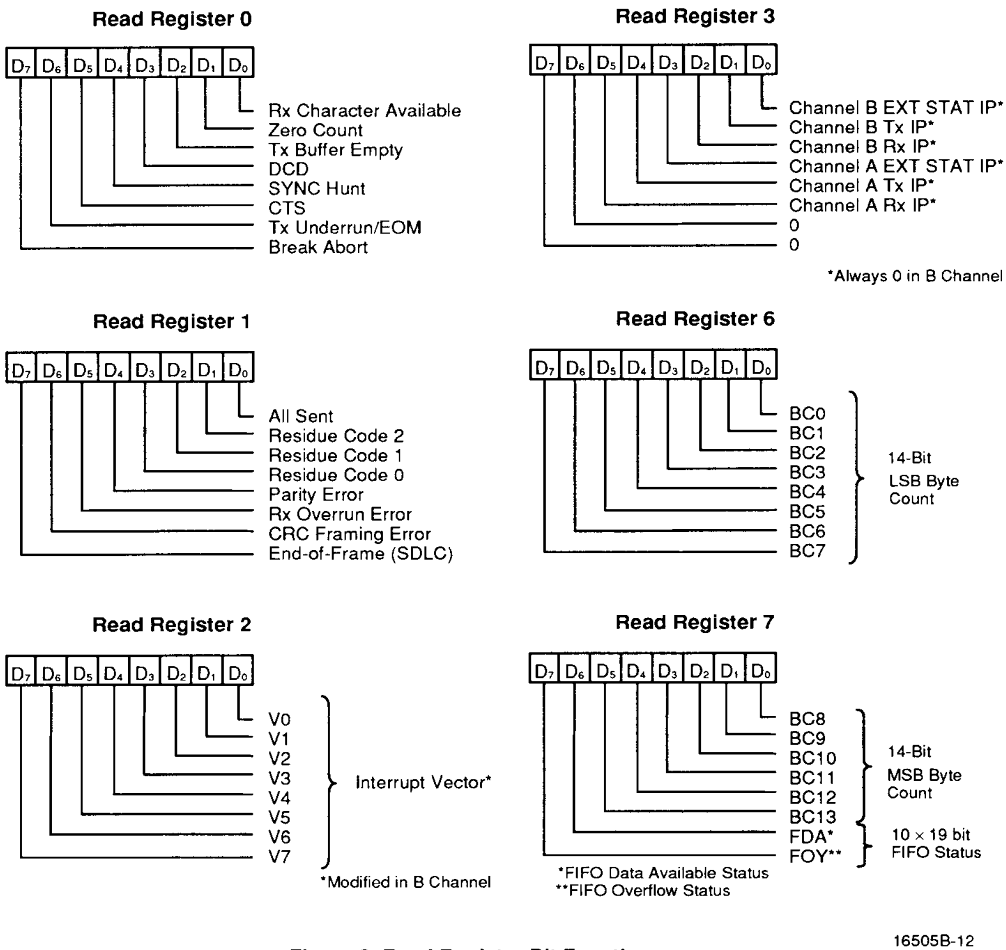

Figure 9. Read Register Bit Functions

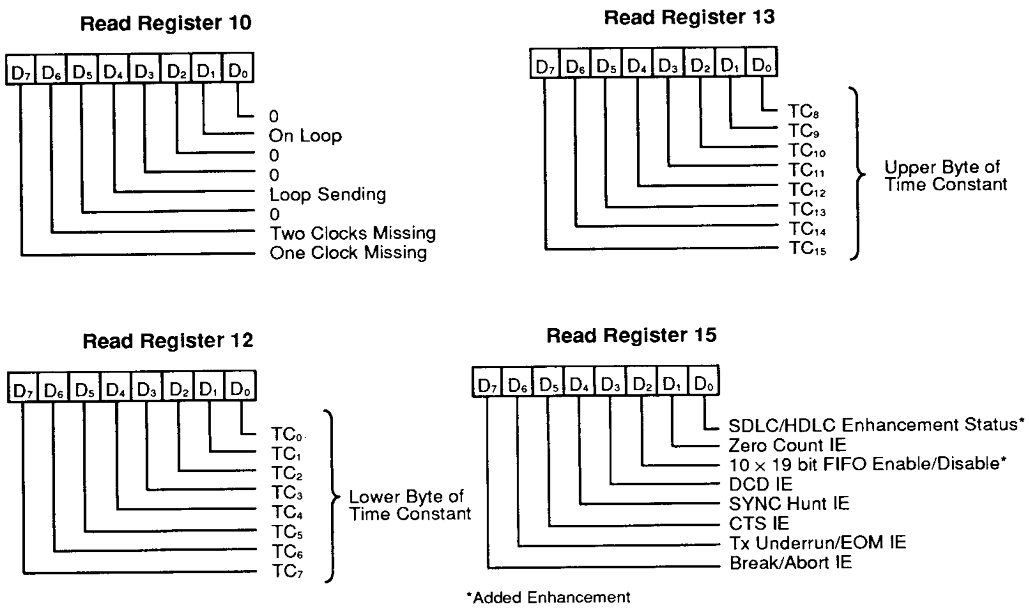

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Figure 9. Read Register Bit Functions (continued)

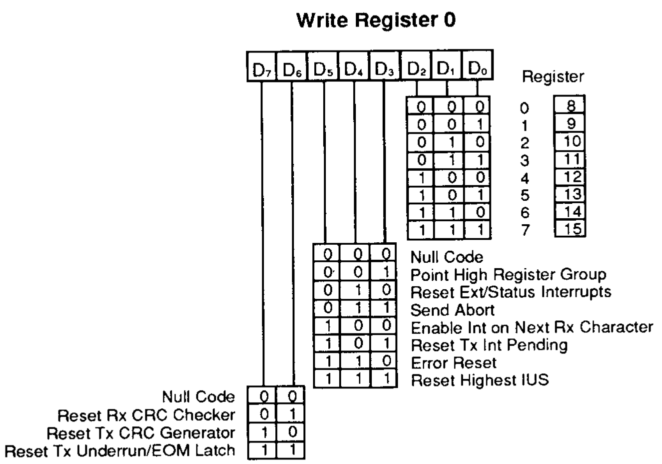

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Figure 10. Write Register Bit Functions

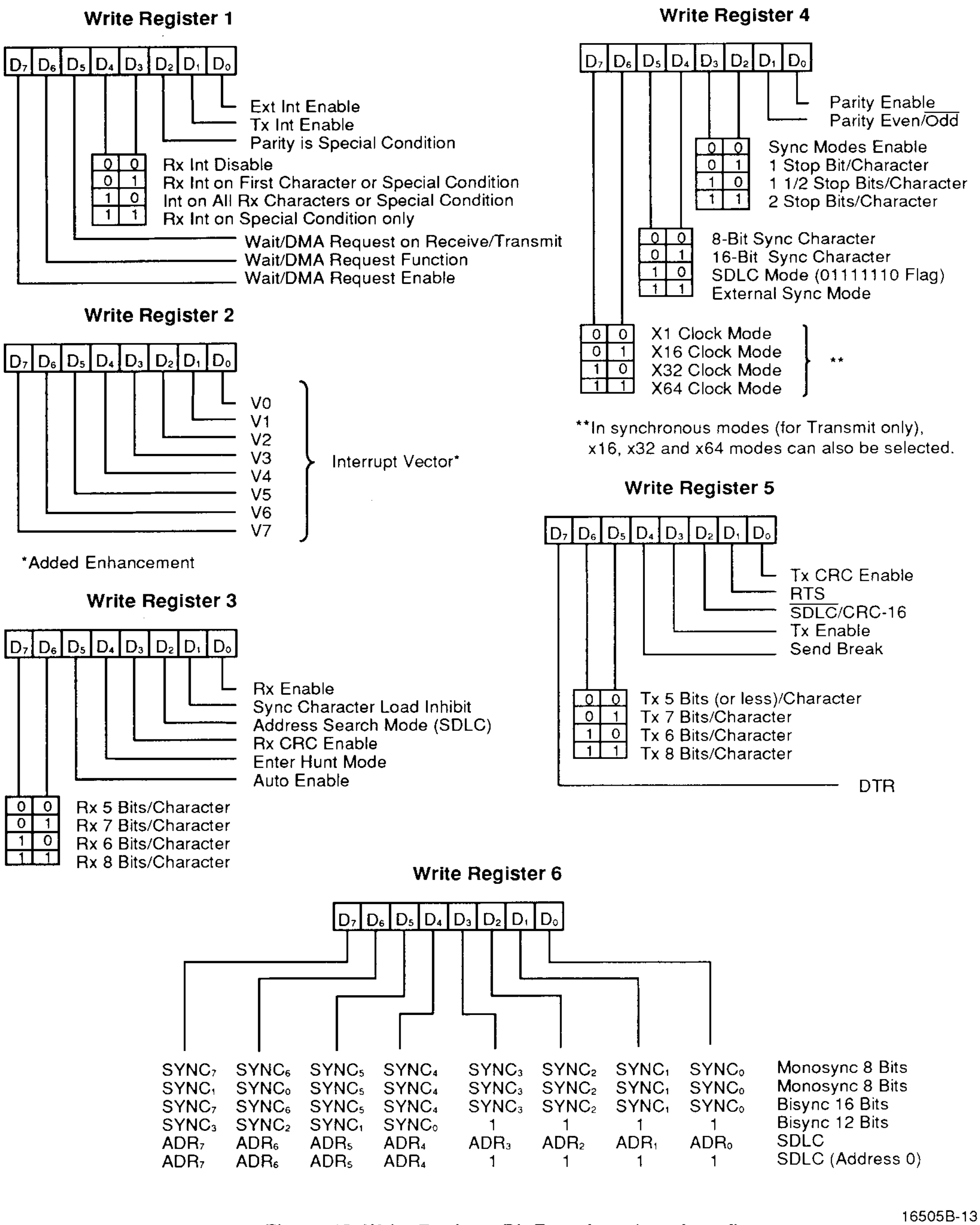

Figure 10. Write Register Bit Functions (continued)

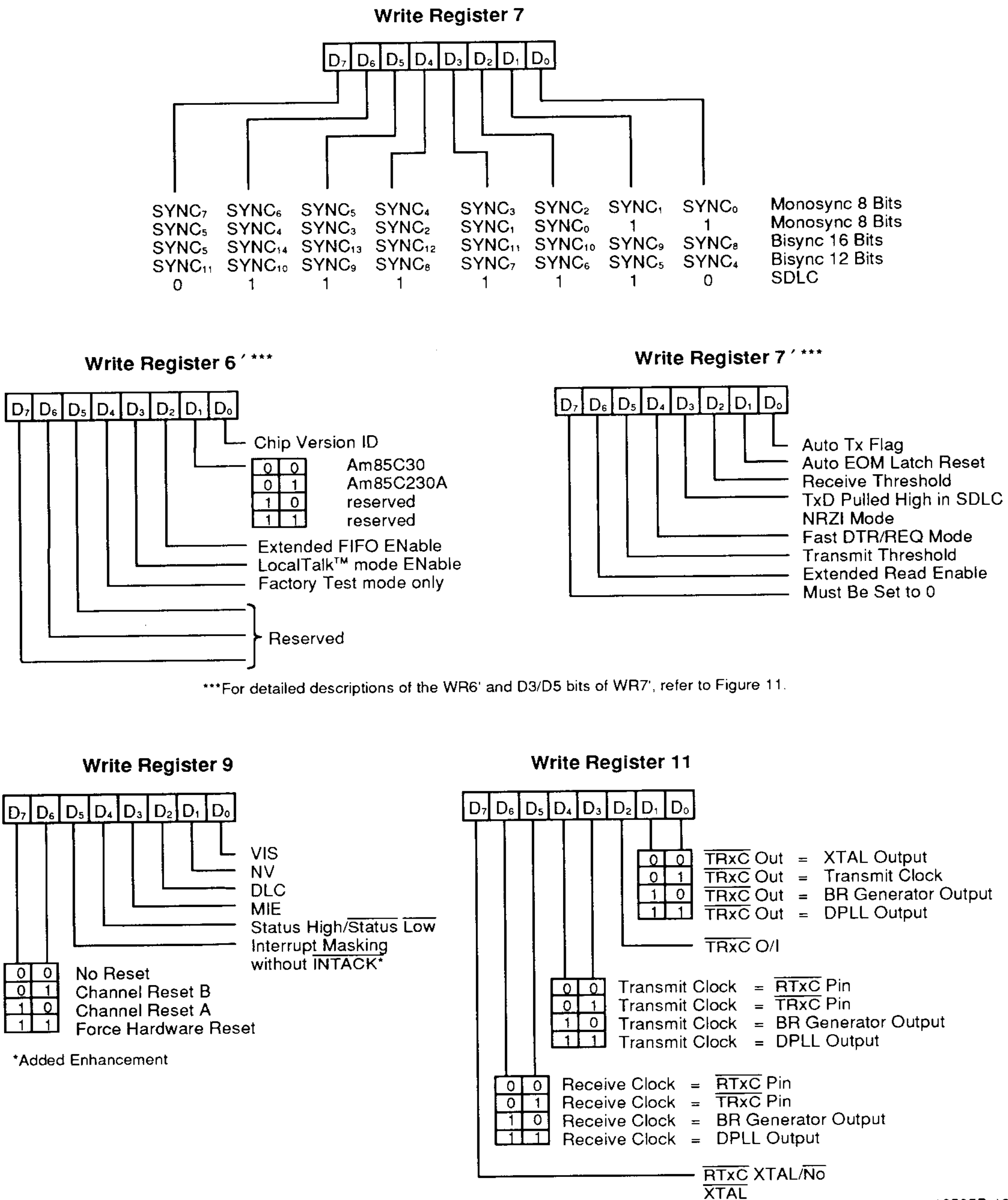

Figure 10. Write Register Bit Functions (continued)

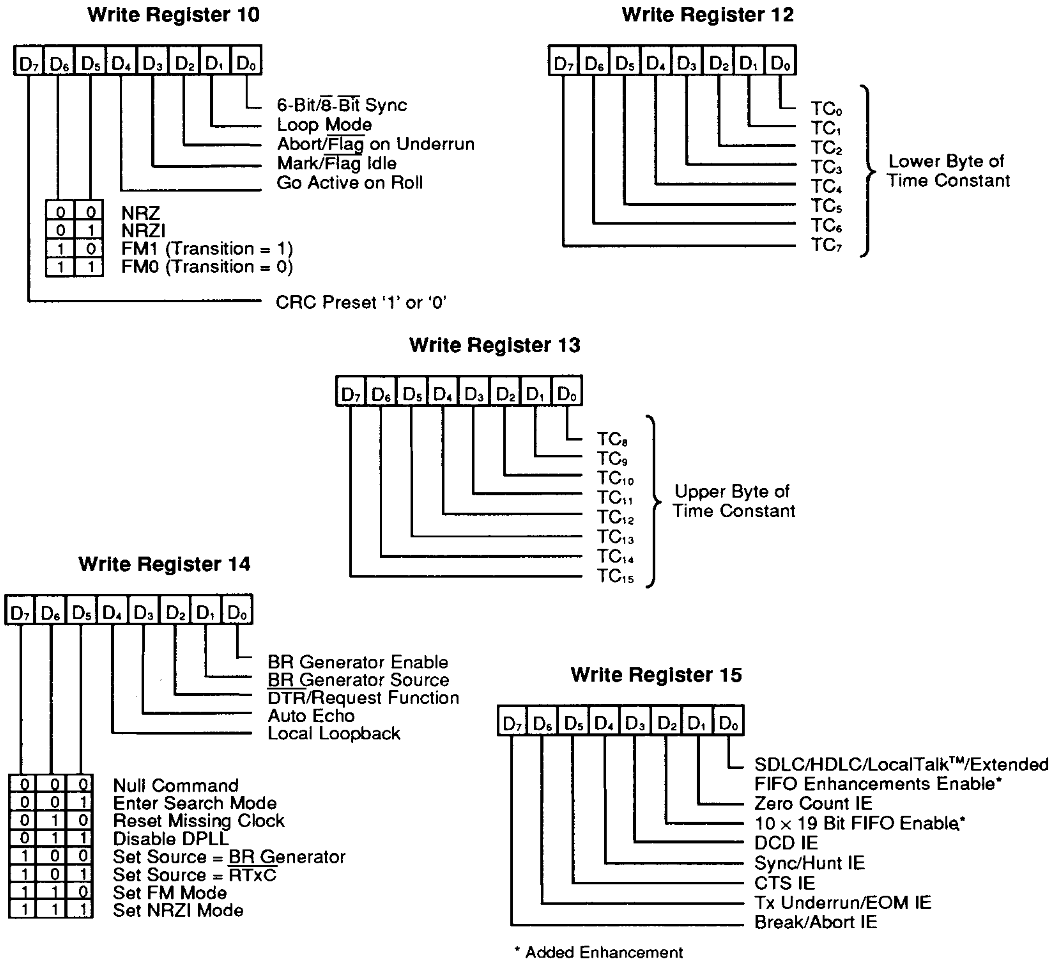

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Figure 10. Write Register Bit Functions (continued)

WR6′

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	X	X	FTM	LTEN	EFEN	ID1	ID0

X = RESERVED

FTM = Factory Test Mode
This bit is used for factory test purpose only and should always be set to '0'.

LTEN = LocalTalk™ mode ENable
If this bit is set to '1', and the SDLC mode is eabled, the ESCC will automatically open transmission with the SYNC pulse and two FLAGs, and will close transmission wih CRC, FLAG, and the ABORT sequence. This bit is reset on hardware or channel reset.

EFEN = Extended FIFO ENable
When set to '1', this bit extends the Tx FIFO to 8-byte deep and puts ESCC/LT in 8x8 FIFO mode. EFEN must be used in conjunction with the TXT bit in WR7′. This bit is reset on hardware or channel reset.

ID1, 0 = Chip Version ID
- = 0 0 Am85C30
- = 0 1 Am85C230A
- = 1 0 Reserved
- = 1 1 Reserved

Modified WR7′

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	TXT	*	RXT	*	*	*

* = Same as in the ESCC (Am85C30)

TXT = Transmit Threshold
- = 1 The ESCC/LT will either generate an interrupt or a DMA request when the transmit FIFO is completely empty in 8x4 mode or half empty in 8x8 mode.
- = 0 The ESCC/LT will generate an interrupt or a DMA request when the top byte location in the transmit FIFO becomes empty in both 8x4 mode and 8x8 modes.

TXT bit is reset to 1 after a hardware or channel reset

RXT = Receive Threshold
- = 1 The ESCC/LT will either generate an interrupt or a DMA request when the receive FIFO is half full (i.e., has 4 bytes).
- = 0 The ESCC/LT will generate an interrupt or a DMA request whenever there is one byte in the receive FIFO.

RXT bit is reset to 0 after a hardware or channel reset

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Figure 11. Extended FIFO/LocalTalk™ Enhancement Implementation

Am85C230A Timing

The ESCC/LT generates internal control signals from $\overline{\text{WR}}$ and $\overline{\text{RD}}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{\text{WR}}$ and $\overline{\text{RD}}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the ESCC/LT. The recovery time required for proper operation is specified from the falling edge of $\overline{\text{WR}}$ or $\overline{\text{RD}}$ in the first transaction involving the ESCC/LT, to the falling edge of $\overline{\text{WR}}$ or $\overline{\text{RD}}$ in the second transaction involving the ESCC/LT. This time must be at least 3 1/2 PCLK regardless of which register or channel is being accessed.

Read Cycle Timing

Figure 12 illustrates Read cycle timing. Addresses on A/$\overline{\text{B}}$ and D/$\overline{\text{C}}$ and the status on $\overline{\text{INTACK}}$ must remain stable throughout the cycle. If $\overline{\text{CE}}$ falls after $\overline{\text{RD}}$ falls or if it rises before $\overline{\text{RD}}$ rises, the effective $\overline{\text{RD}}$ is shortened.

Write Cycle Timing

Figure 13 illustrates Write cycle timing. Addresses on A/$\overline{\text{B}}$ and D/$\overline{\text{C}}$ and the status on $\overline{\text{INTACK}}$ must remain stable throughout the cycle. If $\overline{\text{CE}}$ falls after $\overline{\text{WR}}$ falls or if it rises before $\overline{\text{WR}}$ rises, the effective $\overline{\text{WR}}$ is shortened. Data must be valid before the rising edge of $\overline{\text{WR}}$.

Interrupt Acknowledge Cycle Timing

Figure 14 illustrates Interrupt Acknowledge cycle timing. Between the time $\overline{\text{INTACK}}$ goes Low and the falling edge of $\overline{\text{RD}}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the ESCC/LT and IEI is High when $\overline{\text{RD}}$ falls, the Acknowledge cycle is intended for the ESCC/LT. In this case, the ESCC/LT may be programmed to respond to $\overline{\text{RD}}$ Low by placing its interrupt vector on D_7–D_0 ; it then sets the appropriate Interrupt-Under-Service latch internally.

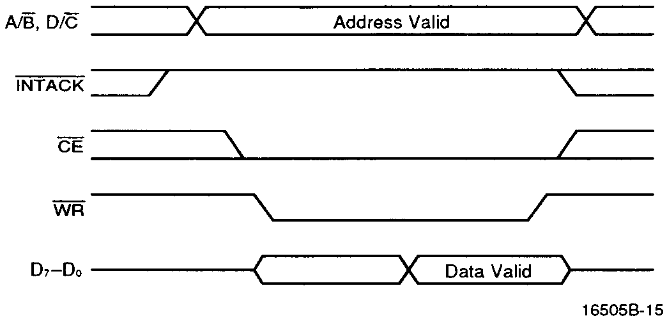


Figure 12. Read Cycle Timing

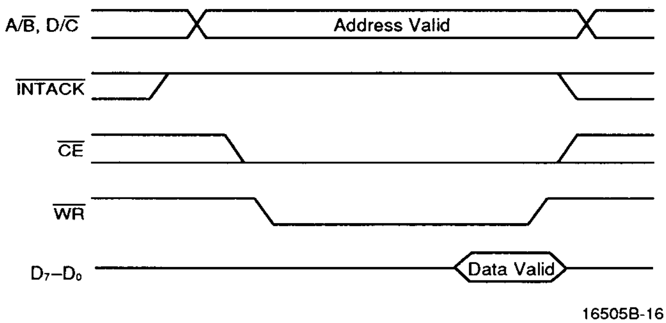


Figure 13. Write Cycle Timing

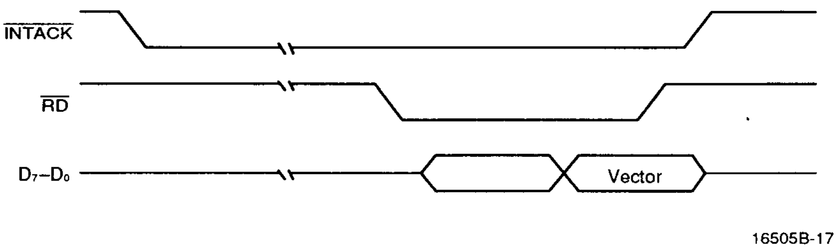


Figure 14. Interrupt Acknowledge Cycle Timing

FIFO

FIFO Enhancements

When used with a DMA controller, the Am85C230A Frame Status FIFO enhancement maximizes the ESCC/LT's ability to receive high-speed back-to-back SDLC messages while minimizing frame overruns due to CPU latencies in responding to interrupts.

Additional logic was added to the industry-standard NMOS SCC consisting of a 10-deep by 19-bit status FIFO, a 14-bit receive byte counter, and control logic as shown in Figure 15. The 10 × 19 bit status FIFO is separate from the existing 8-byte receive data and error FIFOs.

When the enhancement is enabled, the status in Read Register 1 (RR1) and byte count for the SDLC frame will be stored in the 10 × 19 bit status FIFO. This allows the DMA controller to transfer the next frame into memory while the CPU verifies that the message was properly received.

Summarizing the operation, data is received, assembled, and loaded into the 8-byte receive FIFO before being transferred to memory by the DMA controller. When a flag is received at the end of an SDLC frame, the frame byte count from the 14-bit counter and 5 status bits are loaded into the status FIFO for verification by the CPU. The CRC checker is automatically reset in preparation for the next frame, which can begin immediately. Since the byte count and status are saved for each frame, the message integrity can be verified at a later time. Status information for up to 10 frames can be stored before a status FIFO overrun could occur.

If receive interrupts are enabled while the 10 × 19 FIFO is enabled, an SDLC end-of-frame special condition will not lock the 8-byte receive data FIFO. An SDLC end-of-frame still locks the 8-byte receive data FIFO in "Interrupt on first Receive Character or Special Condition" and "Interrupt on Special Condition Only" modes when the 10 × 19 FIFO is disabled. This feature allows

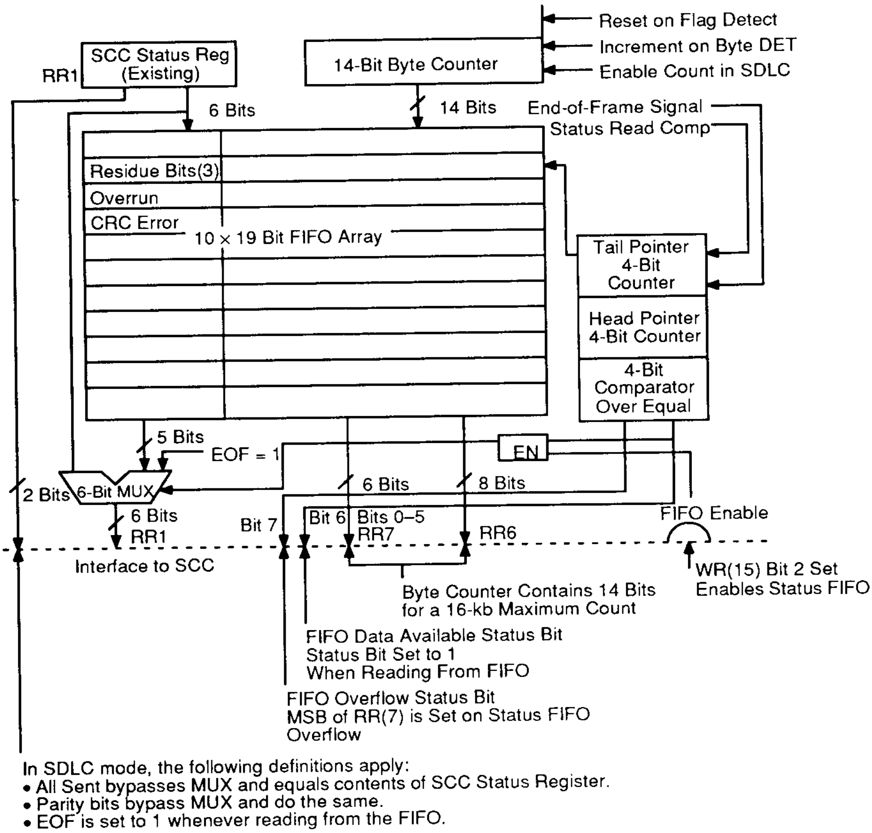


Figure 15. Am85C230A Status Register Modifications

the 10 × 19 SDLC FIFO to accept multiple SDLC frames without CPU intervention at the end of each frame.

FIFO Detail

For a better understanding of details of the FIFO operation, refer to the block diagram contained in Figure 15.

Enable/Disable

This FIFO is implemented so that it is enabled when WR15 bit 2 is set and the ESCC/LT is in the SDLC/HDLC mode, otherwise the status register contents bypass the FIFO and go directly to the bus interface (the FIFO pointer logic is reset either when disabled or via a channel or power-on reset). The FIFO mode is disabled on power-up (WR15 bit 2 is set to 0 on reset). The effects of backward compatibility on the register set are that RR4 is an image of RR0, RR5 is an image of RR1, RR6 is an image of RR2, and RR7 is an image of RR3. For the details of the added registers, refer to Figure 17. The status of the FIFO Enable signal can be obtained by reading RR15 bit 2. If the FIFO is enabled, the bit will be set to 1; otherwise, it will be reset.

Read Operation

When WR15 bit 2 is set and the FIFO is not empty, the next read to status register RR1 or the additional registers RR7 and RR6 will actually be from the FIFO. Reading status register RR1 causes one location of the FIFO to be emptied, so status should be read after reading the byte count, otherwise the count will be incorrect. Before the FIFO underflows, it is disabled. In this case, the multiplexer is switched to allow status to be read directly from the status register, and reads from RR7 and RR6 will contain bits that are undefined. Bit 6 of RR7 (FIFO Data Available) can be used to determine if status data is coming from the FIFO or directly from the status register, since it is set to 1 whenever the FIFO is not empty.

Because not all status bits are stored in the FIFO, the All Sent, Parity, and EOF bits will bypass the FIFO. The status bits sent through the FIFO will be Residue Bits (3), Overrun, and CRC Error.

The sequence for proper operation of the byte count and FIFO logic is to read the registers in the following order, RR7, RR6, and RR1 (reading RR6 is optional). Additional logic prevents the FIFO from being emptied by multiple reads from RR1. The read from RR7 latches the FIFO empty/full status bit (bit 6) and steers the status multiplexer to read from the SCC megacell instead of the status FIFO (since the status FIFO is empty). The read from RR1 allows an entry to be read from the FIFO (if the FIFO was empty, logic is added to prevent a FIFO underflow condition).

Write Operation

When the end of an SDLC frame (EOF) has been received and the FIFO is enabled, the contents of the status and byte-count registers are loaded into the FIFO. The EOF signal is used to increment the FIFO. If the FIFO overflows, the MSB of RR7 (FIFO Overflow) is set to indicate the overflow. This bit and the FIFO control logic are reset by disabling and reenabling the FIFO control bit (WR15 bit 2). For details of FIFO control timing during an SDLC frame, refer to Figure 16.

Byte Counter Detail

The 14-bit byte counter allows for packets up to 16K bytes to be received. For a better understanding of its operation, refer to Figures 15 and 16.

Enable

The byte counter is enabled when the ESCC/LT is in the SDLC/HDLC mode and WR15 bit 2 is set to 1.

Reset

The byte counter is reset whenever an SDLC flag character is received. The reset is timed so that the contents of the byte counter are successfully written into the FIFO.

Increment

The byte counter is incremented by writes to the data FIFO. The counter represents the number of bytes received by the ESCC/LT, rather than the number of bytes transferred from the ESCC/LT. (These counts may differ by up to the number of bytes in the receive data FIFO contained in the ESCC/LT.)

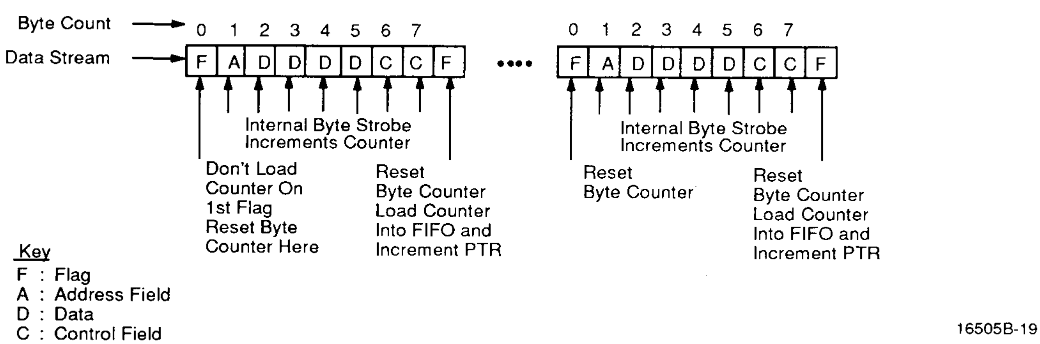
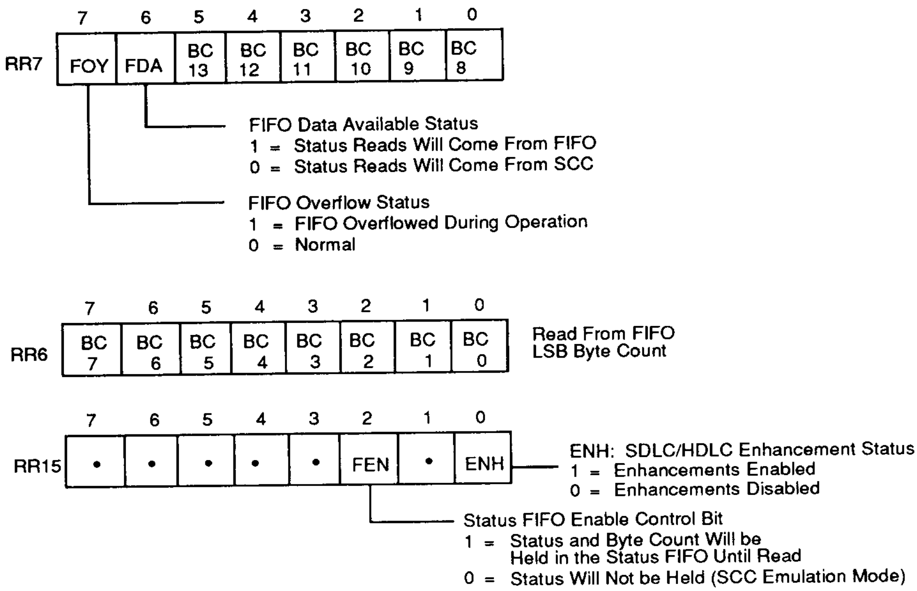


Figure 16. SDLC Byte Counting Detail



• = No Change From NMOS SCC DFN

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Figure 17. SCC Additional Registers

Am85C230A SDLC/HDLC Enhancement Register Access

SDLC/HDLC enhancements on the Am85C230A are enabled or disabled via bits D_2 or D_0 in WR15. Bit D_2 determines whether or not the 10 × 19 bit SDLC/HDLC frame status FIFO is enabled while bit D_0 determines whether or not other enhancements are enabled via WR7′. Table 3 shows what functions on the Am85C230A are enabled when these bits are set.

When bit D_2 of WR15 is set to 1, two additional registers (RR6 and RR7) per channel specific to the 10 × 19 bit Frame Status FIFO are made available. The Am85C230A register map when this function is enabled is shown in Table 4.

Bit D_0 of WR15 determines whether or not other enhancements pertinent only to SDLC/HDLC/LocalTalk™/Extended FIFO mode operation are available for

Table 3. Enhancement Options

WR15 Bit D_2 10 × 19 Bit FIFO Enabled	WR15 Bit D_0 SDLC/HDLC Enhancement Enabled	WR7′ Bit D_6 Extended Read Enabled	Functions Enabled
1	0	x	10 × 19 bit FIFO enhancement enabled only
0	1	0	SDLC/HDLC enhancements enabled only
0	1	1	SDLC/HDLC enhancements enabled with extended read enabled
1	1	0	10 × 19 bit FIFO and SDLC/HDLC enhancements enabled
1	1	1	10 × 19 bit FIFO and SDLC/HDLC enhancements with extended read enabled

programming via WR7′ and WR6′ as shown below. Write Register 7 prime (WR7′) and Write Register 6 prime (WR6′) can be written to when bit D_0 of WR15 is set to 1. When this bit is set, writing to WR7 (flag register) actually writes to WR7′. If bit D_6 of this register is set to 1, previously unreadable registers WR3, WR4, WR5, and WR10 are readable by the processor. In addition, WR7′ and WR6′ are also readable by having this bit set. WR3 is read when a bogus RR9 register is accessed during a read cycle. WR10 is read by accessing RR11, WR6′ is accessed by executing a read to RR6 and WR7′ is accessed by executing a read to RR14. The Am85C230A register map with bit D_0 of WR15 and bit D_6 of WR7′ set is shown in Table 5.

If both bits D_0 and D_2 of WR15 are set to 1 and D_6 of WR7′ is set to 1, then the Am85C230A register map is as shown in Table 6.

Auto RTS Reset

On the CMOS ESCC, if bit D0 of WR15 and bit D2 of WR7′ are set to 1 and the channel is in SDLC mode, the $\overline{RTS}$ pin may be reset early in the Tx Underrun routine and the $\overline{RTS}$ pin will remain active until the last 0 bit of the closing flag leaves the TxD pin as shown in Figure 18. Note that in order for this to function properly, bits D3 and D2 of WR10 must be set to 1 and 0, respectively.

Table 4. 10×19 Bit FIFO Enabled (D2[WR15] = 1)

$A/\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	(RR0B)
0	1	0	1	WR5B	(RR1B)
0	1	1	0	WR6B	RR6B
0	1	1	1	WR7B	RR7B
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	(RR0A)
1	1	0	1	WR5A	(RR1A)
1	1	1	0	WR6A	RR6A
1	1	1	1	WR7A	RR7A
With the Point High command:					
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR13B
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	(RR15B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	(RR10B)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	(RR13A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	(RR15A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	(RR10A)
1	1	1	1	WR15A	RR15A

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Must Be Set to 0	Ext. Read Enable	Transmit Threshold	$\overline{DTR}/\overline{REQ}$ Fast Mode	Receive Threshold	SDLC/HDLC Auto $\overline{RTS}$ Turnoff	SDLC/HDLC Auto EOM Reset	SDLC/HDLC Auto Tx Flag

WR7′—SDLC/HDLC Programmable Enhancements*

*Note: Options available in D4 and D6 may be used regardless of whether SDLC/HDLC mode is selected.

Table 5. SDLC/HDLC Enhancements Enabled (D0 [WR15] = 1)

A/$\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	RR4B (WR4B)
0	1	0	1	WR5B	RR5B (WR5B)
0	1	1	0	WR6′B	(RR2B) (WR6′B*)
0	1	1	1	WR7′B	(RR3B)
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	RR4A (WR4A)
1	1	0	1	WR5A	RR5A (WR5A)
1	1	1	0	WR6′A	(RR2A) (WR6′A*)
1	1	1	1	WR7′A	(RR3A)
With the Point High command:					
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR9 (WR3B)
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	RR11B (WR10B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	RR14B (WR7′B*)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	RR9A (WR3A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	RR11A (WR10A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	RR14A (WR7′A*)
1	1	1	1	WR15A	RR15A

Note:
*D6 bit of WR7′ is set to 1.

On the Am85C230A, the option of being able to receive the complete CRC characters generated by the transmitter is provided when both bit D_0 of WR15 and bit D_5 of WR7′ are set to 1. When these 2 bits are set and an end-of-frame flag is detected, the last 2 bits of the CRC will be clocked into the Receive Shift Register before its contents are transferred to the Receive Data FIFO. The data-CRC boundary and CRC character bit formats for each Residue Code provided are shown in Figures 19A through 19D for each character length selected.

Table 6. SDLC/HDLC Enhancements and 10×19 Bit FIFO Enabled (D0[WR15]=1, D2[WR15]=1)

A/$\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	RR4B (WR4B)
0	1	0	1	WR5B	RR5B (WR5B)
0	1	1	0	WR6′B	RR6B (WR6′B)*
0	1	1	1	WR7′B	RR7B
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	RR4A (WR4A)
1	1	0	1	WR5A	RR5A (WR5A)
1	1	1	0	WR6′A	RR6A (WR6′A)*
1	1	1	1	WR7′A	RR7A
With the Point High command:					
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR9 (WR3B)
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	RR11B (WR10B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	RR14B (WR7′B)*
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	RR9A (WR3A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	RR11A (WR10A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	RR14A (WR7′A)*
1	1	1	1	WR15A	RR15A

Note:
*D6 bit of WR7′ is set to 1

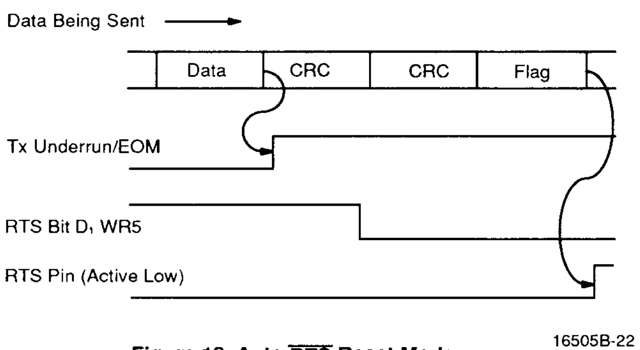

Figure 18. Auto $\overline{RTS}$ Reset Mode

Residue
Code
012
001

D	D	D	D	D	C_0	C_1	C_2
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue
Code
012
101

D	D	D	D	D	D	C_0	C_1
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue
Code
012
100

D	D	D	D	D	D	D	C_0
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue
Code
012
010

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue
Code
012
110

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

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Figure 19A. 5 Bits/Character

Residue Code 012 / 010

D	D	D	D	D	D	C_0	C_1
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 110

D	D	D	D	D	D	D	C_0
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 001

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 101

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 011

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 100

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Figure 19B. 6 Bits/Character 16505B-23

Residue Code
012
111

D	D	D	D	D	D	D	C_0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code
012
100

D	D	D	D	D	D	D	D
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code
012
010

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code
012
110

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code
012
001

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code
012
101

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code
012
011

D	D	D	D	D	D	D	D
D	D	D	D	D	D	C_0	C_1
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

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Figure 19C. 7 Bits/Character

Residue Code 012 / 011

(No Residue)

D	D	D	D	D	D	D	D
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 111

(1 Residue Bit)

D	D	D	D	D	D	D	D
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 000

(2 Residue Bits)

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 100

(3 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 010

(4 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 110

(5 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 001

(6 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	D	C_0	C_1
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 / 101

(7 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	C_0
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

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Figure 19D. 8 Bits/Character

Auto Flag Mode

On the Am85C230A, if bit D_0 of WR15 is set to 1 and the ESCC/LT is programmed for SDLC operation, an option is provided via bit D_0 of WR7′ that eliminates this requirement. If bit D_0 of WR7′ is set to 1 and a character is written to the Transmit Buffer while the transmitter is mark idling, the Mark/Flag Idle bit in WR10 need not be reset to 0 in order to have the opening flag sent because the transmitter will automatically send it before commencing to send data.

In addition, as long as bit D_0 of WR15 and bit D_1 of WR7′ are set to 1, the CRC transmit generator will be automatically preset to the initial state programmed by bit D_7 of WR10 (so the Reset Tx CRC Generator command is also not necessary), and the Tx Underrun/EOM latch will be reset automatically on every new frame sent. This ensures that an opening flag and proper CRC generation and transmission will always be sent without processor intervention under varying bus latency conditions.

Auto Transmit CRC Generator Preset

On the Am85C230A, setting bit D_0 of WR15 to 1 will cause the transmit CRC generator to be preset automatically every time an opening flag is sent, so the Reset Tx CRC Generator Command is not necessary.

Auto Tx Underrun/EOM Latch Reset

On the ESCC/LT, the transmission of the CRC check characters is controlled by the Transmit CRC Enable bit in WR5 (D_0) and the Tx Underrun/EOM bit in RR0 (D_6). However, if the Transmit Enable bit is set to 0 when a transmit underrun (i.e., both the Transmit Buffer and Transmit Shift Register become empty) occurs, the CRC check characters will not be sent regardless of the state of the Tx Underrun/EOM bit.

If the Transmit Enable bit is set to 1 when an underrun occurs, then the state of the Tx Underrun/EOM bit and the Abort/Flag on Underrun bit in WR10 (D_2) determine the action taken by the transmitter. The Abort/Flag on Underrun bit may be set or reset by the processor, whereas the Tx Underrun/EOM bit is set by the transmitter and can only be reset by the processor via the Reset Tx Underrun/EOM Command in WR0.

If the Tx Underrun/EOM bit is set to 1 when an underrun occurs, the transmitter will close the frame by sending a flag; however, if this bit is set to 0, the frame data will be appended with either the accumulated CRC characters followed by a flag or an abort pattern followed by a flag, depending on the state of the Abort/Flag on Underrun bit in the WR10 (D_2). In either case, after the closing flag is sent, the transmitter will idle the transmission line as specified by the Mark/Flag Idle bit D_3 in WR10.

Hence, if the CRC check characters are to be properly appended to a frame, the Abort/Flag on Underrun bit must be set to 0, and the Reset Tx Underrun/EOM Command must be issued after the first but before the last character is written to the Transmit Buffer. This will ensure that either an abort or the CRC will be transmitted if an underrun occurs. Normally, the Abort/Flag on Underrun bit in WR10 should be set to 1 around the same time that the Tx Underrun/EOM bit is reset so that an abort will be sent if the transmitter accidentally underruns, and then set to 0 near the end of the frame to allow the correct transmission of CRC.

On the Am85C230A, if bit D_0 of WR15 is set to 1, the option of having the Tx Underrun/EOM bit reset automatically at the start of every frame is provided via bit D_1 of WR7′. This helps alleviate the software burden of having to respond within one character time when high-speed data are being sent.

SDLC/HDLC NRZI Transmitter Disabling

On the Am85C230A when operating in SDLC mode with NRZI encoding enabled, TxD Pin is forced high.

Complete CRC Receive

In the ESCC/LT, the last 2 bits of the received CRC are properly clocked into the receive shift register and are available to the user.

Interrupt Masking Without $\overline{\text{INTACK}}$

On the Am85C230A, if bit D_5 in WR9 is set to 1, the $\overline{\text{INTACK}}$ cycle does not need to be generated in order to have the IUS bit set. This allows the user to respond to ESCC/LT interrupt requests with a software acknowledgment through RR2. When bit D_5 in WR9 is set and an interrupt occurs, a read to RR2 emulates a hardware Interrupt Acknowledge cycle as it functions in Vectored mode. In this case the CPU must first read RR2 to determine the internal interrupt source and then jump to the appropriate interrupt routine. Reading RR2 sets the IUS bit for the highest priority IP. After the interrupting condition is cleared, the routine can then read RR3 to determine if any other IPs are set and clear them. At the end of the interrupt routine, a Reset IUS command must be issued to unlock the internal daisy chain.

Since the CPU can acknowledge the ESCC/LT of highest priority with a read of its RR2 interrupt vector, there is no need for an external daisy chain. IEI for all ESCC/LT devices should be tied active High. When acknowledging an ESCC/LT interrupt request, the CPU must issue one read to RR2 per interrupt request. The modified interrupt vector can be read from Channel B, or the original vector stored in WR2 can be read from Channel A. Either action will produce the same internal actions on the IUS logic. Note that the No Vector and Vector Includes Status bits in WR9 are ignored when bit D_5 in WR9 is set to 1.

2-Mb/s FM Data Transmission and Reception

The Am85C230A is capable of transmitting and receiving FM-encoded data at the rate of 2 Mb/s. This is accomplished by applying a 32-MHz clock to the $\overline{\text{RTxC}}$ pin and assigning this waveform to drive the Internal Digital Phase-Locked Loop (DPLL) clock. This feature allows the user to send both clock and data information over the same line at 2 Mb/s and can eliminate external DPLLs required for high-speed NRZ data clock generation.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature −65 to +150°C
Voltage at any Pin
Relative to V_{SS} −0.5 to +7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) 0 to +70°C
Supply Voltage (V_{CC}) +5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IH}	Input High Voltage	Commercial	2.2	V_{CC} +0.3*	V
V_{IL}	Input Low Voltage		−0.3*	0.8	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	2.4		V
V_{OH2}	Output High Voltage	I_{OH} = −250 μA	V_{CC} −0.8		V
V_{OL}	Output Low Voltage	I_{OL} = +2.0 mA		0.4	V
I_{IL}	Input Leakage	$0.4\ V \le V_{IN} \le 2.4\ V$		±10.0	μA
I_{OL}	Output Leakage	$0.4\ V \le V_{OUT} \le 2.4\ V$		±10.0	μA
I_{CC1}	V_{CC} Supply Current	8.192 MHz Inputs at		12	mA
		10 MHz voltage rails,		12	mA
		16.384 MHz output unloaded		15	mA
		20 MHz		20	mA
C_{IN}	Input Capacitance	Unmeasured pins returned		10	pF
C_{OUT}	Output Capacitance	to ground = 1 MHz over		15	pF
C_{MO}	Bidirectional Capacitance	specified temperature range		20	pF

*V_{IH} Max and V_{IL} Min not tested. Guaranteed by design.

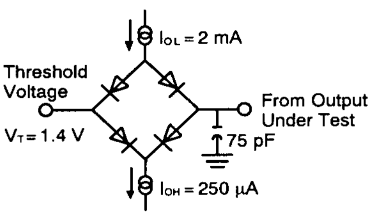
Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

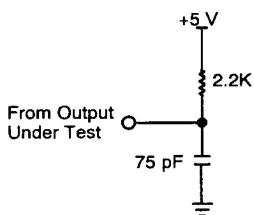
$+4.5\ V \le V_{CC} \le +5.5\ V$
GND = 0 V
$0°C \le T_A \le 70°C$

SWITCHING TEST CIRCUITS

Standard Test Dynamic Load Circuit



Open-Drain Test Load



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SWITCHING CHARACTERISTICS over COMMERCIAL operating range

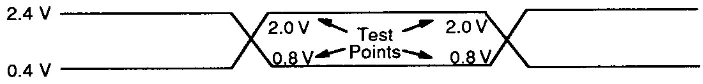
General Timing (see Figure 20)

No.	Parameter Symbol	Parameter Description	8.192 MHz Min.	8.192 MHz Max.	10 MHz Min.	10 MHz Max.	16.384 MHz Min.	16.384 MHz Max.	20 MHz Min.	20 MHz Max.	Unit
1	TdPC(REQ)	PCLK ↓ to $\overline{\text{W/REQ}}$ Valid Delay		250		200		80		70	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		300		180		170	ns
3	TsRXC(PC)	$\overline{\text{RxC}}$ ↑ to PCLK ↑ Setup Time (Notes 1, 4 & 8)	NA	NA	NA	NA	NA	NA	NA	NA	ns
4	TsRXD(RXCr)	RxD to $\overline{\text{RxC}}$ ↑ Setup Time (XI Mode) (Note 1)	0		0		0		0		ns
5	ThRXD(RXCr)	RxD to $\overline{\text{RxC}}$ ↑ Hold Time (XI Mode) (Note 1)	150		125		50		45		ns
6	TsRXD(RXCf)	RxD to $\overline{\text{RxC}}$ ↓ Setup Time (XI Mode) (Notes 1, 5)	0		0		0		0		ns
7	ThRXD(RXCf)	RxD to $\overline{\text{RxC}}$ ↓ Hold Time (XI Mode) (Notes 1, 5)	150		125		50		45		ns
8	TsSY(RXC)	$\overline{\text{SYNC}}$ to $\overline{\text{RxC}}$ ↑ Setup Time (Note 1)	−200		−150		−100		−90		ns
9	ThSY(RXC)	$\overline{\text{SYNC}}$ to $\overline{\text{RxC}}$ ↑ Hold Time (Note 1)	5TcPc		5TcPc		5TcPc		5TcPc		ns
10	TsTXC(PC)	$\overline{\text{TxC}}$ ↓ to PCLK ↑ Setup Time (Notes 2, 4 & 8)	NA		NA		NA		NA		
11	TdTXCf(TXD)	$\overline{\text{TxC}}$ ↓ to TxD Delay (XI Mode) (Note 2)		200		150		80		70	ns
12	TdTXCr(TXD)	$\overline{\text{TxC}}$ ↑ to TxD Delay (XI Mode) (Notes 2, 5)		200		150		80		70	ns
13	TdTXD(TRX)	TxD to $\overline{\text{TRxC}}$ Delay (Send Clock Echo)		200		140		80		70	ns
14a	TwRTXh	$\overline{\text{RTxC}}$ High Width (Note 6)	150		120		80		70		ns
14b	TwRTxh(E)	$\overline{\text{RTxC}}$ High Width (Note 9)	50		40		15.6		15.6		ns
15a	TwRTXl	$\overline{\text{RTxC}}$ Low Width (Note 6)	150		120		80		70		ns
15b	TwRTXl(E)	$\overline{\text{RTxC}}$ Low Width (Note 9)	50		40		15.6		15.6		ns
16a	TcRTX	$\overline{\text{RTxC}}$ Cycle Time (Notes 6, 7)	488		400		244		200		ns
16b	TcRTx(E)	$\overline{\text{RTxC}}$ Cycle Time (Note 9)	125		100		31.25		31.25		ns
17	TcRTXX	Crystal Oscillator Period (Note 3)	125	1000	100	1000	61	1000	61	1000	ns
18	TwTRXh	$\overline{\text{TRxC}}$ High Width (Note 6)	150		120		80		70		ns
19	TwTRXl	$\overline{\text{TRxC}}$ Low Width (Note 6)	150		120		80		70		ns
20	TcTRX	$\overline{\text{TRxC}}$ Cycle Time (Notes 6, 7)	488		400		244		200		ns
21	TwEXT	$\overline{\text{DCD}}$ or $\overline{\text{CTS}}$ Pulse Width	200		120		70		60		ns
22	TwSY	$\overline{\text{SYNC}}$ Pulse Width	200		120		70		60		ns

Notes:

1. $\overline{\text{RxC}}$ is $\overline{\text{RTxC}}$ or $\overline{\text{TRxC}}$, whichever is supplying the receive clock.
2. $\overline{\text{TxC}}$ is $\overline{\text{TRxC}}$ or $\overline{\text{RTxC}}$, whichever is supplying the transmit clock.
3. Both $\overline{\text{RTxC}}$ and $\overline{\text{SYNC}}$ have 30-pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between $\overline{\text{RxC}}$ and PCLK or $\overline{\text{TxC}}$ and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.
8. External PCLK to $\overline{\text{RxC}}$ or $\overline{\text{TxC}}$ synchronization requirement eliminated for PCLK divide-by-four operation. $\overline{\text{TRxC}}$ and $\overline{\text{RTxC}}$ rise and fall times are identical to PCLK. Reference timing specs Tfpc and Trpc. Tx and Rx input clock slow rates should be kept to a maximum of 30 ns. All parameters related to input CLK edges should be referenced at the point at which the transition begins or ends, whichever is the worst case.
9. ENHANCED FEATURE—$\overline{\text{RTxC}}$ used as input to internal DPLL only.

SWITCHING TEST INPUT/OUTPUT WAVEFORM



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AC testing: Inputs are driven at 2.4 V for a logic 1 and 0.4 V for a logic 0.
Timing measurements are made at 2.0 V for a logic 1 and 0.8 V for logic 0.

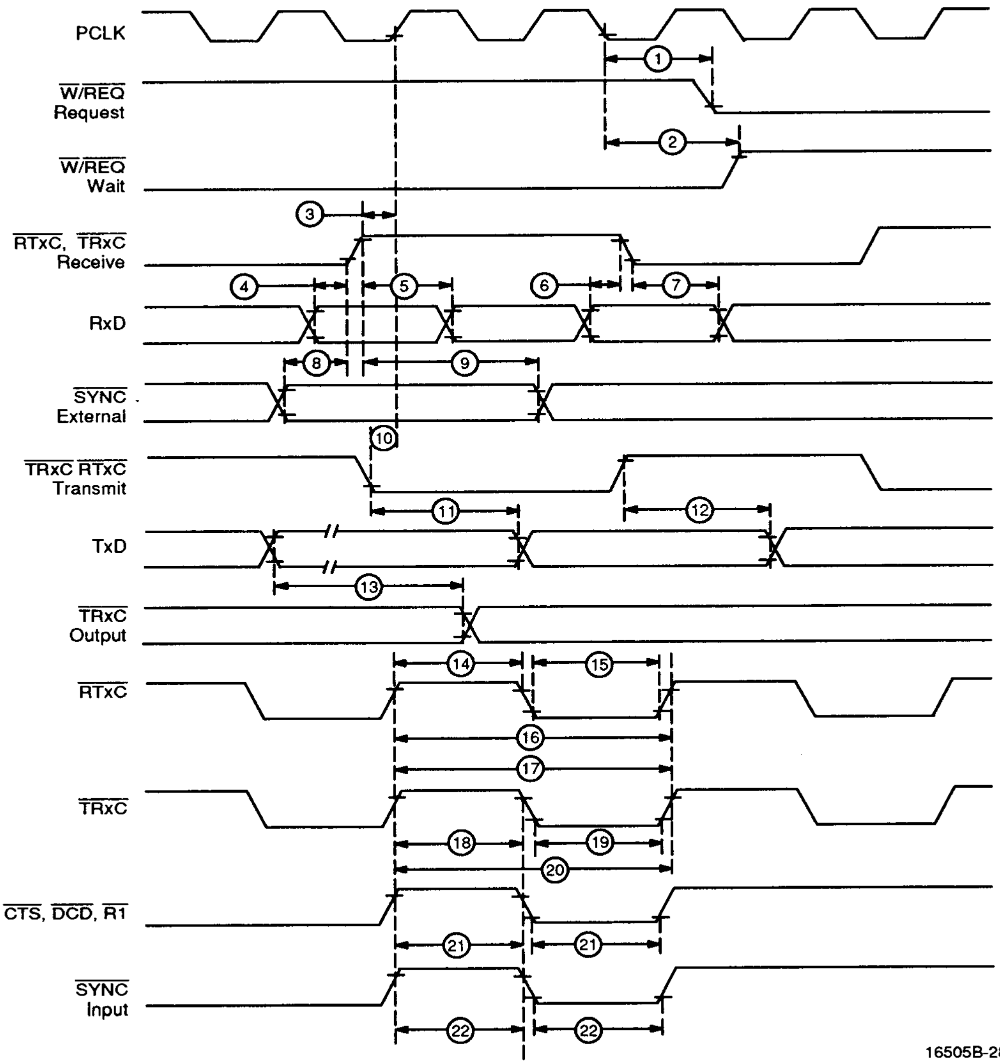

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Figure 20. General Timing

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

System Timing (see Figure 21)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		Unit
			Min.	Max.	Min.	Max.	
1	TdRXC(REQ)	$\overline{\mathrm{RXC}}$ ↑ $\overline{\mathrm{W/REQ}}$ Valid Delay (Note 2)	8	12	8	12	TcPc
2	TdRXC(W)	$\overline{\mathrm{RXC}}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	12	8	12	TcPc
3	TdRXC(SY)	$\overline{\mathrm{RxC}}$ ↑ to $\overline{\mathrm{SYNC}}$ Valid Delay (Note 2)	4	7	4	7	TcPc
4	TdRXC(INT)	$\overline{\mathrm{RxC}}$ ↑ to $\overline{\mathrm{INT}}$ Valid Delay (Notes 1, 2)	10	16	10	16	TcPc
5	TdTXC(REQ)	$\overline{\mathrm{TxC}}$ ↑ to $\overline{\mathrm{W/REQ}}$ Valid Delay (Note 3)	5	8	5	8	TcPc
6	TdTXC(W)	$\overline{\mathrm{TxC}}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	5	11	TcPc
7a	TdTXC(DRQ)	$\overline{\mathrm{TxC}}$ ↓ to $\overline{\mathrm{DTR/REQ}}$ Valid Delay (Note 3)	4	7	4	7	TcPc
7b	TdTXC(EDRQ)	$\overline{\mathrm{TxC}}$ ↓ to $\overline{\mathrm{DTR/REQ}}$ Valid Delay (Notes 3, 4)	5	8	5	8	TcPc
8	TdTXC(INT)	$\overline{\mathrm{TxC}}$ ↓ to $\overline{\mathrm{INT}}$ Valid Delay (Notes 1, 3)	6	10	6	10	TcPc
9	TdSY(INT)	$\overline{\mathrm{SYNC}}$ Transition to $\overline{\mathrm{INT}}$ Valid Delay (Note 1)	2	6	2	6	TcPc
10	TdEXT(INT)	$\overline{\mathrm{DCD}}$ or $\overline{\mathrm{CTS}}$ Transition to $\overline{\mathrm{INT}}$ Valid Delay (Note 1)	2	6	2	6	TcPc

No.	Parameter Symbol	Parameter Description	16.384 MHz		20 MHz		Unit
			Min.	Max.	Min.	Max.	
1	TdRXC(REQ)	$\overline{\mathrm{RXC}}$ ↑ $\overline{\mathrm{W/REQ}}$ Valid Delay (Note 2)	8	12	8	12	TcPc
2	TdRXC(W)	$\overline{\mathrm{RXC}}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	14	8	14	TcPc
3	TdRXC(SY)	$\overline{\mathrm{RxC}}$ ↑ to $\overline{\mathrm{SYNC}}$ Valid Delay (Note 2)	4	7	4	7	TcPc
4	TdRXC(INT)	$\overline{\mathrm{RxC}}$ ↑ to $\overline{\mathrm{INT}}$ Valid Delay (Notes 1, 2)	10	16	10	16	TcPc
5	TdTXC(REQ)	$\overline{\mathrm{TxC}}$ ↓ to $\overline{\mathrm{W/REQ}}$ Valid Delay (Note 3)	5	8	5	8	TcPc
6	TdTXC(W)	$\overline{\mathrm{TxC}}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	5	11	TcPc
7a	TdTXC(DRQ)	$\overline{\mathrm{TxC}}$ ↓ to $\overline{\mathrm{DTR/REQ}}$ Valid Delay (Note 3)	4	7	4	7	TcPc
7b	TdTXC(EDRQ)	$\overline{\mathrm{TxC}}$ ↓ to $\overline{\mathrm{DTR/REQ}}$ Valid Delay (Notes 3, 4)	5	8	5	8	TcPc
8	TdTXC(INT)	$\overline{\mathrm{TxC}}$ ↓ to $\overline{\mathrm{INT}}$ Valid Delay (Notes 1, 3)	6	10	6	10	TcPc
9	TdSY(INT)	$\overline{\mathrm{SYNC}}$ Transition to $\overline{\mathrm{INT}}$ Valid Delay (Note 1)	2	6	2	6	TcPc
10	TdEXT(INT)	$\overline{\mathrm{DCD}}$ or $\overline{\mathrm{CTS}}$ Transition to $\overline{\mathrm{INT}}$ Valid Delay (Note 1)	2	6	2	6	TcPc

Notes:
1. Open-drain output, measured with open-drain test load.
2. $\overline{\mathrm{RxC}}$ is $\overline{\mathrm{RTxC}}$ or $\overline{\mathrm{TRxC}}$, whichever is supplying the receive clock.
3. $\overline{\mathrm{TxC}}$ is $\overline{\mathrm{TRxC}}$ or $\overline{\mathrm{RTxC}}$, whichever is supplying the transmit clock.
4. Parameter applies to Enhanced Request mode only.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

Read and Write Timing (see Figure 22)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		16.384 MHz		20 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TwPCl	PCLK Low Width	50	2000	40	1000	26	1000	22	1000	ns
2	TwPCh	PCLK High Width	50	2000	40	1000	26	1000	22	1000	ns
3	TfPC	PCLK Fall Time		15		10		5		5	ns
4	TrPC	PCLK Rise Time		15		10		5		5	ns
5	TcPC	PCLK Cycle Time	122	4000	100	2000	61	2000	50	2000	ns
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	70		50		35		30		ns
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		0		0		ns
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	70		50		35		30		ns
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		0		0		ns
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	20		20		15		15		ns
11	TsIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time (Note 1)	145		130		70		65		ns
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		0		0		ns
13	TsIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time (Note 1)	145		130		70		65		ns
14	ThIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		0		0		ns
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	40		30		15		15		ns
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		0		0		ns
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		0		0		ns
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	60		50		30		25		ns
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time (Note 1)	0		0		0		0		ns
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time (Note1)	0		0		0		0		ns
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time (Note 1)	60		50		30		25		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	150		125		75		65		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		0		0		ns
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		0		0		ns
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		140		120		70		65	ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		40		35		20		20	ns

Notes:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time at which the data bus is released from its drive state with a maximum DC load and minimum AC load.

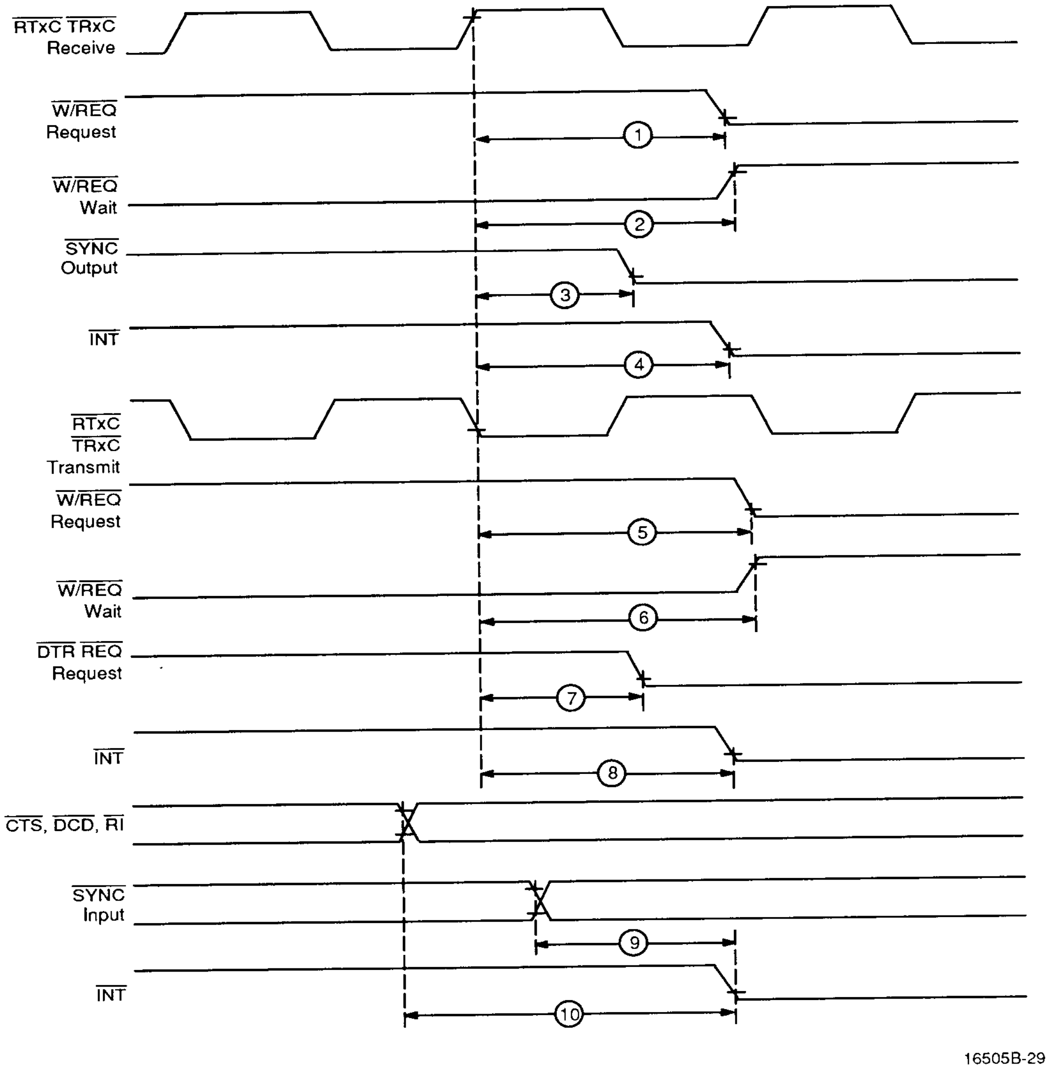


Figure 21. System Timing

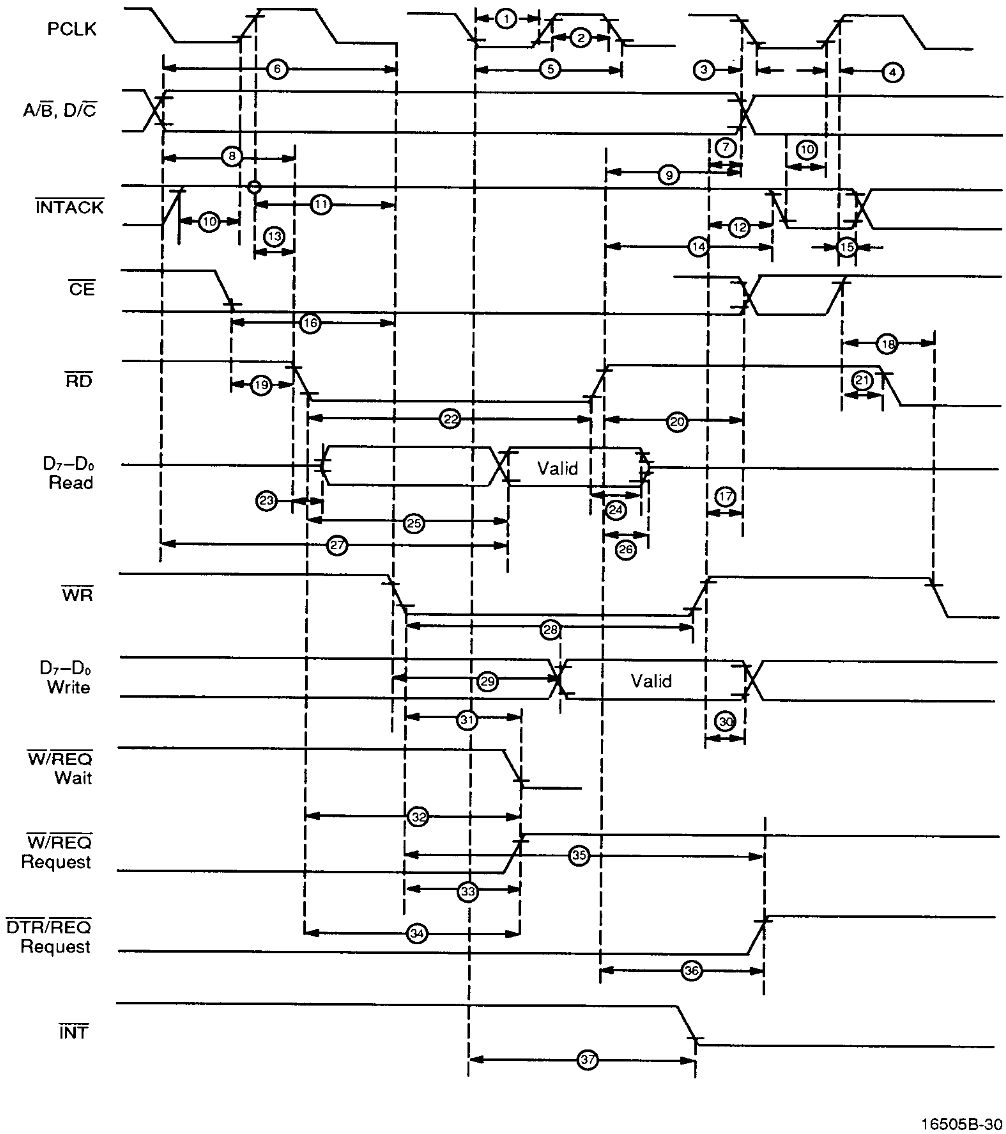


Figure 22. Read and Write Timing

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

Interrupt Acknowledge Timing, Reset Timing, Cycle Timing (see Figures 23–25)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		16.384 MHz		20 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		220		180		100		90	ns
28	TwWRl	$\overline{WR}$ Low Width	150		125		75		65		ns
29	TdWRf(DW)	$\overline{WR}$ ↓ to Write Data Valid		35		20		20		20	ns
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		0		0		0		ns
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay (Note 2)		170		100		50		50	ns
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay (Note 2)		170		100		50		50	ns
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		170		120		70		65	ns
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		170		120		70		65	ns
35a	TdWRr(REQ)	$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		4TcPc		4TcPc		4TcPc		4TcPc	ns
35b	TdWRr(EREQ)	$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		120		100		70		65	ns
36	TdRDr(REQ)	$\overline{RD}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		NA		NA		NA		NA	ns
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay (Note 2)		500		320		175		160	ns
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay (Note 3)	150		90		50		45		ns
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	150		125		75		65		ns
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		140		120		70		60	ns
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time	95		80		50		45		ns
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	0		0		0		0		ns
43	TdIEI(IEO)	IEI to IEO Delay Time		95		90		45		40	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay		200		175		80		70	ns
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 2)		450		320		200		180	ns
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	15		15		10		10		ns
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	15		15		10		10		ns
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	150		100		75		65		ns
49	Trc	Valid Access Recovery Time (Note 1)	3.5		4		4		4		TcPc

Notes:

1. Parameter applies only between transactions involving the ESCC/LT, if $\overline{WR/RD}$ falling edge is synchronized to PCLK falling edge, then TrC = 3TcPc.
2. Open-drain output, measured with open-drain test load.
3. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of DdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEI(IEO) for each device separating them in the daisy chain.
4. Parameter applies to Enhanced Request mode only.

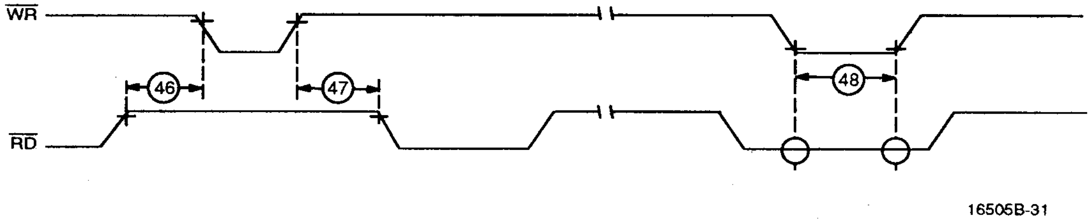


Figure 23. Reset Timing

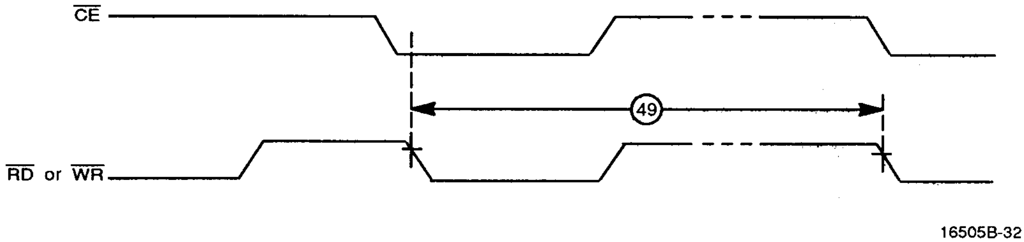


Figure 24. Cycle Timing

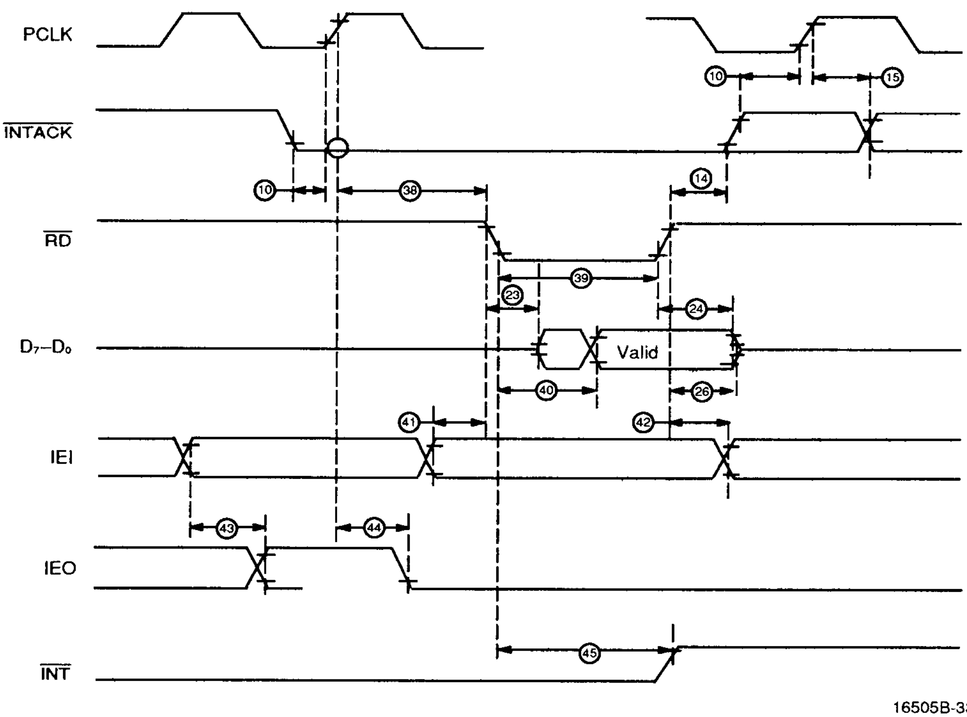
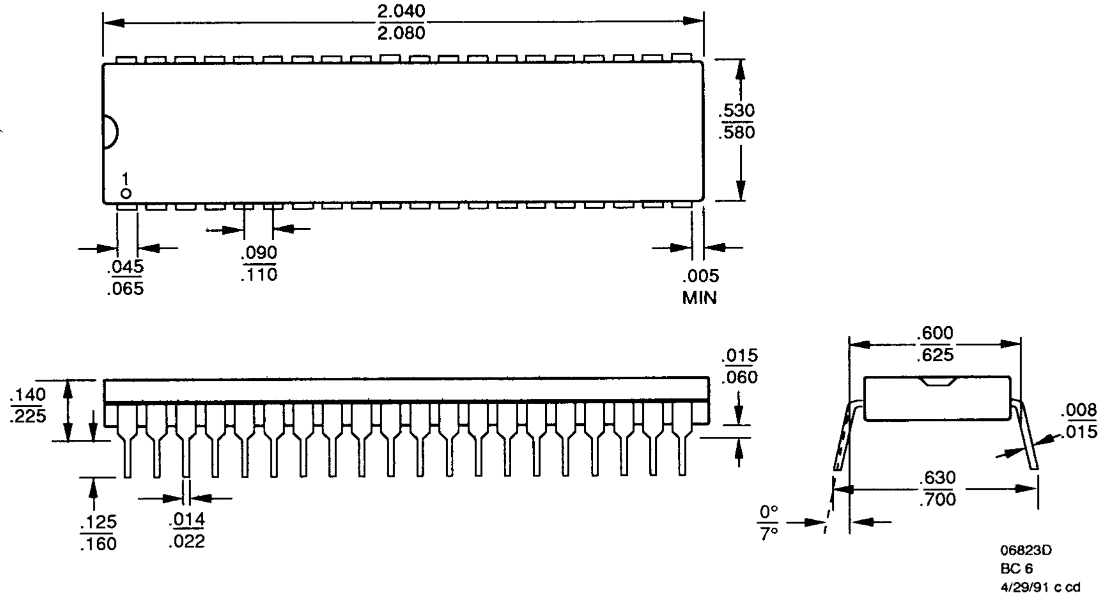
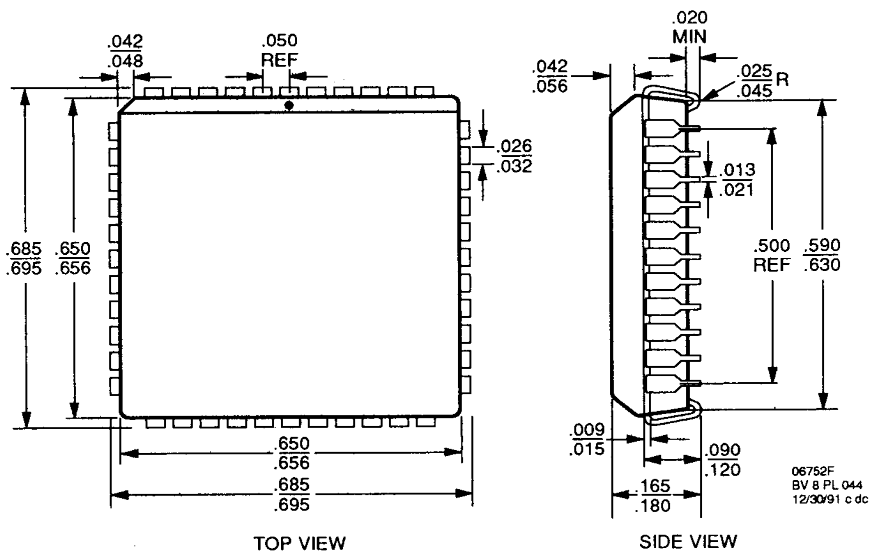


Figure 25. Interrupt Acknowledge Timing

PHYSICAL DIMENSIONS*
PD 040



PL 044



* For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

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