mosaic
semiconductor, inc.

PUMA 3F16006-90/12/15

512K x 32 FLASH MODULE

Issue 4.0 August 1995

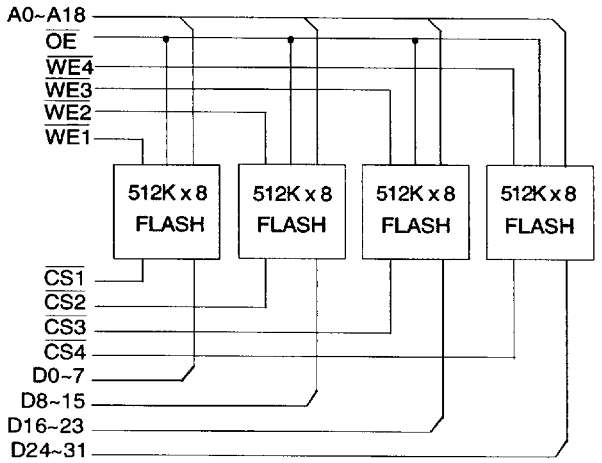
Description

The PUMA 3F16006 is a 16 Megabit CMOS 5.0V only FLASH Module in a 66 pin PGA package, which is configurable as 8, 16, 32 bit wide using CE1-4. Access times of 90, 120 and 150 ns are available. Flash memory combines the functionality of EEPROM with the on board electrical Write/Erasure, which reliably stores data even after 100,000 cycles. The PUMA 3F16006 utilises devices which incorporate Automatic Programming and Erase by Embedded Algorithms. In addition Sector Erase architecture can erase any of the 64K sectors of data randomly and supports full chip erase. The device also features hardware sector protection, which disables both program and erase operations in any of the 32 sectors on the module.

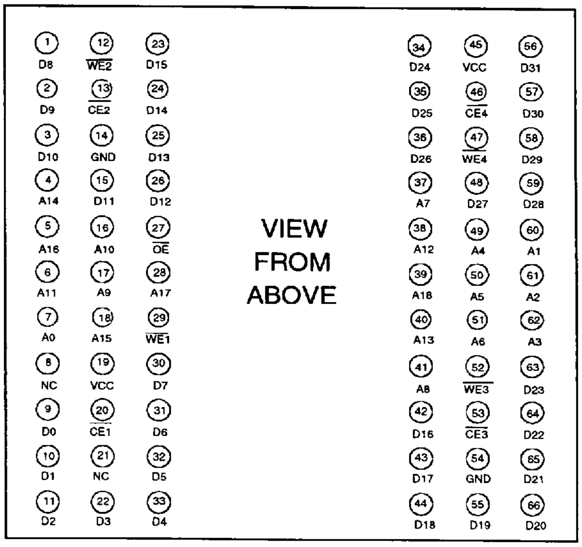
Features

- 16 Megabit FLASH module.
- Fast Access Times of 90/120/150 ns.
- Output Configurable as 32 / 16 / 8 bit wide.
- Operating Power 880/451/237 mW (max).
  Low Power Standby 2.2mW (max).
- Automatic Write/Erase by Embedded Algorithm - end of Write/Erase indicated by DATA Polling and Toggle Bit.
- Flexible Sector Erase Architecture - 64K byte sector size, with hardware protection of any number of sectors.
- Single Byte Program of 16µs (min.), Sector Program time of 1 sec. (typ.).
- Erase/Write Cycle Endurance 100,000 (min.)

Block Diagram



Pin Definition



Pin Functions

A0-A18	Address Input	D0-D31	Data Inputs/Outputs
CE1-4	Chip Enables	WE1-4	Write Enables
OE	Output Enable	Vcc	Power (+5V)
GND	Ground		

6353379 0002814 474

Absolute Maximum Ratings ⁽¹⁾

	max	unit
Voltage on any pin w.r.t. Gnd	-2.0 to +7	V
Supply Voltage ⁽²⁾	-2.0 to +7	V
Voltage on A9 w.r.t. Gnd ⁽³⁾	-2.0 to +14	V
Storage Temperature	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operationof the device at those or any other conditions above those indicated in the operational sections of this specification is not implied.

(2) Minimum DC voltage on any input or I/O pin is -0.5V. Maximum DC voltage on output and I/O pins is Vcc+0.5V During transitions voltage may overshoot by +/-2V for upto 20ns

(3) Minimum DC input voltage on A9 is -0.5V during voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20ns, maximum DC input voltage in A9 is 13.5V which may overshoot to 14.0V for periods up to 20ns

Recommended Operating Conditions

parameter		min	typ	max	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	0.7V_{CC}	-	V_{CC}+0.3	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (-I suffix)

Parameter		Symbol	Test Condition	min	typ	max	Unit
I/P Leakage Current	Address, $\overline{OE}$	I_{LI}	V_{CC}=V_{CC} max, V_{IN}=0V or V_{CC}	-	-	±4	µA
A9 Input Leakage Current		I_{LI1}	V_{CC}=V_{CC} max, A9=12.5V	-	-	200	µA
	Other Pins	I_{LI2}	V_{CC}=V_{CC} max, V_{IN}=0V or V_{CC}	-	-	±1	µA
Output Leakage Current		I_{LO}	V_{CC}=V_{CC} max, V_{OUT}=0V or V_{CC}	-	-	±4	µA
V_{CC} Operating Current	32 bit	I_{CCO32}	CE=V_{IL} ⁽¹⁾, $\overline{OE}$=V_{IH},I_{OUT}=0mA, f=6MHz	-	-	160	mA
	16 bit	I_{CCO16}	As above	-	-	82	mA
	8 bit	I_{CCO8}	As above	-	-	43	mA
V_{CC} Program/Erase Current	32 bit	I_{CCP32}	Programming in Progress	-	-	240	mA
	16 bit	I_{CCP16}	As above	-	-	122	mA
	8 bit	I_{CCP8}	As above	-	-	63	mA
Standby Supply Current		I_{SB1}	V_{CC}=V_{CC} max, $\overline{CE}$=V_{IH} ⁽¹⁾ $\overline{OE}$ = V_{IH}	-	-	4	mA
Autoselect / Sector Protect Voltage		V_{ID}	V_{CC} = 5.0V	11.5	-	12.5	V
Voltage for Sector Unprotect		V_{SP}	V_{CC} = 5.0V	9.5	-	10.5	V
Output Low Voltage		V_{OL}	I_{OL}=12mA. V_{CC} = V_{CC} min.	-	-	0.45	V
Output High Voltage		V_{OH1}	I_{OH}=-2.5mA. V_{CC} = V_{CC} min.	2.4	-	-	V
Low V_{CC} Lock-Out Voltage		V_{LKO}		3.2	-	4.2	V

Notes (1) $\overline{CE}$ above are accessed through CE1-4. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

Capacitance (T_A=25°C, f=1MHz)

Parameter		Symbol	Test Condition	typ	max	Unit
Input Capacitance	Address, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	30	pF
	Other pins	C_{IN2}	V_{IN}=0V	-	36	pF
Output Capacitance	32 bit	C_{OUT32}	V_{OUT}=0V	-	48	pF

Note: These parameters are calculated, not measured.

AC OPERATING CONDITIONS

Read Cycle

Parameter		90			120			150			
		min	typ	max	min	typ	max	min	typ	max	Unit
Read Cycle Time	tRC	90	-	-	120	-	-	150	-	-	ns
Address to output delay	tACC	-	-	90	-	-	120	-	-	150	ns
Chip enable to output	tCE	-	-	90	-	-	120	-	-	150	ns
Output enable to output	tOE	-	-	35	-	-	50	-	-	55	ns
Output enable to output High Z	tDF	-	-	20	-	-	30	-	-	35	ns
Output hold time from address CE or OE whichever occurs first	toH	0	-	-	0	-	-	0	-	-	ns

Write/Erase/Program

Parameter	symbol	90			120			150			
		min	typ	max	min	typ	max	min	typ	max	unit
Write Cycle time (4)	t_{WC}	90	-	-	120	-	-	150	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	45	-	-	50	-	-	50	-	-	ns
Data Setup Time	t_{DS}	45	-	-	50	-	-	50	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHWL}	0	-	-	0	-	-	0	-	-	ns
CE setup time	t_{CE}	0	-	-	0	-	-	0	-	-	ns
CE hold time	t_{CH}	0	-	-	0	-	-	0	-	-	ns
WE Pulse Width	t_{WP}	45	-	-	50	-	-	50	-	-	ns
WE Pulse Width High	t_{WPH}	20	-	-	20	-	-	20	-	-	ns
Programming operation	t_{WHWH1}	-	16	-	-	16	-	-	16	-	µs
Sector Erase operation (1)	t_{WHWH2}	-	1	30	-	1	30	-	1	30	sec
Chip Erase operation (1)	t_{WHWH2}	-	8	-	-	8	-	-	8	-	sec
Vcc setup time (4)	t_{VCS}	50	-	-	50	-	-	50	-	-	µs
Voltage Transition Time (2,4)	t_{VLHT}	4	-	-	4	-	-	4	-	-	µs
Write Pulse Width 1 (2)	t_{WPP1}	100	-	-	100	-	-	100	-	-	µs
Write Pulse Width 2 (2)	t_{WPP2}	10	-	-	10	-	-	10	-	-	ms
OE setup to WE active (2,4)	t_{OESP}	4	-	-	4	-	-	4	-	-	µs
CE setup to WE active (3,4)	t_{CSP}	4	-	-	4	-	-	4	-	-	µs

Notes: (1) This does not include the preprogramming time.
(2) These timings are for Sector Protect/Unprotect operations.
(3) This timing is only for Sector Unprotect.
(4) Not 100% tested.

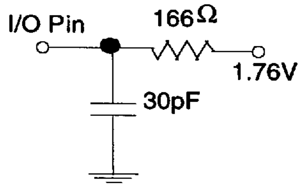
Write/Erase/Program Alternate $\overline{CE}$ controlled Writes

Parameter	symbol	90			120			150			
		min	typ	max	min	typ	max	min	typ	max	unit
Write Cycle time (2)	t_{WC}	90	-	-	120	-	-	150	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	45	-	-	50	-	-	50	-	-	ns
Data Setup Time	t_{DS}	45	-	-	50	-	-	50	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	0	-	-	ns
$\overline{\text{Read}}$ Recover before Write	t_{GHEL}	0	-	-	0	-	-	0	-	-	ns
$\overline{WE}$ setup time	t_{WS}	0	-	-	0	-	-	0	-	-	ns
$\overline{WE}$ hold time	t_{WH}	0	-	-	0	-	-	0	-	-	ns
$\overline{CE}$ Pulse Width	t_{CP}	45	-	-	50	-	-	50	-	-	ns
CE Pulse Width High	t_{CPH}	20	-	-	20	-	-	20	-	-	ns
Programming operation	t_{WHWH1}	-	16	-	-	16	-	-	16	-	us
Sector Erase operation (1)	t_{WHWH2}	-	1	30	-	1	30	-	1	30	sec
Chip Erase operation (1)	t_{WHWH2}	-	8	-	-	8	-	-	8	-	sec
Vcc setup time (2)	t_{VCE}	-	50	-	-	50	-	-	50	-	us

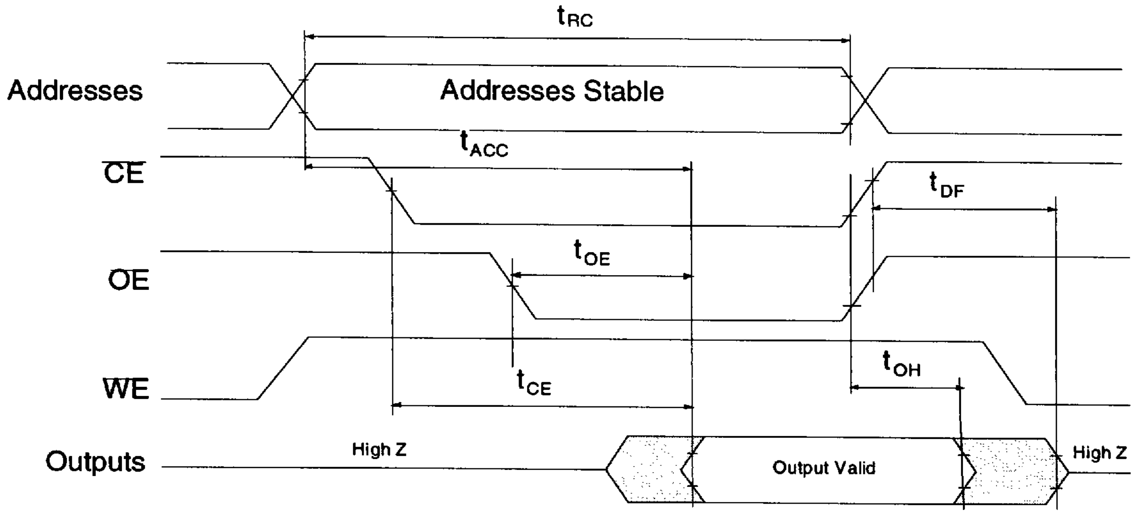
Note: (1) Does not include pre-programming time.
(2) Not 100% tested.

AC Test Conditions

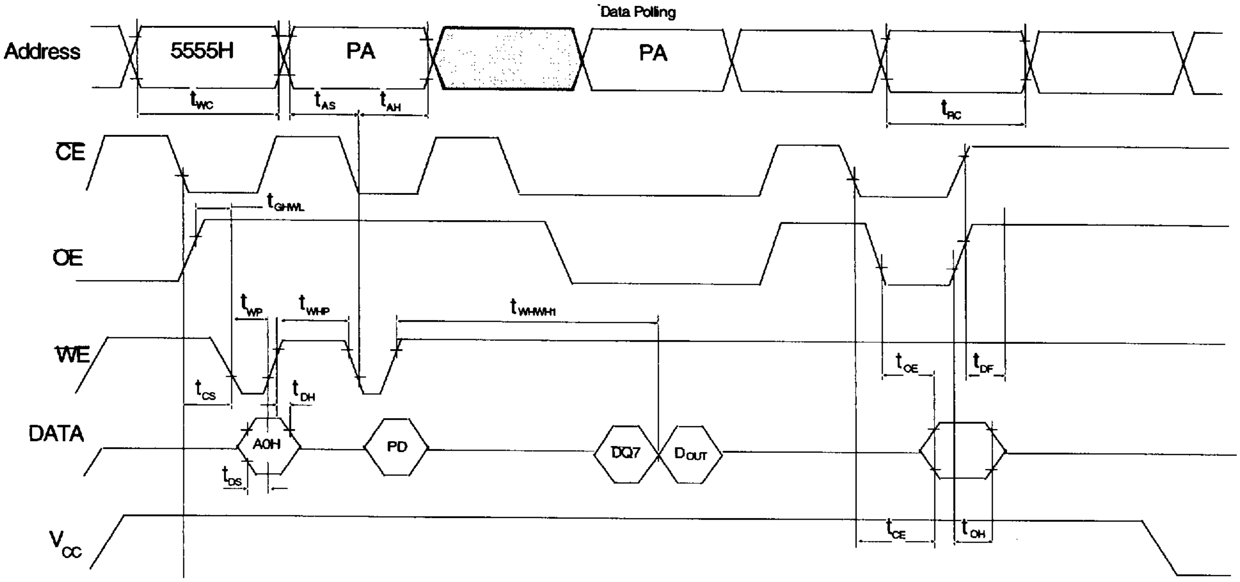
- * Input pulse levels : 0.0V to 3.0V
- * Input rise and fall times : 5 ns
- * Input and output timing reference levels : 1.5V
- * VCC = 5V +/- 10%
- * Module tested in 32 bit mode



AC Waveforms for Read Operation



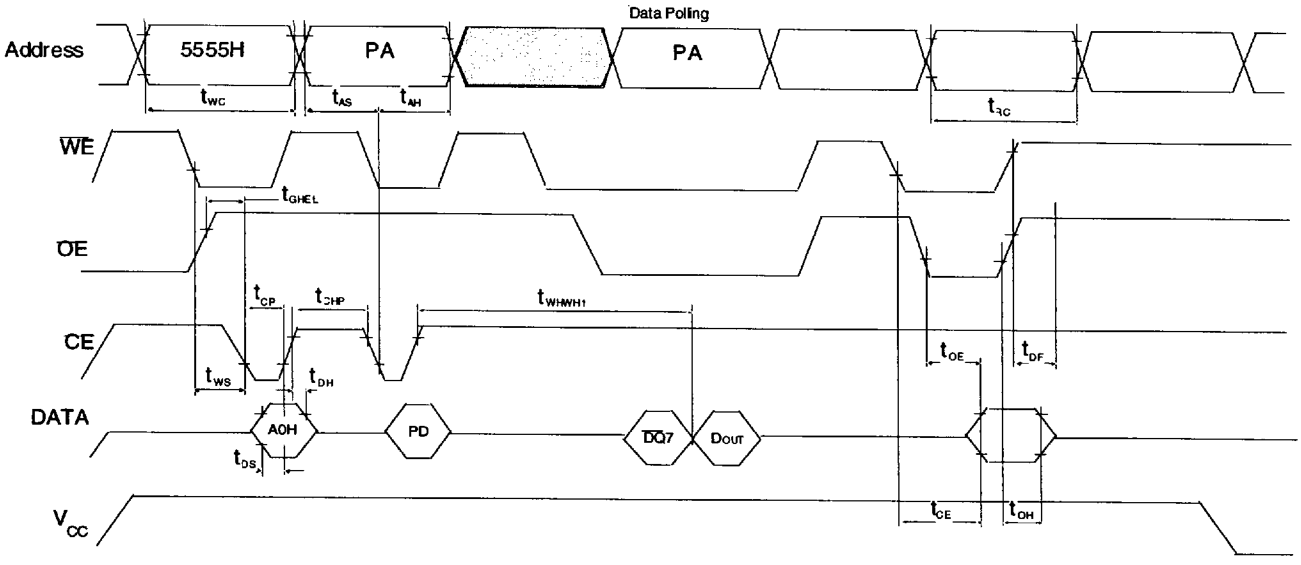
AC Waveforms Program



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the out put of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

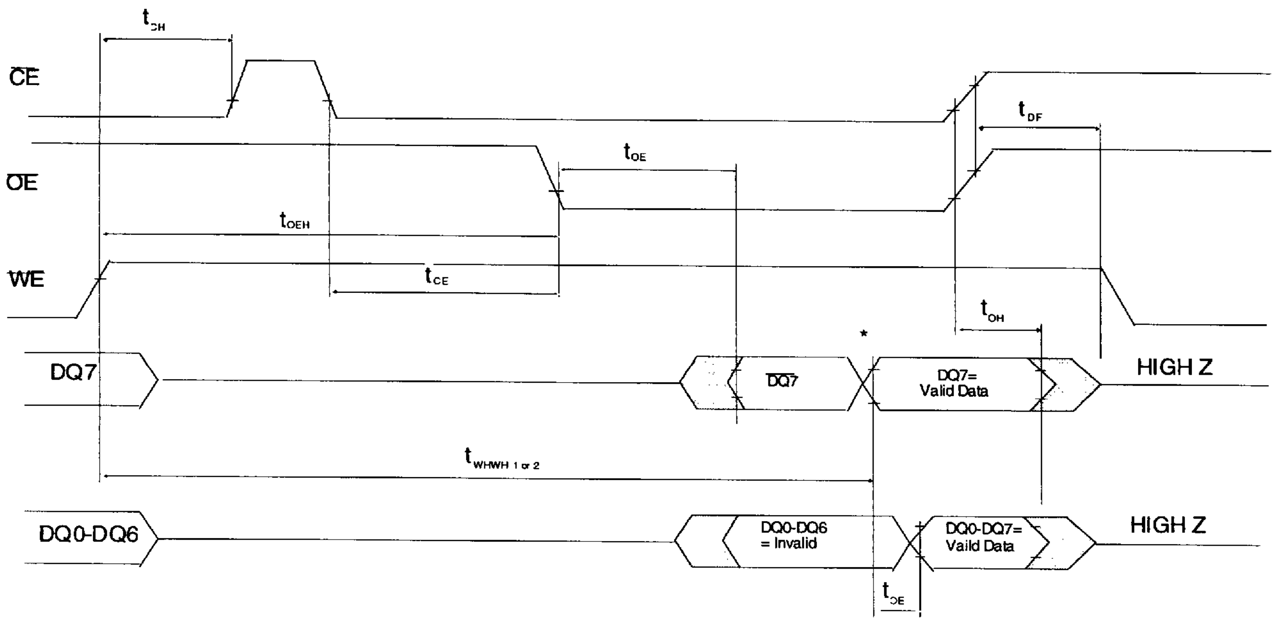
A.C Waveforms - Alternate CE controlled Program operation timings



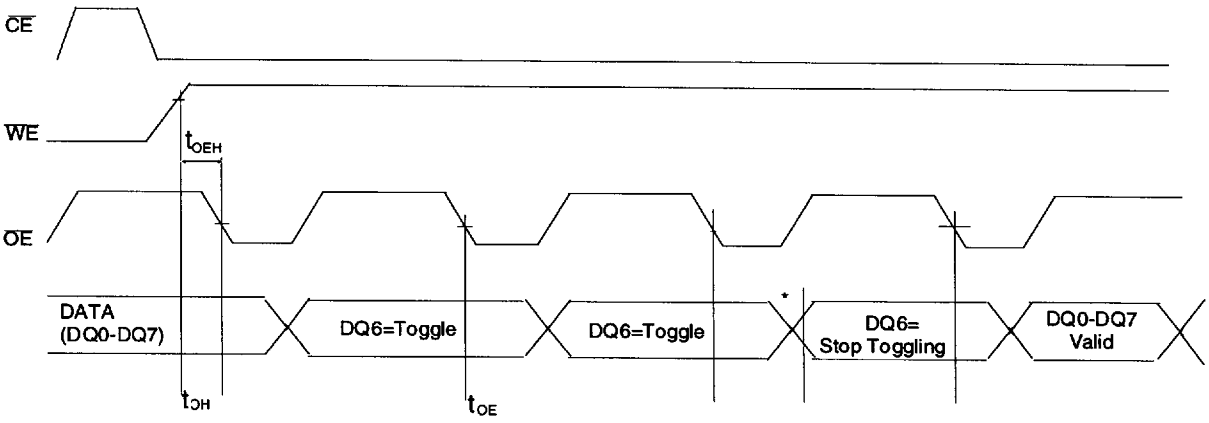
NOTES:

1. PA is address of memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC Waveforms for Data Polling During Embedded Algorithm Operations

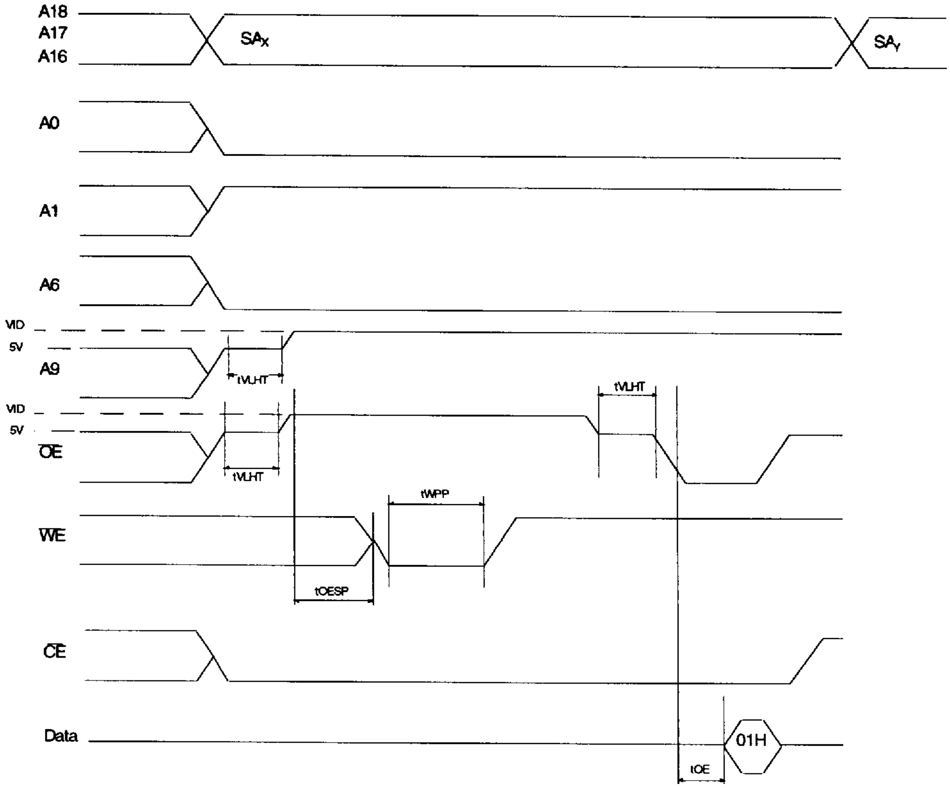


AC Waveforms for Toggle Bit During Embedded Algorithm Operations



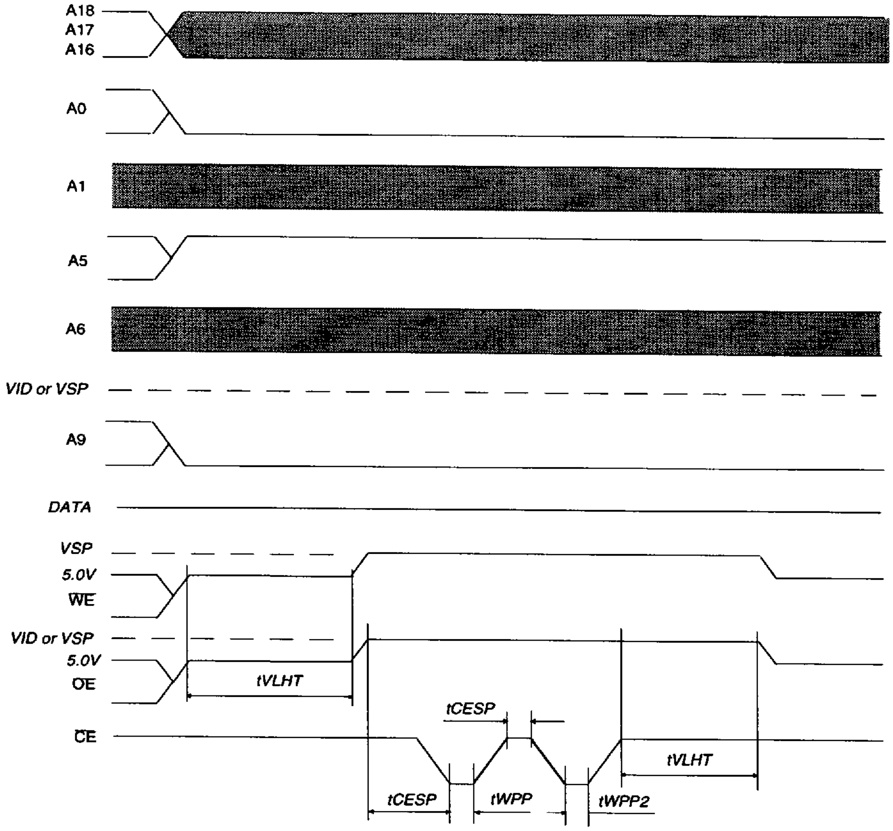
* DQ6 stops toggling (the device has completed the embedded operations)

AC Waveforms For Sector Protection

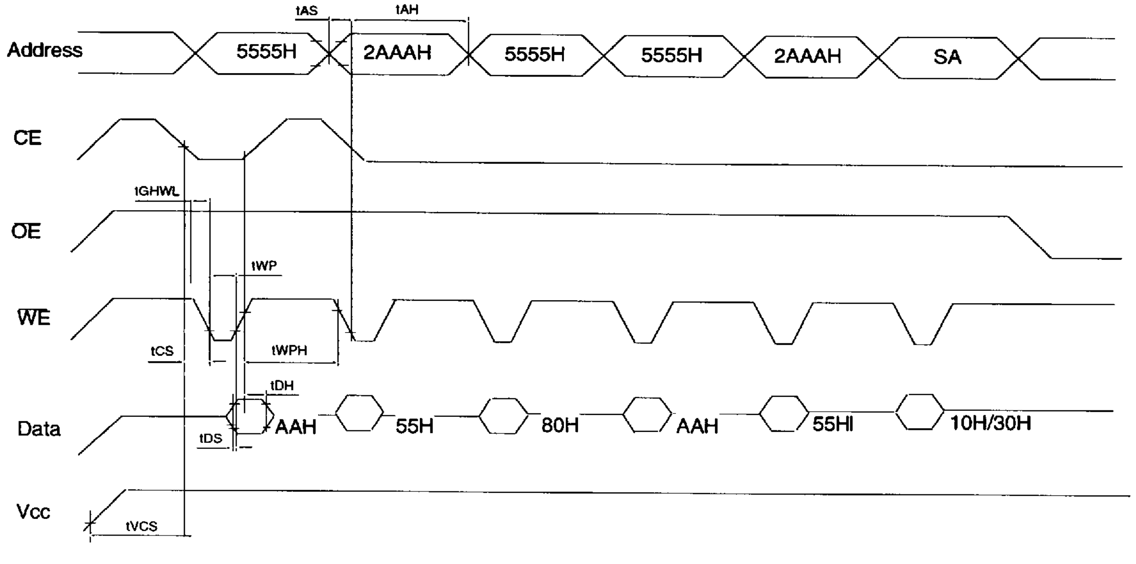


SA_X = sector Addr for intial sector
SA_Y = sector Addr for next sector

AC Waveforms for Sector Unprotect



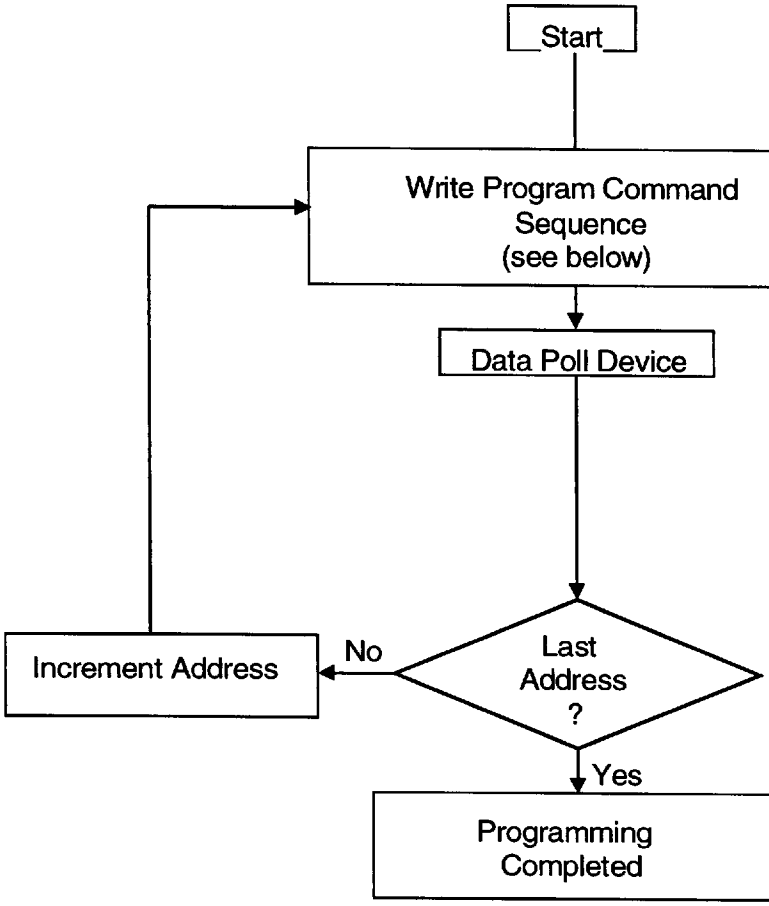
AC Waveforms Chip / Sector Erase



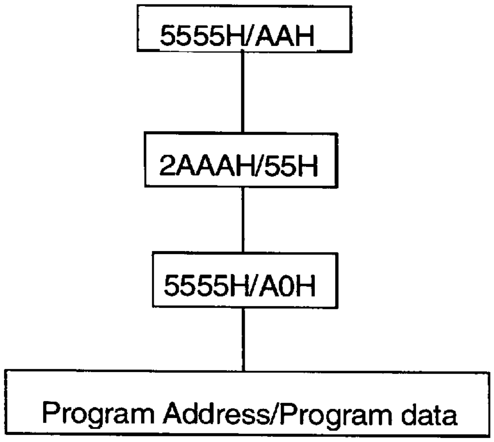
NOTES:

1. SA is the address for sector erase. Addresses = don't care for Chip Erase.

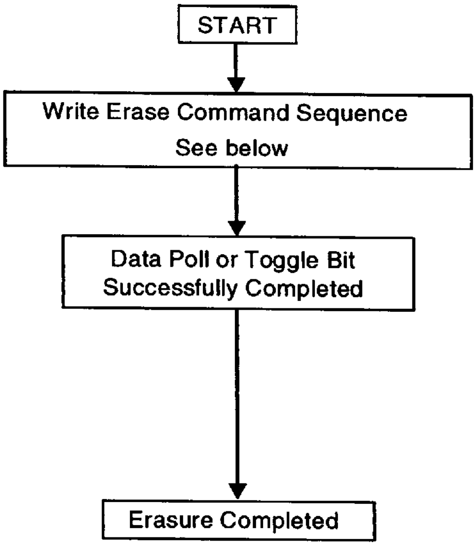
EMBEDDED PROGRAMMING ALGORITHM



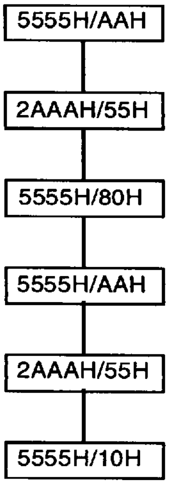
Program Command Sequence (Address /Command)



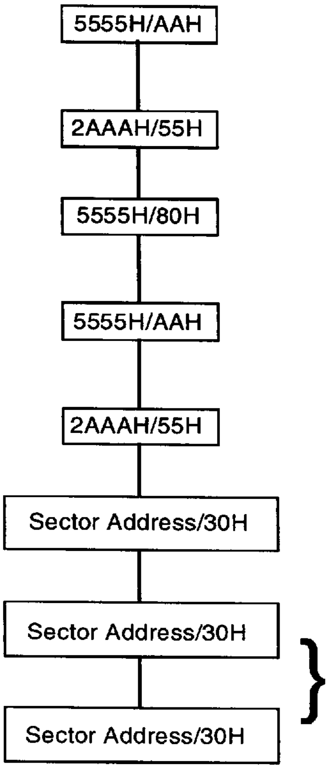
EMBEDDED ERASE ALGORITHM



Chip Erase Command Sequence
(Address/Command):

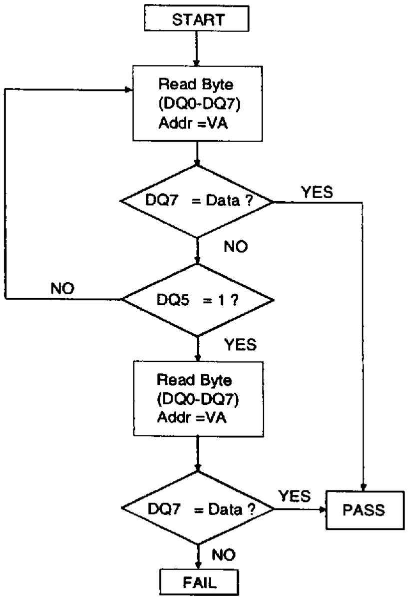


Individual Sector/Mulitiple Sector
Erase Command Sequence
(Address/Command):



Additional sector
erase commands
are optional

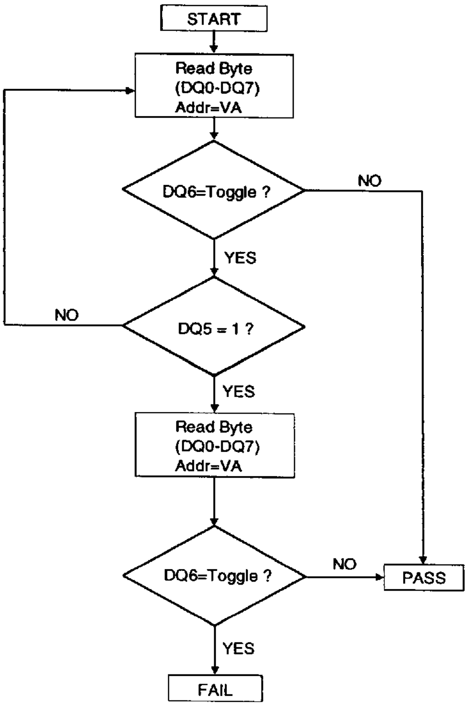
DATA POLLING ALGORITHM



NOTE:

1. DQ7 is rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.
2. VA = Byte address for programming.
   = Any of the sector addresses within the sector being erased during sector erase operation
   = XXXXXH during chip erase

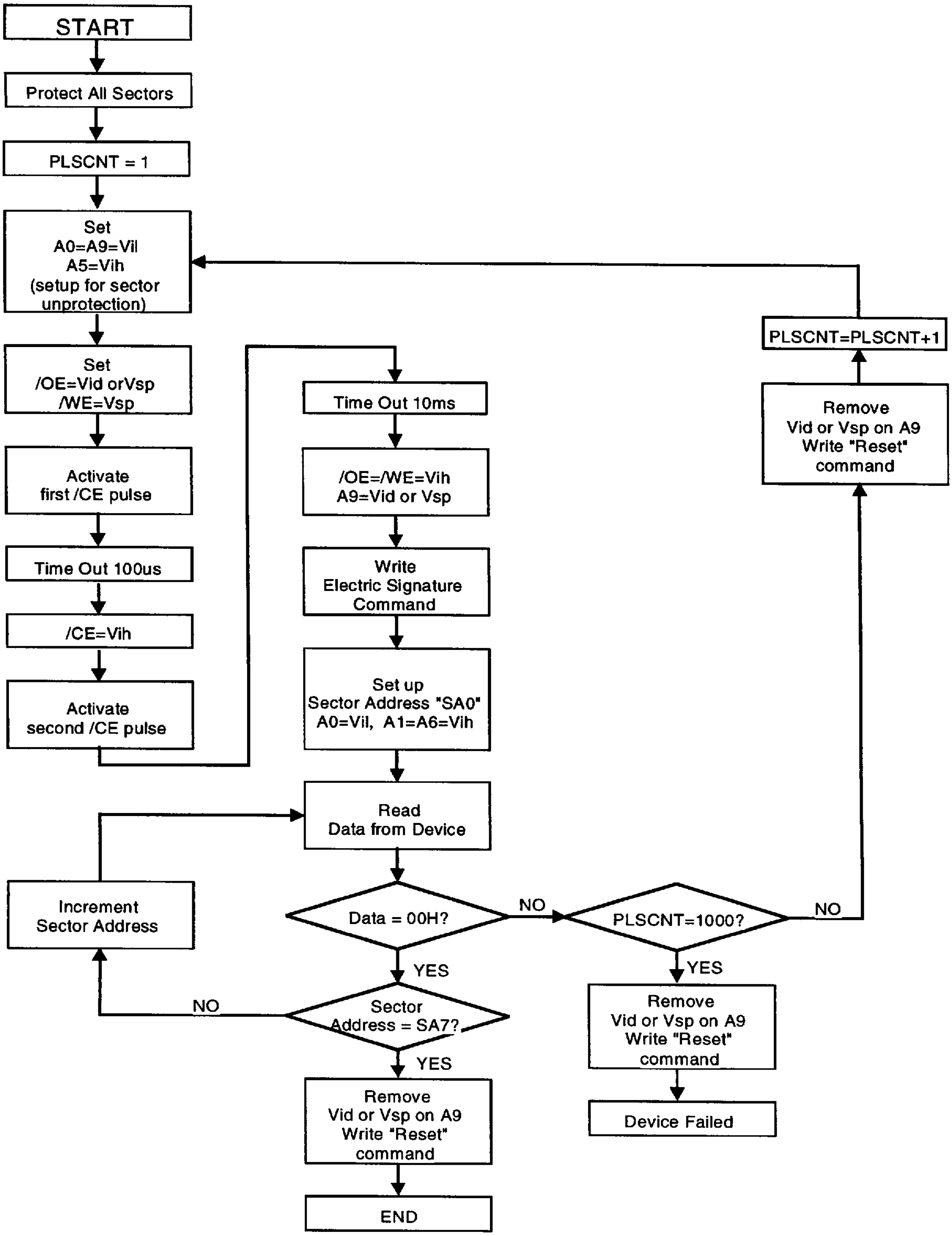
TOGGLE BIT ALGORITHM



NOTES:

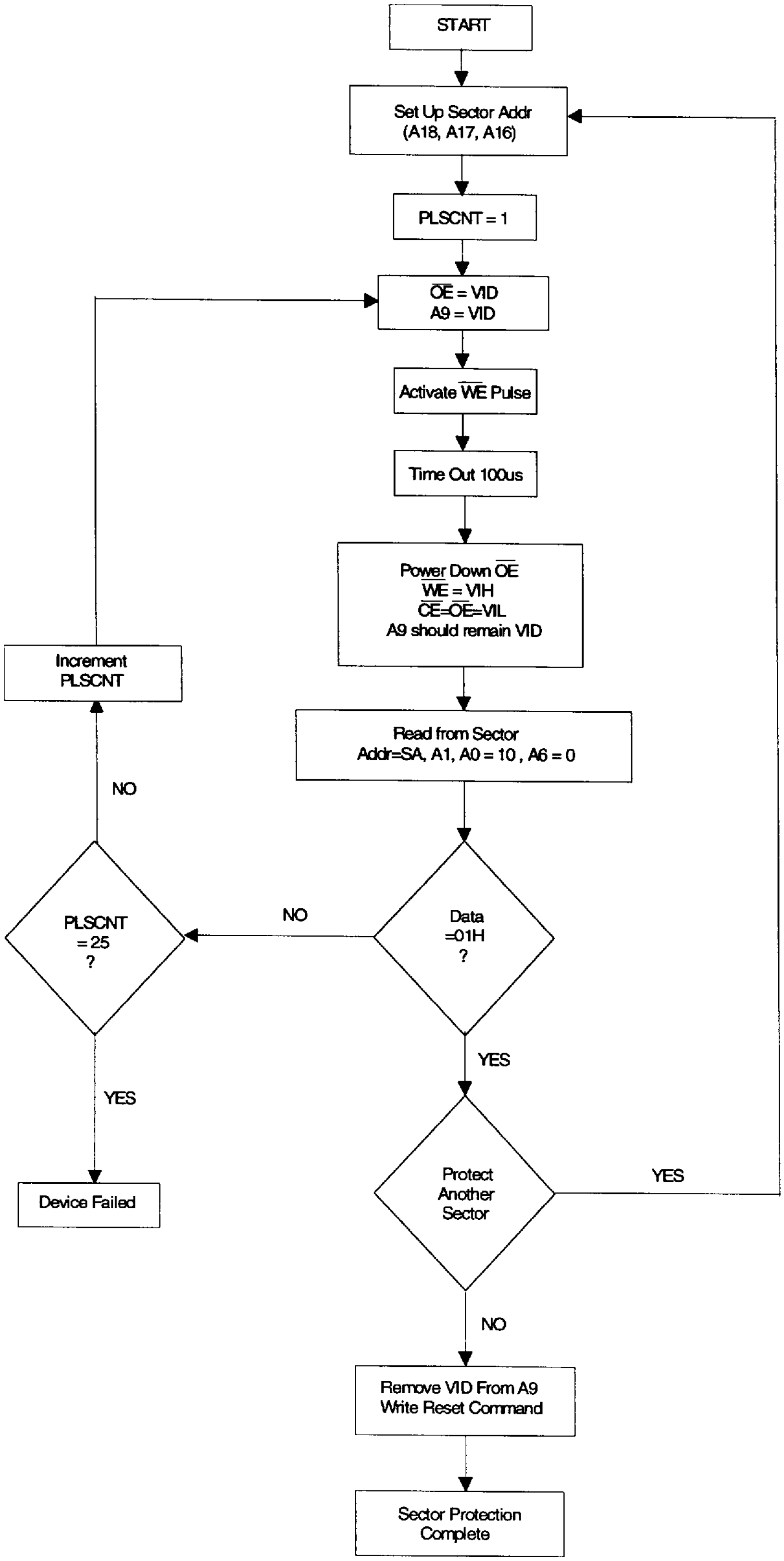
1. DQ6 is rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time as DQ5 changing to "1".
2 VA = As above.

SECTOR UNPROTECT ALGORITHM



NOTES:
SA0 = The First Sector Address
SA7 = The Last Sector Address
(Sector Address is indicated
using A16 to A18)

SECTOR PROTECTION ALOGORITHM



DEVICE OPERATION

The following description deals with the PUMA 3F16006 operating in 8 bit mode accessed through CE1, however status flag definitions shown apply equally to the corresponding flag for each device in the module.

Read Mode

The PUMA 3F16006 has two control functions which must be satisfied in order to obtain data at the outputs
CE1-4 is the power control and should be used for device selection
OE is the output control and should be used to gate data to the output pins if the device is selected.

Standby Mode

Two standby modes are available :
CMOS standby : CE1-4 held at Vcc +/- 0.5V
TTL standby : CE1-4 held at V_{IH}
In the standby mode the outputs are in a high impedance state independent of the OE input. If the device is deselected during erasure or programming the device will draw active current until the operation is completed.

Output Disable

With the OE input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify the die manufacturer and type. This mode is intended for use by programming equipment. This mode is functional over the full military temperature range. The autoselect codes for the first device are as follows :

Type	A18	A17	A16	A6	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacture Code	X	X	X	V_{IL}	V_{IL}	V_{IL}	04H	0	0	0	0	0	0	0	1
Device Code	X	X	X	V_{IL}	V_{IL}	V_{IH}	A4H	1	0	1	0	0	1	0	0
Sector Protection	Sector Address		V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1	

* Outputs 01H at protected sector address

To activate this mode the programming equipment must force V_{ID} on address A9 . Two identifier bytes may then be sequenced from each die device outputs by toggling A0 from V_{IL} to V_{IH}. All addresses are dont care apart from A1 & A0. All identifiers for manufacturer and device will exhibit odd parity with D7 defined as the parity bit. In order to read the proper device codes when executing the autoselect A1 must be V_{IL}.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The register is a latch used to store the commands along with the address and data information required to execute the command. The command register is written by bringing WE to V_{IL} while CE1-4 is at V_{IL} and OE is at V_{IH}. Addresses are latched on the falling edge of WE while data is latched on the rising edge.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. The following table defines these register command sequences.

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	F0H										
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care) Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (Don't Care), Data (30H)											

NOTES:

1. Address bit A_{15},A_{16},A_{17},A_{18}=X=Don't care. Write Sequences may be initiated with A_{15},A_{17} and A_{18} in either state.
2. Address bit A_{15},A_{16},A_{17},A_{18}=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA).
3. RA=Address of the memory location to be read.

   PA=Address of memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

   SA=Address of the sector to be erased. The combination of A_{18},A_{17} and A_{16} will uniquely select any sector.

4. RD=Data read from location RA during read operation.

   PD=Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$

Read / Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Sector Protection

The PUMA 3F16006 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 8). The sector protect feature is enabled using programming equipment at the users site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, and $CE=V_{IH}$. The sector adresses (A_{18},A_{17} and A_{16}) should be set to the sector to be protected. Programming of the protection circuitry begins on the falling edge of the WE pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the WE pulse.

To verify programming of the protection equipment circuitry, the programming equipment must force V_{ID} on address pin A_9 with CE and OE at V_{IL} and WE at V_{IH}. Reading the device at a particular sector address (A_{16},A_{17} and A_{18}) while (A_6,A_1,A_0) = (0,1,0) will produce 01H at data output D0 for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A_0, ,A_1 and A_6, are don't care. Address with $A_1=V_{IL}$ are reserved for autoselect codes. If a verify of the sector protection circuitry were done at these addresses, the device would output the manufacturer and device codes respectively.

It is also possible to determine if a sector is protected in the system by writing the autoselect command. Performing a read operation at XX02H , where the higher order addresses (A16, A17, A18) are sector addresses, (other addresses are a don't care) will produce 01H data if those sectors are protected. Otherwise the devidce will read 00H for an unprotected sector.

Sector Address Table

	A18	A17	A16	Address Range
SA0	0	0	0	000000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

Sector Unprotect

Sectors which have previously been protected from being programmed or erased may be unprotected using the Sector Unprotect Algorithm. All sectors must be placed in the protection mode using the protection algorithm before unprotection can proceed.

A special high voltage for unprotection V_{SP} is defined to be 10V+/-0.5V.

The unprotection mode is entered by setting $\overline{OE}$ to V_{ID} or V_{SP}, $\overline{WE}$ to V_{SP}, A5 to V_{IH} and A0=A9 to V_{IL}. Unprotect is invoked by applying to negative pulses on CE for a period of t_{WPP2}.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target systems. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desired system design practice.

The device contains an autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code A4H. A read cycle from address XXX2H returns information as to which sectors are protected. All manufacturer and device codes will exhibit odd parity with the MSB (D_7) defined as the paritybit.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycle. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE1-4}}$, whichever happens later, while the data are latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE1-4}}$ whichever happens first. The rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE1-4}}$ begins programming. Upon executing the Embedded Program Algorithm Command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. The automatic programming operation is completed when the data on D_7 is equivalent to data written to this bit (see written Operations Status) at which time the device returns to read mode. Data Polling must be performed at the memory location which is being programmed.

Programming is allowed in any address sequence and across sector boundaries.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase doesn't require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The systems is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{\text{WE}}$ pulse in the command sequence and terminates when the data on D_7 is "1" (See Written Operation Section) at which time the device returns to read the mode.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock"write cycles. These are followed by writing the "Set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{\text{WE}}$, while the command (data) is latched on the rising edge of $\overline{\text{WE}}$. A time-out of 50us from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as desribed above. This sequence is followed with writes of the sector erase command 30H to addresses in other sectors required to be concurrently erased. A time-out of 50us from the rising edge of the $\overline{\text{WE}}$ pulse for the last sector erase command will initiate the sector erase. If another sector erase command is wriiten within the 50us time-out window the timer is reset. Any command other than sector erase within the time-out window will reset the device to the read mode, ignoring the previous command string (refer to Write Operation Status section for Sector Erase Timer operation). Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase doesn't require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50us time-out from the rising edge of the $\overline{\text{WE}}$ pulse for the last sector erase command pulse and terminates when the data on D_7 is "1" (see Written Operation Status Section) at which time the device returns to read mode. Data polling must be preformed at an address within any of the sectors being erased.

Erase Suspend

Erase suspend allows the user to interupt the chip and read data (not program) from a non busy sector while it is in the middle of a sector erase operation, which may take several seconds.

The command can only be used during sector erase operation and otherwise will be ignored. The erase suspend command B0h is also allowed during the Sector Erase Operation that will include the sector erase time out period after the sector erase commands B0h. Writing this command during the timeout will result in immediate termination of the time out period and any subsequent writes of Sector Erase Command will be taken as Erase Resume.

To suspend the erase operation and go into erase suspend mode (pseudo read mode) requires between 0.1 and 10µs, during which time the user can read from a sector that is not being erased. The toggle bit stops toggling when the device enters pseudo read mode and an address of a sector not being erased must be used to read the toggle bit.

After the user writes the erase suspend command and waits until the toggle bit stops toggling, data reads from the device may then be performed. After an Erase Resume command the internal counters, which are used to count the high voltage pulses required to program or erase, are reset. The Exceed Time limit flag D5 is set if the count exceeds a certain limit. (The resetting of the counters is necessary as the erase suspend command can potentially interupt the high voltage pulses.)

Operating Modes

The following modes are used to control the PUMA 3F16006

OPERATION	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0	A1	A6	A9	I /O
Auto-Select Manufacturer Code	L	L	H	L	L	L	V_{ID}	Code
Auto Select Device Code	L	L	H	H	L	L	V_{ID}	Code
Read (1)	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	High Z
Output Disable	L	H	H	X	X	X	X	High Z
Write	L	H	L	A0	A1	A6	A9	Din
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X
Verify Sector Protect	L	L	H	L	H	L	V_{ID}	Code

1) L=V_{IL}, H=$V_{IH,}$ X=Don't Care

NOTE: 1) $\overline{\text{WE}}$ can be V_{IL} if $\overline{\text{CE}}$ is V_{IL}, $\overline{\text{OE}}$ at V_{IH} initiates write cycle.

WRITE OPERATIONS STATUS

HARDWARE SEQUENCE FLAGS

	STATUS	D7	D6	D5	D3	D2-D0
In Progress	Auto-Programming	$\overline{DQ_7}$	Toggle	0	0	$(\overline{D})$
	Programming in auto erase	0	Toggle	0	1	
	Erasing in Auto Erase	0	Toggle	0	1	
Exceeded Time limits	Auto-Programming	$\overline{DQ_7}$	Toggle	1	1	$(\overline{D})$
	Programming in auto erase	0	Toggle	1	1	
	Erasing in Auto-Erase	0	Toggle	1	1	

NOTE: DQ0, DQ1, DQ2, DQ4 are reserve pins for future use.

D7 Data Polling

The Puma 3F16006 features Data Polling as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Programming Algorithm, an attempt to read the device will produce complement data of the data last written to D_7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to D_7. Data Polling is valid after the rising edge of the forth $\overline{\text{WE}}$ pulse in the four write pulse sequence.

During the Embedded Erase Algorithm, D_7 will be "0" until the erase operation is completed. Upon completion data at D_7 is "1". For chip erase, the Data Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, Data Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out.

D_6 Toggle Bit

The PUMA 3F16006 also features the "toggle bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read data from the device will result in D_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, D_6 will stop toggling and valid data will be read on successive attempts. During programming, the Toggle bit is valid after the rising edge of the forth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector time-out.

D_5 Exceeding Time Limits

D_5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions D_5 will produce "1", indicating the program or erase cycle was not successfully completed . Data Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions . To reset the device, write reset command sequence to the device. This allows the system to continue to use the other active sectors in the device, if this failure occurs during sector erase operations, it specifies that a particular sector is bad and may not be re-used. The device must be reset to use other sectors. While the reset command sequence and execute program or erase command sequence.
If this failure occurs during chip erase operation , it specifies that the device chip or combination of sectors are bad. If this failure occurs during the byte programming operation, it specifies that the active sectors containing that byte is bad and may not be re-used.
The D5 failure condition may also appear if the user tries to program a non blank location without erasing. In this case the device locks out and never completes the embedded algorithm operation. Hence the system never reads a valid data on D7 and D6 never stops toggling. Once the device has exceeded timing limits, the D5 bit will indicate '1'

D_4 Hardware Sequence Flag

If the device has exceeded the specified erase or program time and D_5 is "1", then D_4 will indicate at which step in the algorithm the device exceeded the limits. A "0" in D_4 indicates in programming, a "1" indicates an erase.

D_3 Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D_3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, D_3 may be used to determine if the sector erase timer window is still open. If D_3 is high the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If D_3 is low , the device will accept additional sector erase commands. To insure the command has been accepted, the software should check the status of D_3 prior to and following each subsequent sector erase command. If D_3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The PUMA 3F16006 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the internal state machine in the Read mode. Also, with its controls register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power up and power down transitions or system noise.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during V_{CC} power up and power down, a write cycle is locked out for V_{CC} less than 3.2V (typically 3.7V). If $V_{CC}<V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is usually correct to prevent unintentional writes when V_{CC} is above 3.2V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$, $\overline{\text{WE}}$ will not initiate a write cycle

Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}}=V_{IL}$, $\overline{\text{CE}}=V_{IH}$ or $\overline{\text{WE}}=V_{IH}$. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be logical zero while $\overline{\text{OE}}$ is a logical one.

Power Up Write Inhibit

Power-up of the device with $\overline{\text{WE}}=\overline{\text{CE}}=V_{IL}$ and $\overline{\text{OE}}=V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

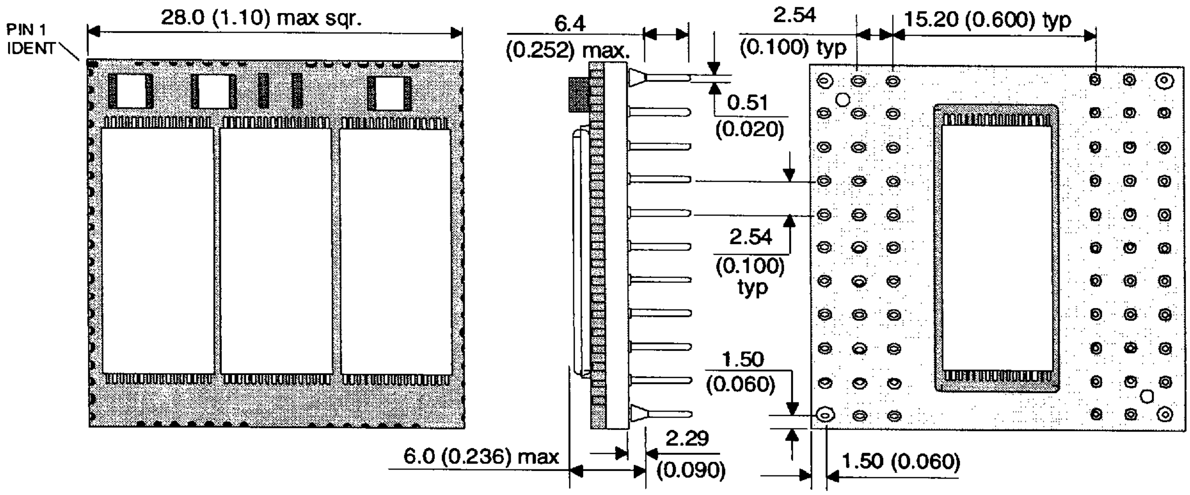
Sectors of the PUMA 3F16006 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time		1 (Note 1)	30	sec	Excludes 00H programming prior to erasure.
Byte Programming Time		16	1000 (Note 2)	us	Excludes System-level overhead.
Chip Programming Time		8.0 (Note 1)	50	sec	Excludes system-level overhead.
Erase/Program Cycles	100,000	1,000,000		cycles	

Notes: (1) 25°C, 5V V_{cc}, 100,000 cycles.
(2) The Embedded Algorithms allow for 48ms byte program time.

Package Details



Ordering Information

PUMA 3F16006I-90

Speed
90 = 90 ns
12 = 120 ns
15 = 150 ns

Temp. range/screening
Blank = Commercial Temperature
I = Industrial Temperature

Organisation
16006 = 512Kx 32, user confiurable as 1M x 16 and 2M x 8

Technology
F = FLASH MEMORY

Package
PUMA3 = 66 pin PGA