Agilent HDMP-3001 STS-3c/STM-1 Ethernet over SONET/SDH Mapper

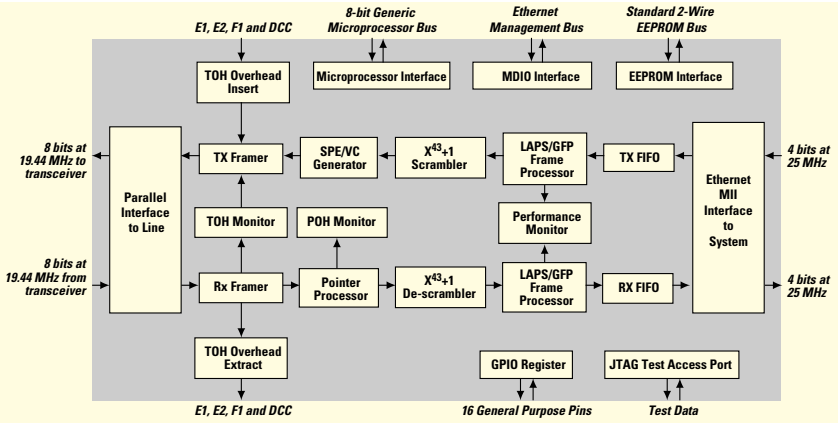
Product Brief

Description

The HDMP-3001 is an integrated device that provides full-duplex mapping of Ethernet frames into an STS-3c SONET/STM-1 SDH payload as well as complete SONET/SDH framing. Mapping of Ethernet frames is performed using either the LAPS or GFP protocol.

On the system side, the HDMP-3001 can be connected to either an Ethernet PHY or an Ethernet MAC depending on system requirements. When connected to a MAC, it behaves like any other 100 Mb/s Ethernet PHY and can be connected to the same MDIO bus as regular PHY's. When connected to a PHY, a connection to the Ethernet is achieved with a minimum of components.

HDMP-3001 Block Diagram



Features

- **Single-chip frame processor with full-duplex mapping of Ethernet frames into SONET/SDH payload using the GFP or LAPS protocol**
- **Integrated SONET STS-3c/SDH STM-1 framer that terminates and generates SONET/SDH overhead limits the number of external devices required**
- **System-side Ethernet MII interface and line-side 8-bit parallel interface allows for easy hook-up to standard components**
- **Availability of both generic microprocessor interface and Ethernet MDIO interface provides for configuration and status monitoring**
- **Extensive set of performance counters**
- **Configurable by an external EEPROM (useful in stand-alone applications)**
- **Provides internal loop-back paths for diagnostics**
- **Implemented in low-power 0.25 micron CMOS process with 1.8V core and 3.3V I/Os**
- **160 pin PQFP**

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Benefits

- Allows LANs to be interconnected over leased OC-3c lines, thereby extending a LAN to multiple sites
- Ethernet switches in each LAN can be connected together directly which reduces cost and complexity
- Enables Transparent LAN Services which, unlike POS solutions, does not require WAN access routers
- 1+1 redundancy private reliable Ethernet service in SDH/SONET ring

Applications

- Multi-Service Ethernet Switches
- Enhanced Services SONET/SDH Add/Drop Multiplexers (ADMs)
- DSU/CSUs

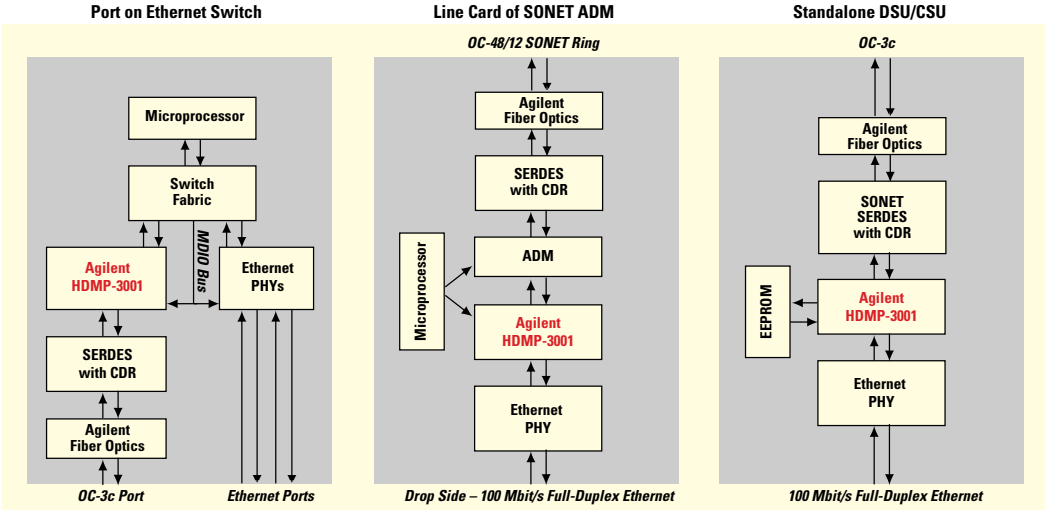
Interfaces

- System interface is a 25 MHz IEEE 802.3 full-duplex, 100 Mb/s Ethernet MII port that connects to either a PHY and or a MAC
- Line side SERDES interface is 8-bit parallel operating at 19.44 MHz. SONET/SDH framer is compliant to specifications ANSI T1.105 and ITU G.707
- Serial data channels for add and drop of SONET overhead bytes E1, E2, F1 and DCC
- Generic 8-bit microprocessor interface allows direct connection to commonly used processors
- IEEE 802.3 MDIO management interface
- Standard 2-wire EEPROM interface for optional boot-up configuration
- Provides 16-bit General Purpose I/O (GPIO) register
- Provides standard five-pin IEEE 1149.1 JTAG test port

Data Processing

- Complies to the GFP (Generic Framing Procedure) draft specification, revision 2, of ANSI T1X1.5 Implements both the null and linear header options
- Complies to the LAPS (Link Access Procedure – SDH) specification X.86 of ITU-T
- Optional self-synchronous $X^{43}+1$ scrambling of the payload

Typical Usage



This product was jointly developed by Agilent Technologies and Wuhan Research Institute.

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