Programmable Data Coder

Ordering Information

Device	28-Pin Plastic DIP	28-Pin Plastic Quad J Lead	28-Pin SO Gullwing	Die
DC7	DC7P	DC7PJ	DC7WG	DC7X

Features

- 8 data bits (byte wide data)
- 7 address bits (128 addresses)
- Manchester phase encoding
- Transmitter/receiver in one circuit
- Schmitt trigger input for excellent noise rejection
- Built-in oscillator using non-critical RC components
- Zener diode to regulate the power supply
- Low power, high noise immunity CMOS technology
- Ability to decode original signals
- Automatic preamble generation

Applications

- Multi-port computer I/O
- Smoke & fire alarm control systems
- Pocket pagers
- Digital locks
- Theft alarm systems
- Security systems
- Digital paging systems
- Special identification code systems
- Remote sensor data acquisition systems
- Single channel digital transmission of information

General Description

The DC7 is a single monolithic chip using metal gate CMOS technology for low cost, low power, high yield and high reliability. This dual purpose circuit is capable of working either as an encoder, or decoder of its own transmission, in applications where exclusive recognition of address codes is required in addition to transmission or reception of 8 data bits. It will decode 1 of 128 address codes. In the transmit mode, this circuit is capable of generating the possible codes by connecting the Address and Data Inputs to V_{DD} or GND for a "1" or a "0". In the receive mode, this circuit is capable of decoding the transmitted signals and simultaneously making comparisons to the local address code for identification.

Absolute Maximum Ratings

Supply Voltage with respect to GND	6.4V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +150°C
Zener Current	100mA

i5

Electrical Characteristics

DC Characteristics (V_{DD} = 5.0 ± 5%; GND = 0V; T_A = 25°C)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
V_{IH}	Input High Voltage	V_{DD} - 0.3		V_{DD} + 0.3	V	"1" INPUT
V_{IL}	Input Low Voltage	GND - 0.3		0.3	V	"0" INPUT
I_{LKC}	Input Leakage Current		0.1	2.0	µA	V_{IN} = 5.0V for pins T/R, SDI
I_{LC}	Input Load Current	2.0	6.0	20.0	µA	V_{IN} = 5.0V for pins RS, A0 - A6, D0 - D7
V_{OH}	Output High Voltage	V_{DD} - 0.3			V	V_{DD} = 4.75V, I_{LOAD} = -100µA
V_{OL}	Output Low Voltage			0.3	V	V_{DD} = 4.75V, I_{LOAD} = 100µA
I_{OH}	Output High Current (Sourcing)	-1.0	-1.5		mA	V_{OH} = V_{DD} - 1.0V
I_{OL}	Output Low Current (Sinking)	1.0	3.0		mA	V_{OL} = 1.0V
V_Z	Zener Voltage	5.5	6.4	7.0	V	I_Z = 10µA (Note 2)
		6.0	6.7	7.5	V	I_Z = 10mA (Note 2)
C_{IN}	Input Capacitance			10	pF	(Note 2)
C_{OUT}	Output Capacitance			10	pF	(Note 2)
I_{DD}	Drain Current			10	µA	V_{DD} = 5.0V, all inputs = GND all outputs floating

Notes:
1. Typical values are those values measured in a production sample at V_{CC} = 5.0V.
2. This parameter is periodcally sampled and is not 100% tested.

AC Characteristics (V_{DD} = 5.0 ± 5%; T_A = 25°C)

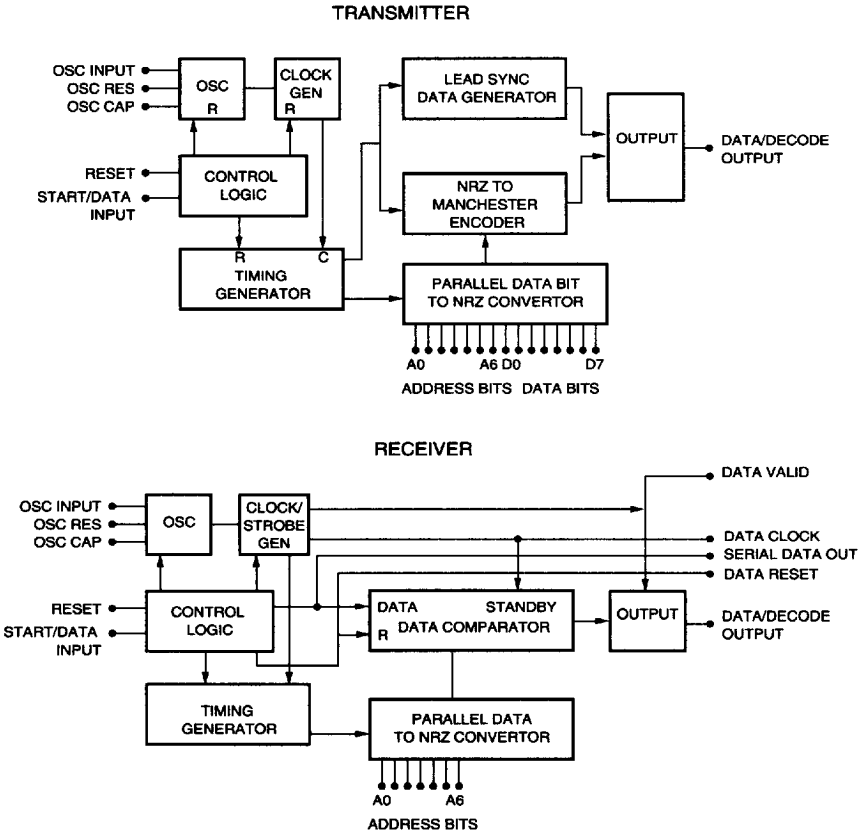
Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Conditions
f_C	Clock Frequency	0		20	kHz	R = 150k, C = 100pF; Clock Period (t_C) = 1/f_c
t_{SDI}	Start Pulse Width	500			ns	
t_{DDO}	DDO Delay from SDI		5		µs	
t_{DC}	Data Clock Pulse Width		.5t_C		sec	
t_{WORD}	Full Cycle Word Length		130t_C		sec	
R_R	Receiver Oscillator Resistor Tolerance from Transmitter Oscillator Resistor		±10		%	
C_R	Receiver Oscillator Capacitor Tolerance from Transmitter Oscillator Capacitor		±10		%	

Note:
1. Typical values are those values measured on a production sample at V_{CC} = 5.0V.

Pin Definition

Label	Pin Name	Function
GND	Ground	Supply Potential negative side.
OI	Oscillator Input	This input is to drive the oscillator and is the tie point of the timing resistor (R_T), and the timing capacitor(C_T). It also is connected through a diode to an open drain P-channel device that turns on to V_{DD} when the oscillator is being reset. This input can exceed the power supplies during normal oscillator operation.
OR	Oscillator	Provides phase feedback to the RC timing circuit through the connected timing resistor. Note: This resistor pin is driven high during oscillator reset.
OC	Oscillator Capacitor	Capacitor connection of RC timing circuit provides phased feedback from the oscillator. This pin is driven low during oscillator reset.
RS	Reset	This input pin may be used to override the data transmission cycle or to inhibit an SDI input. It clears the D/DO to a low state and resets the internal oscillator and data comparison circuits. This pin may be left open (No Connection) when not used, or driven as an input, or an external capacitor (100pF) to V_{DD} may be added for power-up reset. The reset function is activated when this input is connected to V_{DD}.
S/DI	Start/Data Input	Start/Data input is a dual function pin. It is used to start the oscillator which enables the transmission of the encoded word in the transmit mode. And, in the receive mode, this input receives the serial coded information for processing and comparison.
D/DO	Data/Decode Output	Another dual purpose pin, this pin is the encoded sequence data output in the transmit mode and becomes the decode true output in the receive mode. It indicates that the incoming code has matched the local bit data input address.
A0-A6	Address Inputs	These inputs provide the parallel address to be sequentially transmitted. In the receive mode, these inputs become the parallel local address code for comparison with the incoming data.
D0-D7	Data Bit Inputs	These inputs provide parallel data to be sequentially transmitted. In the receive mode, these inputs are not used.
SDO	Serial Data Output	This output signal is a buffered S/DI signal after going through the input Schmitt Trigger, a delay circuit, and is the same polarity as the input and can be used to chain a number of receivers together. This output can be connected to the input of an 8-bit shift register (clocked by the DC pin) in a receiver system where data is to be recovered. This output can be connected to the input of a 16-bit shift register (clocked by the DC pin) in a receiver system where address and data are to be recovered.
DRS	Data Reset Output	Data Reset can be used in the receive mode to reset an external data shift register since this signal pulse indicates that a new word has just begun processing.
DC	Data Clock Outputs	The Data Clock output may be used in a receive system since it is the recovered data sync pulses. Also, this output can be used to clock an external shift register where data is to be recovered.
DV	Data Valid Output	This output is triggered low at the start of any input and will remain low until a complete word has been processed. Note that this output simply signals that a valid word has been received and not that the code received has matched the local address code.
T/R	Transmit/ Receive	This is a control input to determine the operating mode. A logic high applied to this input puts it in the transmit mode; a logic low puts it in the receive mode.
V_{DD}	V_{DD}	Positive Supply Potential: This circuit contains an on-chip zener of approximately 6.7 volts across the supply terminals.

Block Diagrams



Operation

General

The DC7 mode of operation is controlled by the transmit/receive control input (T/R). When switched from V_{DD} to GND, the circuit will automatically change the oscillator, start/data input, and data decoder output from transmit to receive mode.

The DC7 contains an on-chip zener diode to clamp the power supply to around 6.7 volts. The circuit will operate from 4.0 volts to the zener voltage, but operation is recommended at 5 volts ± 5%, or from a regulated power supply in order to stabilize the time constants of the oscillator circuit. In order to use the on-chip zener diode, a current limiting resistor of 1K ohm or greater is required. If pull up resistors are used for the D_1 - D_{15} drivers, the resistors should be tied to a voltage no higher than that on Pin 28 or 6 volts, whichever is lower.

Output drivers are capable of sinking or sourcing 1.0mA minimum at 1.0 volt V_{DS} . All inputs are gate protected to both power supplies by internal diodes. The Address Data Inputs of the DC7 each have pull down resistors to ground so that only a "1" will have to be programmed. This allows the inputs to be programmed by using SPST switches or jumpers to V_{DD} only. The transmit/ receive input does not have a pull up or pull down resistor. The start/data input also does not have a pull up or pull down resistor, but is applied to a Schmitt Trigger Input circuit to improve noise rejection.

Transmit Function

This function is selected by connecting the transmit/receive control input to V_{DD}. This enables the transmit mode and the circuit to function, as an encoder, sampling the 7 address and 8 data input pin digital information and encoding this parallel data in NRZ format, combining it with the clock in Manchester Code (Phase Encoded) and presenting it to the D/DO pin for transmission (usually to another DC device used as the decoder circuit). The encoder will transmit the serial data each time the start/data input is activated.

This encoded data word is transmitted in 2 parts. The first part is the preamble information which is a series of 12 "1"s and then a space indicating that the encoded data is to follow. This preamble information is intended to be used to synchronize a phase locked loop at the receiver or used as a setting time for receivers that have automatic gain control. The second part contains the 7 bits of address and 8 bits of data.

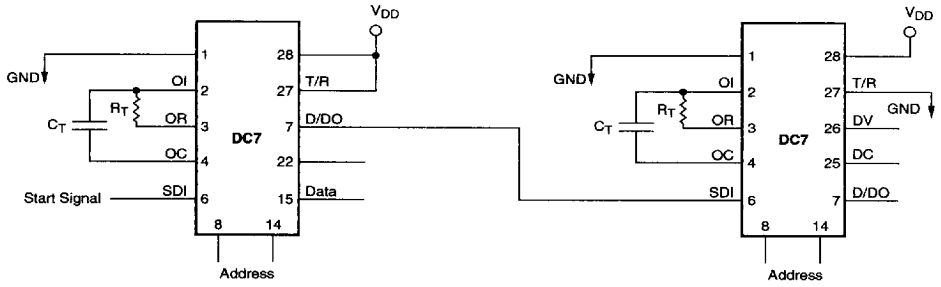
Receive Function

The receive mode is selected by connecting the transmit/receive control input to ground. In this mode the circuit will work as a decoder receiving the serial data in Manchester Encoded format and recovering the clock. The incoming data is converted to a 15-bit serial word. It is compared with the local address word by sampling the address inputs (7-bits). These bits are usually programmed to the expected address that will be decoded. If the two address words match, the decoded output will go to a logic "1" state, but if the two do not match the decoded output will stay low. Also, if the words do not match but the bit stream was valid (i.e., 15-bits of proper timing) then only the output valid signal will go high. If at any time the bit sequence has the wrong timing, the local oscillator and internal comparison circuits will be reset and any new input pulses will be recognized as a new bit stream. Therefore, as with the receiver processing of the preamble information, the 12-bits will be recognized. But, during the 13th interval where no bit transition occurs, the circuit times out and awaits the start bit of the address and data sequence.

The DC7 will only compare the first 7 bits and ignore the state of the last 8-bits — that is, 128 distinct address codes with 8 bits that may be used for data transmission.

Transmit and Receive Address and Data Patterns

DC7 to DC7



Transmitted Bit Sequence

1	X	X	X	X	X	X	X	X	X	X	X	X	X	X
A0							A6	D0						D7

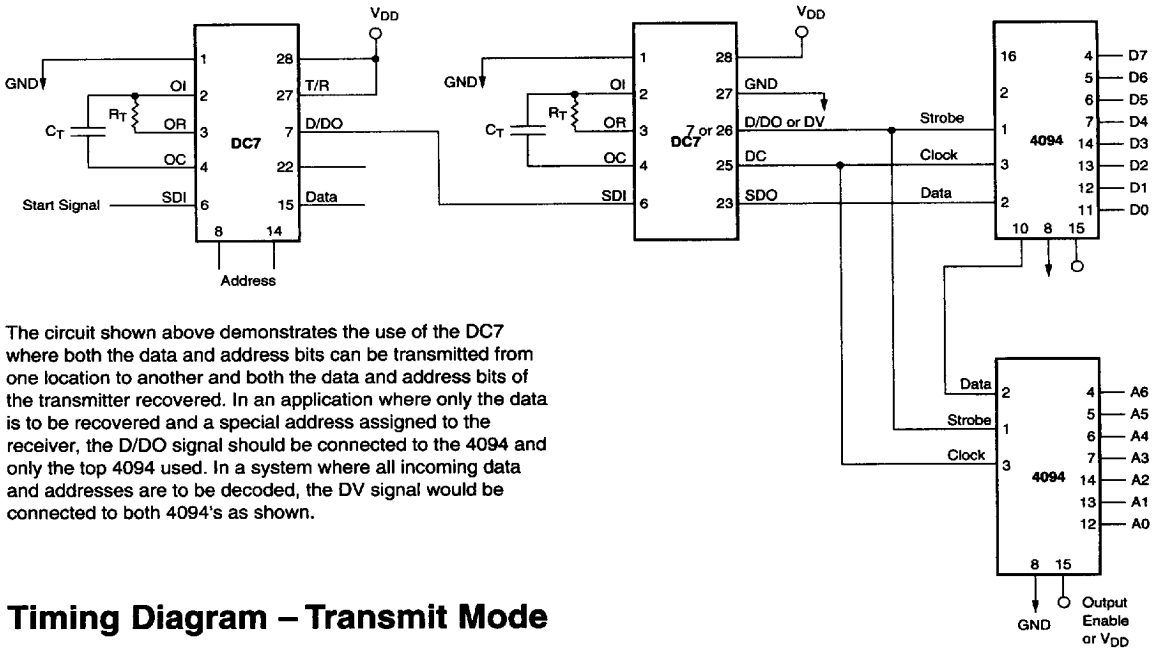
Received Address Code

1	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D
A0							A6	D0							D7

Note: Bit Sequence Code Format
X = Programmable
0 = Hardwired Internally Zero
1 = Hardwired Internally One
D = Don't Care in Receive Mode (Data)

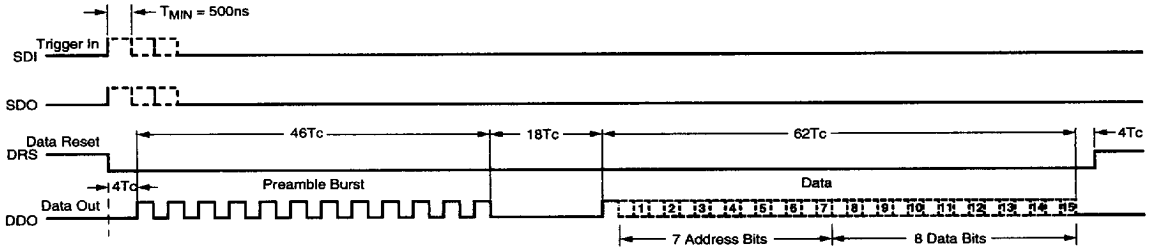
When unused, the DV, DC, DRS and SDO pins should be left floating and **must not** be tied to either a power supply or to ground.

Typical Application



The circuit shown above demonstrates the use of the DC7 where both the data and address bits can be transmitted from one location to another and both the data and address bits of the transmitter recovered. In an application where only the data is to be recovered and a special address assigned to the receiver, the D/DO signal should be connected to the 4094 and only the top 4094 used. In a system where all incoming data and addresses are to be decoded, the DV signal would be connected to both 4094's as shown.

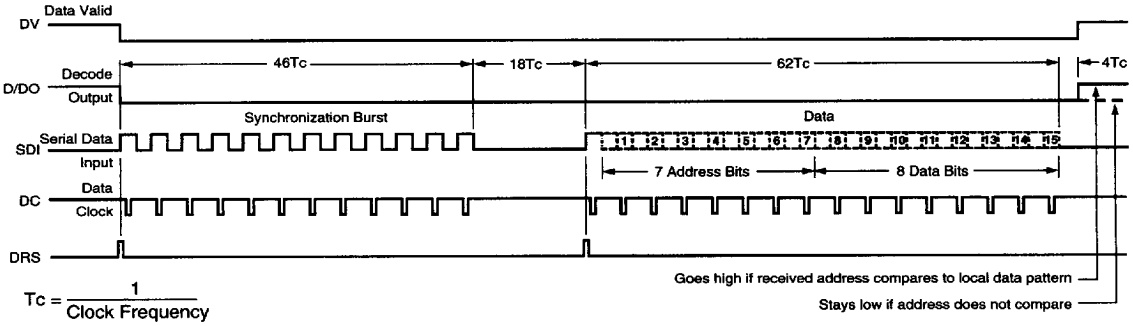
Timing Diagram – Transmit Mode



Total Time Required for Transmission of One Sequence = (DRS – 4Tc) =130Tc

$$Tc = \frac{1}{\text{Clock Frequency}}$$

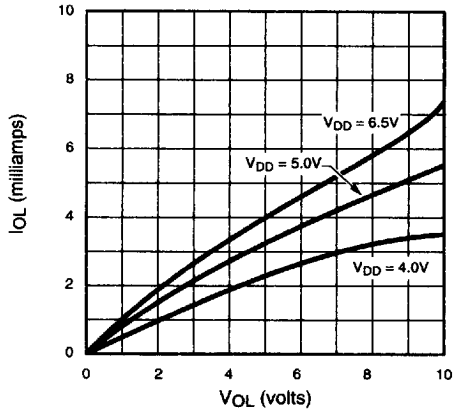
Timing Diagram – Receive Mode



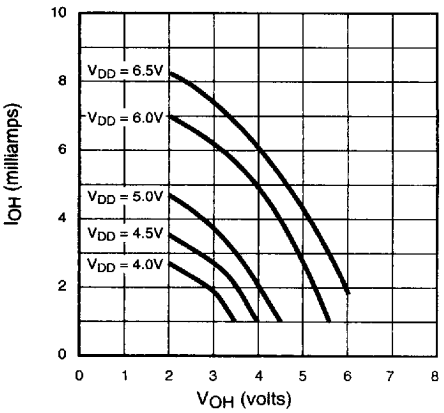
$$Tc = \frac{1}{\text{Clock Frequency}}$$

Typical Performance Curves (T_A = 25°C unless otherwise noted)

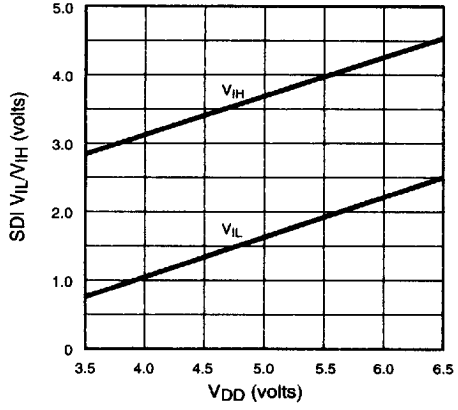
I_{OL} vs V_{DD} vs D_{OL}



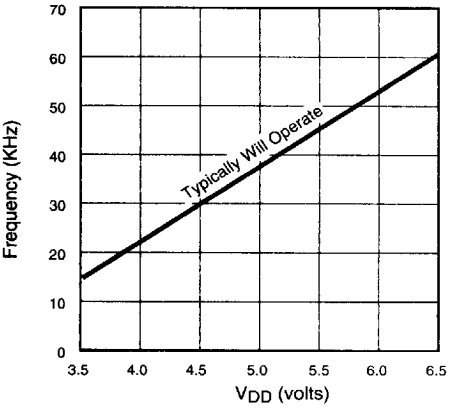
I_{OH} vs V_{DD} vs V_{OH}



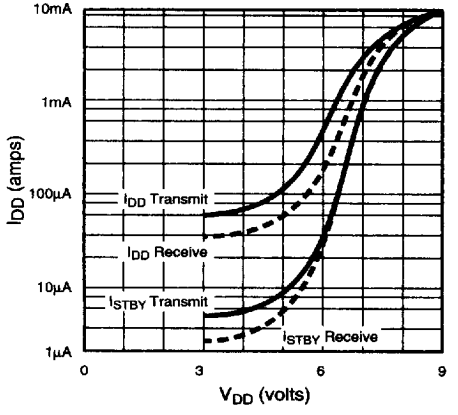
SDI Input
V_{IL}/V_{IH} vs V_{DD}



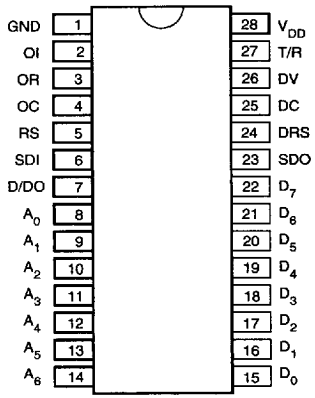
Operating Frequency vs V_{DD}



I_{DD} vs V_{DD}

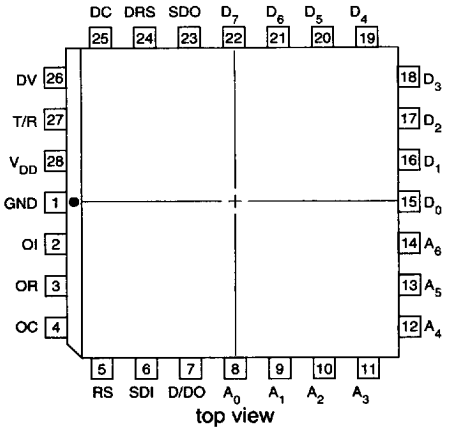


Pin Configuration



top view

28-pin DIP and 28-pin SOW



top view

28-pin J-Lead Package