2.5V 8BIT 2MSPS DAC DAC1252X

GENERAL DESCRIPTION

The DAC1252X is a CMOS 8BIT D/A converter for general application. This digital to analog converter has a R2R structure.

Its settling time is 500ns (Typical value).

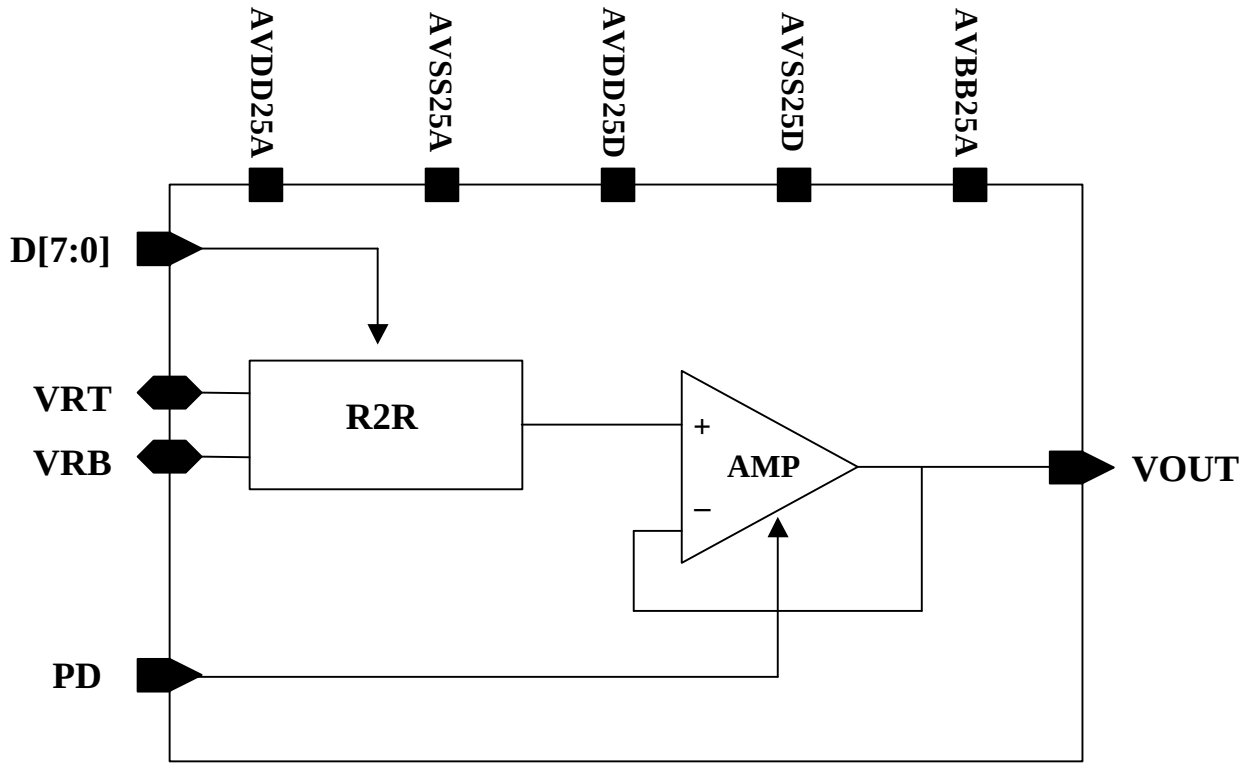
TYPICAL APPLICATIONS

- Hard Disk Drive (HDD)
- Battery Operated Instruments
- Motor Control Systems
- General Applications

FEATURES

- **Resolution : 8BIT**
- **Differential Linearity Error : ± 1.0 LSB**
- **Integral Linearity Error : ± 1.0 LSB**
- **Settling Time : 500ns**
- **Low Power Consumption : 890uA**
- **Power Down Mode**
- **Operation Temperature Range : 0° C ~ 70° C**
- **Power Supply : 2.5V Single**

FUNCTIONAL BLOCK DIAGRAM



Ver 2.1 (Apr. 2002)

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CORE PIN DESCRIPTION

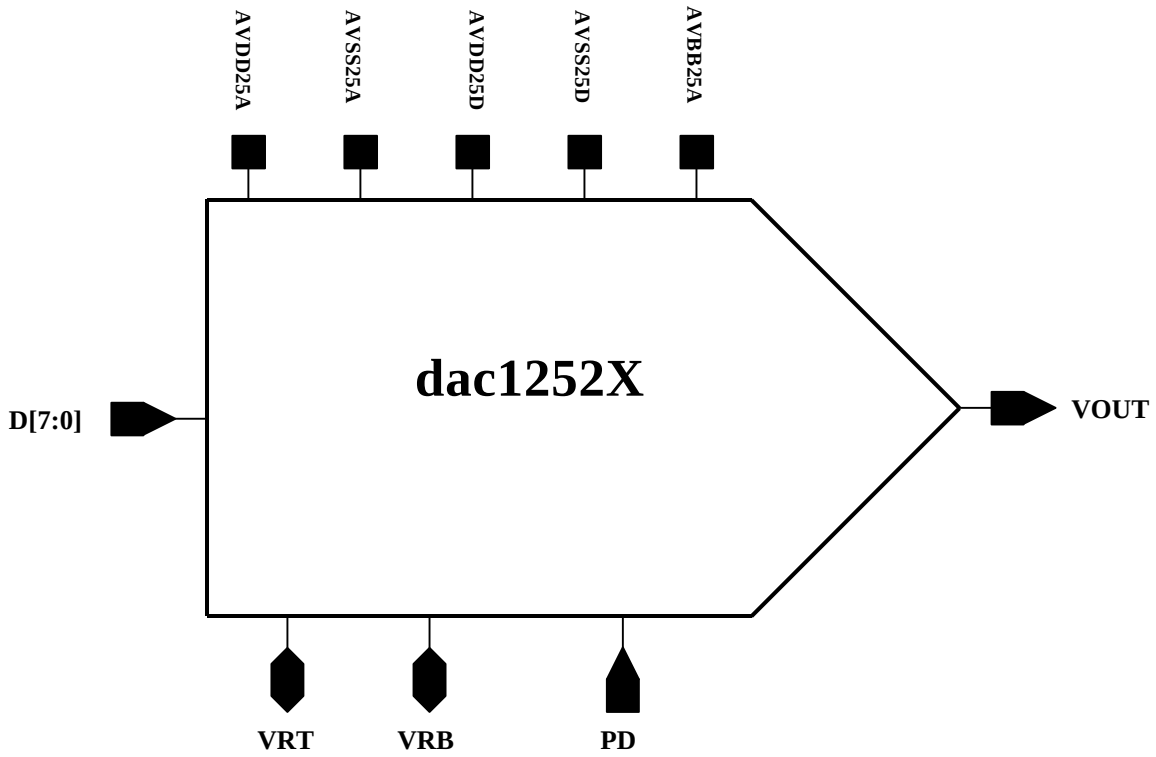
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
D[7:0]	DI	picc_abb	Digital Input Data (8BIT) D[7] : MSB , D[0] : LSB
PD	DI	picc_abb	Power Down (Active Low)
VRT	AB	pia_abb	Voltage Reference Top
VRB	AB	pia_abb	Voltage Reference Bottom
VOUT	AO	poa_abb	Analog Voltage Output
AVDD25A	AP	vdd2t_abb	Analog Power (+2.5V)
AVSS25A	AG	vdd2t_abb	Analog Ground (0.0V)
AVDD25D	DP	vdd2t_abb	Digital Power (+2.5V)
AVSS25D	DG	vss2t_abb	Digital Ground (0.0V)
AVBB25A	AG	vbb_abb	Analog Sub Bias (0.0V)

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD (AVDD25A,AVDD25D)	3.3	V
Analog Output Voltage	VOUT	AVSS25A to AVDD25A	V
Digital Input Voltage	D[7:0]	AVSS25D to AVDD25D	V
Reference Voltage	VRT VRB	AVDD25A AVSS25A	V
Operating Temperature Range	Topr	0 to 70	°C

NOTES :

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS(AVSS25A or AVSS25D or AVBB25A) unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD25A - AVSS25A AVDD25D - AVSS25D	2.375	2.5	2.625	V
Supply Voltage Difference	AVDD25A - AVDD25D	-0.1	0.0	0.1	V
Reference Voltage	VRT VRB	- 0.0	- -	2.5 -	V
Digital Input 'Low' Voltage Digital Input 'High' Voltage	VIL VIH	- 0.7×VDD	- -	0.3×VDD -	V
Operating Temperature	Topr	0	-	70	°C

NOTE :

It is strongly recommended that to avoid power latch-up all the supply pins(AVDD25A,AVDD25D) be driven from the same source.

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications : AVDD25A=AVDD25D=2.5V, AVSS25A=AVSS25D=AVBB25A=0V, PD=High, Top=25°C, VRT=2.5V, VRB=0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	Bit	-	8	-	Bits	-
Differential Linearity Error	DLE	-	1.0	-	LSB	-
Integral Linearity Error	ILE	-	1.0	-	LSB	-
Zero Scale Error[1]	V_{ZSE}	-	5	-	mV	VRT=2.5V , VRB=0.0V
Full Scale Voltage Error[2]	V_{FSE}	-	5	-	mV	
Maximum Output Voltage	Vo_{MAX}	-	2.499	-	V	Vo_{MAX} = VOUT(D[7:0]=High)
LSB Size	V_{LSB}	-	0.61	-	mV	V_{LSB} = Vo_{MAX} / 256

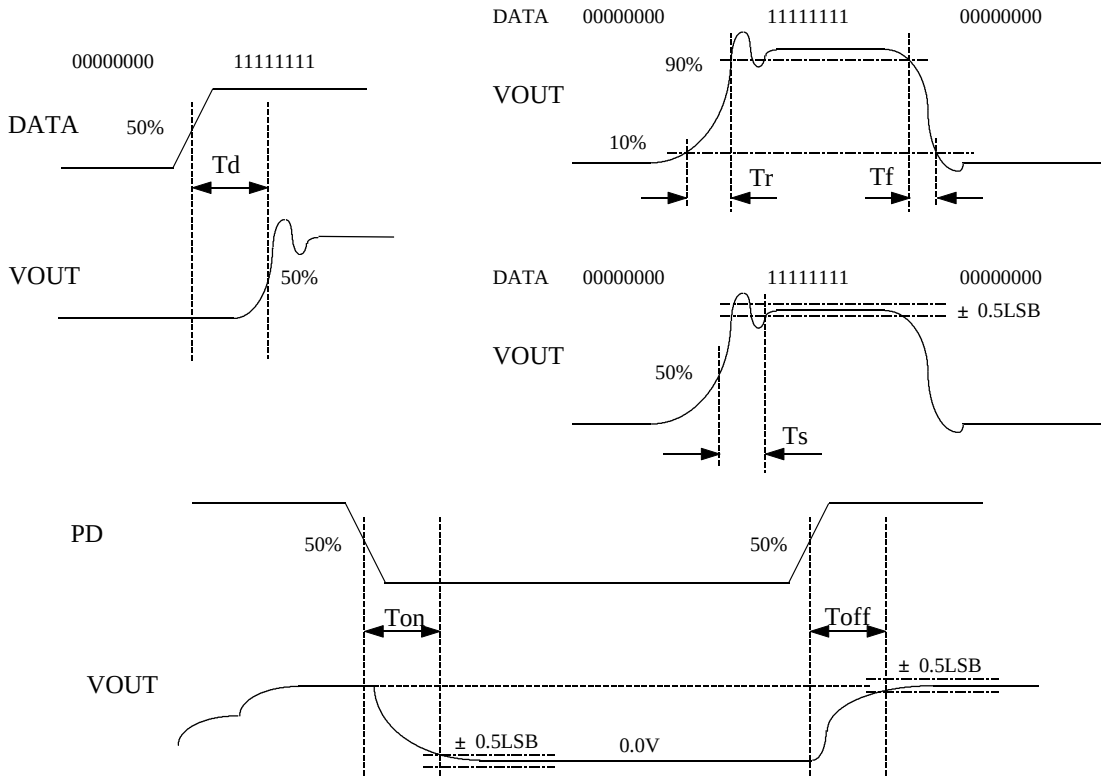
NOTE 1 : V_{ZSE}=VOUT(D[7:0]=Low) - VRB
2 : V_{FSE}=VOUT(D[7:0]=High) - {(VRT-VRB) × 255/256 + VRB}

AC ELECTRICAL CHARACTERISTICS

(Converter Specifications : AVDD25A=AVDD25D=2.5V, AVSS25A=AVSS25D=AVBB25A=0V, load cap=25pF Top=25°C, PD=High, VRT=2.45V, VRB=0.05V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Supply Current	Ivdd1	-	0.89	-	mA	Ivdd1 = $I_{VDD28AA0}$ + $I_{AVDD25D}$ VRT=2.5V , VRB = 0.0V Data Input : All Low or All High
	Ivdd2	-	1.22	-	mA	Ivdd2 = $I_{AVDD25A}$ + $I_{AVDD25D}$ Data Input : All Low or All High
Supply Current (Power Down Mode)	Ivdd3	-	-	10	uA	Ivdd3 = $I_{AVDD25A}$ + $I_{AVDD25D}$ Data Rate = 2MHz Load cap = 25pF , PWDN=LOW
Short Circuit Current	I_{SC}	-	12	-	mA	VOUT : AVSS25A or AVDD25A Data Input : All High or All Low
Analog Output Delay	Td	-	65	-	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Analog Output Rise Time	Tr	-	100	-	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Analog Output Fall Time	Tf	-	100	-	ns	Data Rate = 2MHz Data : All HIGH → All LOW
Analog Output Settling Time	Ts	-	500	-	ns	Data Rate = 2MHz Data : All LOW → All HIGH
Power Down Off Time	Ton	-	500	-	ns	PD : HIGH → LOW
Power Down On Time	Toff	-	500	-	ns	PD : LOW → HIGH

TIMING DIAGRAM



1. Output delay measured from the 50% point of the rising edge of input data to the full scale transition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within ±1/2 LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

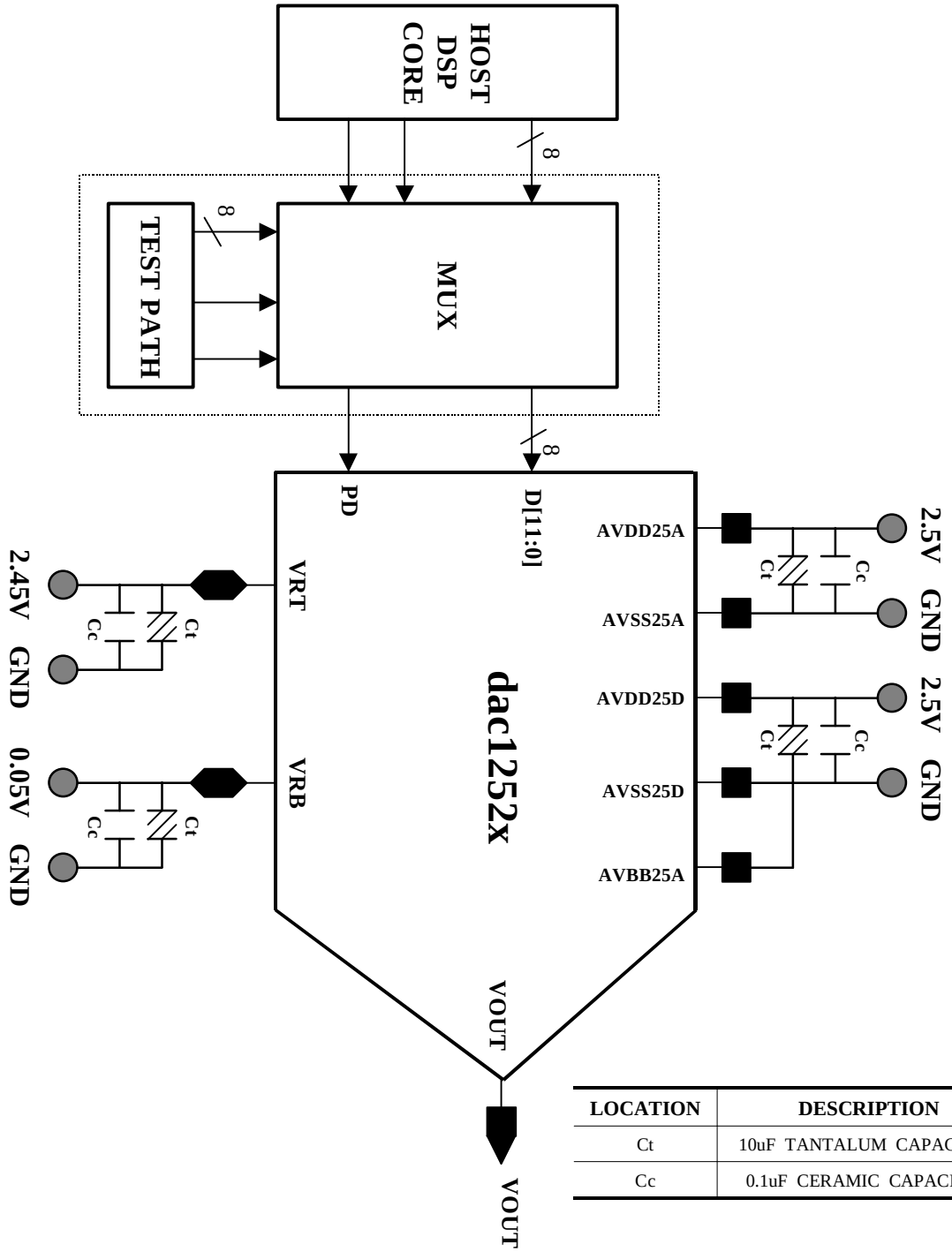
FUNCTIONAL DESCRIPTION

1. The DAC1252X has a 8BIT R-string block, two decoders, two OP amps, and control block.
2. The digital outputs of two decoders decide the voltage level of R2R block.

$$V_{Rstring} = \frac{VRT - VRB}{2^8} \sum_{n=0}^{8} (2^n * Dn)$$

3. Normal Conditions : VRT=2.45V , VRB=0.05V, PD=Low
   You can change the voltages of VRT and VRB to 2.5V and 0.0V , but the performance of DAC1252X will be degraded.

CORE EVALUATION GUIDE

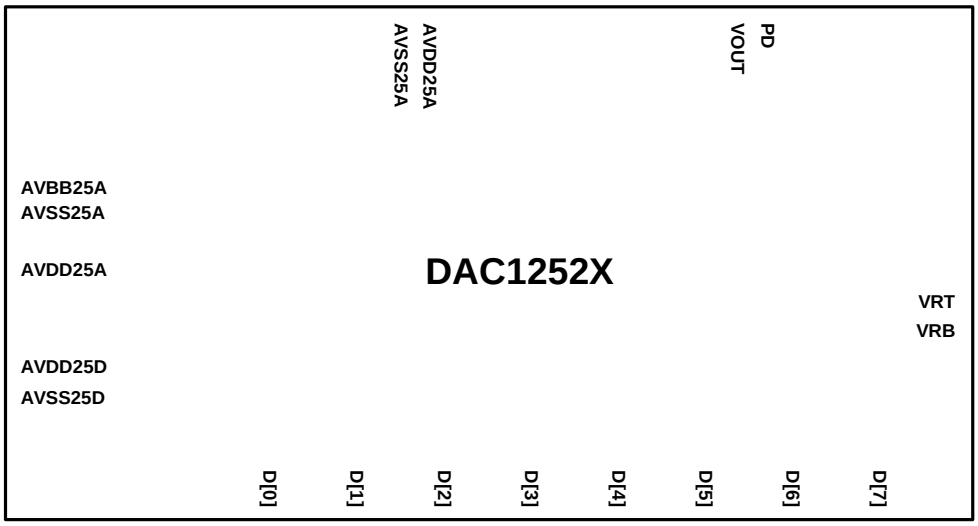


LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR

TESTABILITY

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D[7:0]).
See above figure. Only if it is, you can check the main functon. (Linearity)
Normal Test Condition : VRT=2.45V , VRB=0.05V , PD=High

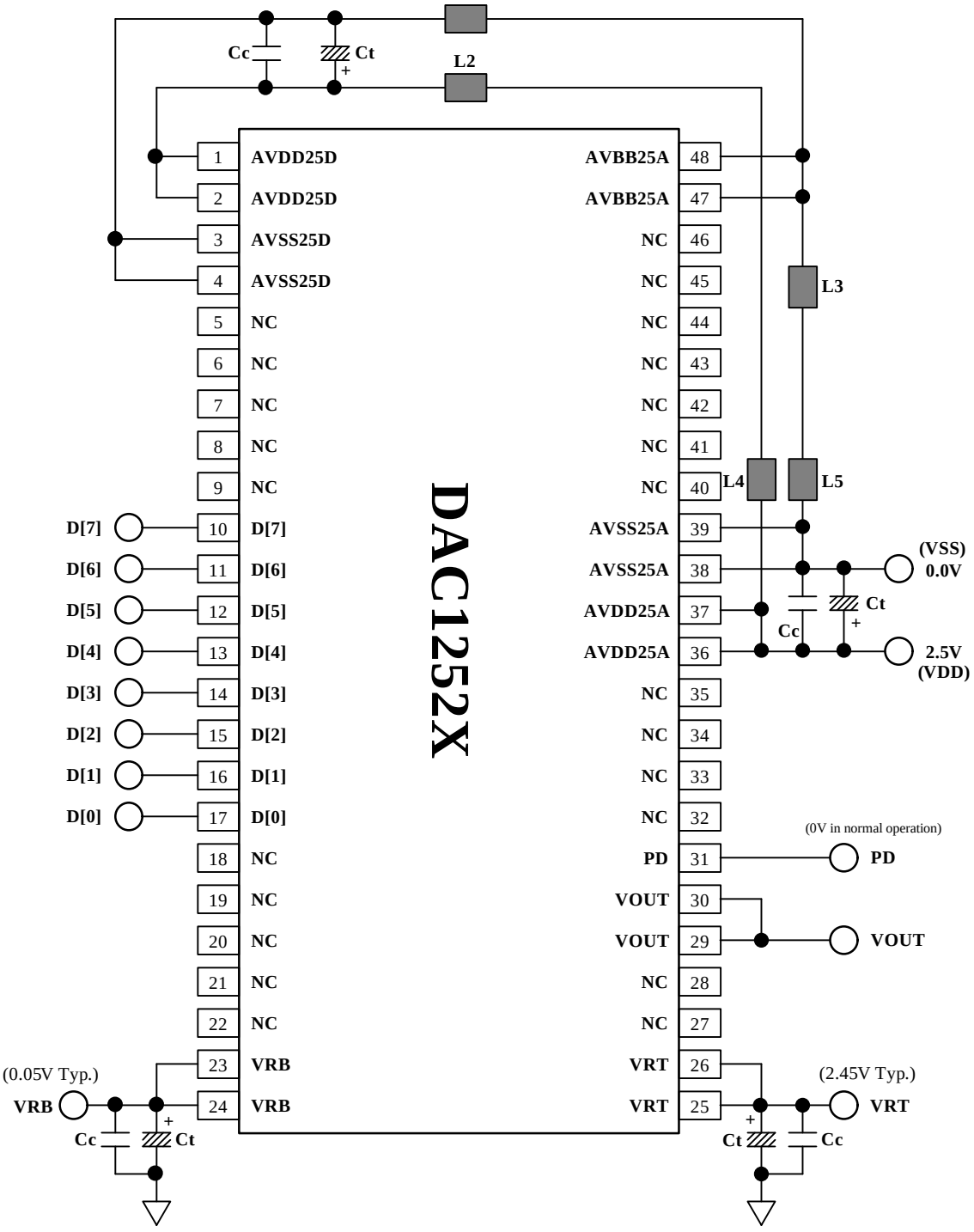
PHANTOM CELL INFORMATION



Pin Name	Property	Pin Usage	Pin Layout Guide
D[7:0]	DI	Internal / External	1. Digital Input Signal lines must have same length to reduce propagation delay.
PD	DI	Internal / External	
VRT	AB	Internal / External	1. Voltage reference lines (VRT / VRB) must be wide metal to reduce voltage drop of metal lines. 2. VOUT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.
VRB	AB	Internal / External	
VOUT	AO	Internal / External	
AVDD25A	AP	External	1. It is recommended that you use thick analog power metal. When connected to PAD, the path should be kept as short as possible. 2. Digital power and analog power are separately used.
AVSS25A	AG	External	
AVDD25D	DP	External	
AVSS25D	DG	External	
AVBB25A	AG	External	

1. When the core block is connected to other blocks, it must be double guard-ring using N-well and P+ active to remove the substrate and coupling noise.
   In that case, the power metal should be connected to PAD directly.
2. The Bulk power is used to reduce the influence of substrate noise.

PACKAGE CONFIGURATION



LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR
L1~L5	FERRITE BEAD (0.1mh)

PACKAGE PIN DESCRIPTION

NAME	PIN NO	I/O TYPE	PIN DESCRIPTION
AVDD25D	1,2	DP	Digital Power (2.5V)
AVSS25D	3,4	DG	Digital Ground (0.0V)
D[7:0]	10~17	DI	Digital Input Data
VRB	23,24	AB	Voltage Reference Bottom (0.05V)
VRT	25,26	AB	Voltage Reference Top (2.45V)
VOUT	29,30	AO	Analog Voltage Output
PD	31	DI	Power Down Mode (High Active)
AVDD25A	36,37	AP	Analog Power (2.5V)
AVSS25A	38,39	AG	Analog Ground (0.0V)
AVBB25A	47,48	AB	Analog Sub Bias (0.0V)
NC	5,6,7,8,9,18,19 20,21,22,27 28,32,33,34 35,40.41,42,43 44,45,46	DO	No Connection

I/O TYPE ABBR.

- AI : Analog Input
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- AB : Analog Bidirectional
- DB : Digital Bidirectional

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- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

PC BOARD LAYOUT CONSIDERATION

1. PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of VDD (AVDD25A,AVDD25D) and VSS (AVSS25A,AVSS25D) pins should be as short as possible so as to minimize inductive ringing.

2. Supply Decoupling and Planes

For the decoupling capacitor between the power line and the ground line, 0.1uF ceramic capacitor is used in parallel with a 10uF tantalum capacitor.
The digital power plane(AVDD25D) and analog power plane(AVDD25A) are connected through a ferrite bead, and also the digital ground plane(AVSS25D) and the analog ground plane(AVSS25A). This ferrite bead should be located within 3inches of the DAC1252X. The analog power plane supplies power to the DAC1252X of the analog output pin and related devices.

FEEDBACK REQUEST

We appreciate your interest in out products.
If you have further questions, please specify in the attached form.
Thank you very much.

DC / AC ELECTRICAL CHARACTERISTIC

Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				°C	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

VOLTAGE OUTPUT DAC

Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

CURRENT OUTPUT DAC

Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				kHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				W	
Pipeline Delay				sec	

- Do you want to Power down mode?
- Do you want to Interal Reference Voltage(BGR)?
- Which do you want to Serial Input TYPE or parallel Input TYPE?
- Do you need 3.3V and 5V power supply in your system?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.0	Aug.'98	Original version published	
Ver 2.0	Feb.'00	Power Naming convention & Core layout Guide update	
Ver 2.1	Apr.'02	Phantom Cell information update	