CALMOS™

CA82C50A

ASYNCHRONOUS COMMUNICATIONS ELEMENT

- **Single Chip UART/BRG**

- **DC to 10 MHz Operation (DC to 625K Baud)**

- **Crystal or External Clock Input**

- **On Chip Baud Rate Generator 1 to 65535 Divisor Generates 16x Clock**

- **Prioritized Interrupt Mode**

- **Fully TTL/CMOS Compatible**

- **Microprocessor Bus Oriented Interface**

- **80C86/80C88 Compatible**

- **Low Power CMOS Implementation (1 mA/MHz Typ)**

- **Modem Interface**

- **Line Break Generation and Detection**

- **Loopback Mode**

- **Double Buffered Transmitter and Receiver**

- **Single 5V Supply**

The 82C50A Asynchronous Communications Element (ACE) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. The device supports data rates from DC to 625K baud (0 - 10 MHz clock).

The ACE receiver circuitry converts start, data, stop and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity and stop bits. The word length is programmable to 5, 6, 7 or 8 data bits. Stop bit selection provides a choice of 1, 1.5 or 2 stop bits.

The Baud Rate Generator divides the clock by a divisor programmable from 1 to $2^{16}-1$ to provide standard RS-232C baud rates when using any one of three industry standard baud rate crystals (1.8432 MHz, 2.4576 MHz or 3.072 MHz). The BAUDOUT programmable clock output provides a buffered oscillator or a 16x (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals RTS, CTS, DSR, DTR, RI, DCD are provided. Inputs and outputs have been designed with full TTL/CMOS compatibility in order to facilitate mixed TTL/NMOS/CMOS system design.
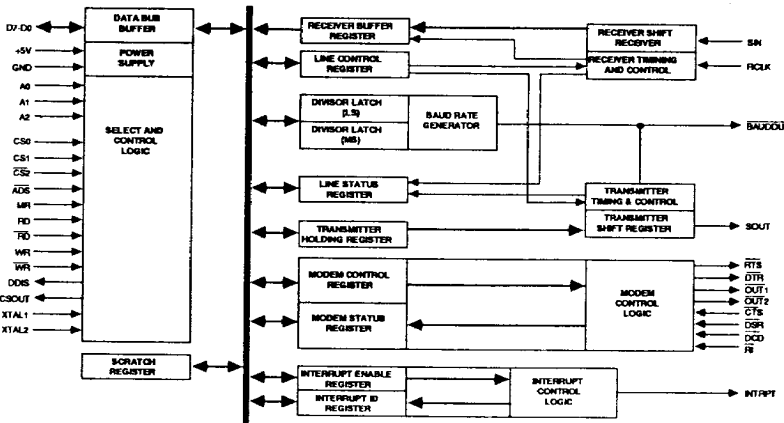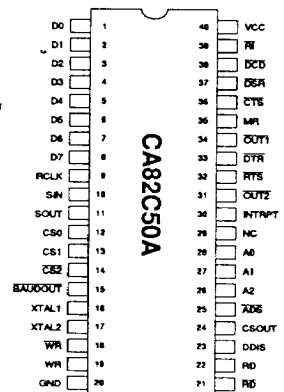

Figure 1 : BLOCK DIAGRAM OF CA82C50A

Figure 2 : PIN CONFIGURATION (40-PIN DIP)

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Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s)	Type	Name and Function
$\overline{RD}$, RD	22, 21	I	Read, Read: $\overline{RD}$, RD are read inputs which cause the CA82C50A to output data to the data bus (D_0 - D_7). The data output depends upon the register selected by the address inputs A_0, A_1 and A_2. The chip select inputs CS_0, CS_1 and $\overline{CS_2}$ enable the $\overline{RD}$, RD inputs. Only an active $\overline{RD}$ or RD, not both, is used to receive data from the CA82C50A during a read operation. If RD is used as the read input, $\overline{RD}$ should be tied high. If $\overline{RD}$ is used as the active read input, RD should be tied low.
$\overline{WR}$, WR	19,18	I	Write, Write: $\overline{WR}$, WR are write inputs which cause data from the data bus (D_0 - D_7) to be input to the CA82C50A. The data input depends upon the register selected by the address inputs A_0, A_1 and A_2. The chip select inputs CS_0, CS_1, and $\overline{CS_2}$ enable the $\overline{WR}$, WR inputs. Only an active $\overline{WR}$ or WR, not both, is used to transmit data to the CA82C50A during a write operation. If WR is used as the write input, $\overline{WR}$ should be tied high. If $\overline{WR}$ is used as the write input, WR must be tied low.
D_0 - D_7	1 - 8	I/O	Data Bus: The Data Bus provides eight 3-state input/output lines for the transfer of data, control and status information between the CA82C50A and the CPU. For character formats of less than 8 bits, D_7, D_6 and D_5 are *don't cares* for data write operations and zero for data read operations. These lines are normally in a high impedance state except during read operations. D_0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A_0, A_1, A_2	28, 27,26	I	Register Select: The address lines select the internal registers during CPU bus operations.
$XTAL_1$, $XTAL_2$	16, 17	I, O	Crystal/Clock: Crystal connections for the internal Baud Rate Generator. $XTAL_1$ can also be used as an external clock input, in which case $XTAL_2$ should be left open.
SOUT	11	O	Serial Data Output: Serial data ouputput from the CA82C50A transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SOUT is held in the Mark condition when the transmitter is disabled, MR is true, the Transmitter Register is empty, or when in the Loop Mode. SOUT is not affected by the CTS input.
V_{SS}	20	-	Ground: Power supply ground, 0V
$\overline{CTS}$	36	I	Clear to Send: An active low signal, the logical state of the $\overline{CTS}$ pin is reflected in the CTS bit of the (MSR) Modem Status Register (CTS is bit 4 of the MSR, written MSR[4]). A change of state in the CTS pin since the previous reading of the MSR causes the setting of DCTS (MSR[0]) of the Modem Status Register. When CTS is active (low), the modem is indicating that data on SOUT can be transmitted on the communications link. CTS pin does not affect Loop Mode operation.
$\overline{DSR}$	37	I	Data Set Ready: An active low signal, the logical state of the $\overline{DSR}$ pin is reflected in MSR[5] of the Modem Status Register. DDSR (MSR[1]) indicates whether the DSR pin has changed state since the previous reading of the MSR. When the DSR pin is active (low), the modem is indicating that it is ready to exchange data with the CA82C50A, while the DSR pin inactive (high) indicates that the modem is not ready for data exchange. The active condition indicates only the condition of the local Data Communications Equipment (DCE), and does not imply that a data circuit has been established with remote equipment.

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Table 1 : PIN DESCRIPTIONS con't

Symbol	Pin(s)	Type	Name and Function
$\overline{\text{DTR}}$	33	O	Data Terminal Ready: An active low signal, the $\overline{\text{DTR}}$ pin can be set (low) by writing a logic one to MCR[0], Modem Control Register bit 0. This signal is cleared (high) by writing a logic zero to the DTR bit (MCR[0]) or whenever a MR active (high) is applied to the CA82C50A. When active (low), DTR pin indicates to the DCE that the CA82C50A is ready to receive data. In some instances, DTR pin is used as a power on indicator. The inactive (high) state causes the DCE to disconnect the modem from the telecommunications circuit.
$\overline{\text{RTS}}$	32	O	Request to Send: An active low signal, $\overline{\text{RTS}}$ is an output used to enable the modem. The RTS pin is set low by writing a logic one to MCR[1] bit 1 of the Modem Control Register. The RTS pin is reset high by Master Reset. When active, the RTS pin indicates to the DCE that the CA82C50A has data ready to transmit. In half duplex operations, RTS is used to control the direction of the line.
$\overline{\text{BAUDOUT}}$	15	O	BAUDOUT: This active low output signal is a 16x clock out used for the transmitter section (16x = 16 times the data rate). The BAUDOUT clock rate is equal to the reference oscillator frequency divided by the specified divisor in the Baud Rate Generator Divisor Latches DLL and DLM. BAUDOUT may be used by the receiver section by tying this output to RCLK.
$\overline{\text{OUT1}}$	34	O	Output 1: This is an active low general purpose output that can be programmed active (low) by setting MCR[2] (OUT1) of the Modem Control Register to a high level. The OUT1 pin is set high by Master Reset. The OUT1 pin is inactive (high) during loop mode operation.
$\overline{\text{OUT2}}$	31	O	Output 2: This a an active low general purpose output that can be programmed active (low) by setting MCR[3] (OUT2) of the Modem Control Register to a high level. The OUT2 pin is set high by Master Reset. The OUT2 signal is inactive (high) during loop mode operation.
$\overline{\text{RI}}$	39	I	Ring Indicator: When low, RI indicates that a telephone ringing signal has been received by the modem or data set. The RI signal is a modem control input whose condition is tested by reading MSR[6] (RI). The Modem Status Register output TERI (MSR[2]) indicates whether the RI input has changed from a low to high since the previous reading of the MSR. If the interrupt is enabled (IER[3] = 1) and RI changes from a low to high, an interrupt is generated. The active (low) state of RI indicates that the DCE is receiving a ringing signal. RI will appear active for approximately the same length of time as the active segment of the ringing cycle. The inactive state of RI will occur during the inactive segments of the ringing cycle, or when ringing is not detected by the DCE. This circuit is not disabled by the inactive condition of DTR.
$\overline{\text{DCD}}$	38	I	Data Carrier Detect: When active (low), $\overline{\text{DCD}}$ indicates that the data carrier has been detected by the modem or data set. DCD is a modem input whose condition can be tested by the CPU by reading MSR[7] (DCD) of the Modem Status Register, MSR[3] (DDCD) of the Modem Status Register indicates whether the DCD input has changed since the previous reading of the MSR. DCD has no effect on the receiver. If the DCD changes state with the modem status interrupt enabled, an interrupt is generated. When $\overline{\text{DCD}}$ is active (low), the received line signal from the remote terminal is within the limits specified by the DCE manufacturer. The inactive (high) signal indicates that the signal is not within the specified limits, or is not present.

Table 1 : PIN DESCRIPTIONS cont

Symbol	Pin(s)	Type	Name and Function
MR	35	I	Master Reset: The MR input forces the CA82C50A into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. The CA82C50A remains in an idle state until programmed to resume serial data activities. The MR input is a TTL compatible Schmitt trigger.
INTRPT	30	O	Interrupt Request: The INTRPT output goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register: Receiver Error flag. Received Data Available, Transmitter Holding Register Empty and Modem Status. The INTRPT is reset low upon appropriate service or a MR operation.
SIN	10	I	Serial Data Input: The SIN input is the serial data input from the communication line or modem to the CA82C50A receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SIN are disabled when operating in the loop mode.
V_{DD}	40	-	Power Supply: +5V±10% DC Supply. A 0.1 μF decoupling capacitor from V_{DD} (pin 40) to V_{SS} (pin 20) is recommended.
CS_0, CS_1, $\overline{CS_2}$	12, 13, 14	I	Chip Select: The Chip Select inputs act as enable signals for the write ($\overline{WR}$, WR) and read ($\overline{RD}$, RD) input signals. The Chip select inputs are latched by the ADS input.
NC	29	-	Do Not Connect
CSOUT	24	O	Chip Select Out: When active (high), this pin indicates that the chip has been selected by active CS_0, CS_1 and $\overline{CS_2}$ inputs. No data trasfer can be initiated until CSOUT is a logic one, active (high).
DDIS	23	O	Driver Disable: This output is inactive (low) when the CPU is reading data from the CA82C50A. An active (high) DDIS output can be used to disable an external transceiver when the CPU is reading data.
$\overline{ADS}$	25	I	Address Strobe: When active (low), $\overline{ADS}$ latches the Register Select (A_0, A_1 and A_2) and Chip Select (CS_0, CS_1 and $\overline{CS_2}$) inputs. An active $\overline{ADS}$ is required when the Register Select pins are not stable for the duration of the read or write operation, multiplexed mode. If not required, the $\overline{ADS}$ input should be tied low, non-multiplexed mode.
RCLK	9	I	This input is the 16x Baud Rate Clock for the receiver section of the CA82C50A. This input may be provided from the $\overline{BAUDOUT}$ output or an external clock.

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Table 2a : AC CHARACTERISTICS: READ AND WRITE $(T_A = -40°C$ to $+85°C$, $V_{DD} = 5.0V \pm 10\%)$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
tADS	Address strobe width		50	-	ns
tAH	Address hold time		0	-	ns
tAR	RD, $\overline{RD}$ delay from address		80	-	ns
tAS	Address setup time	Note 1	60	-	ns
tAW	WR, $\overline{WR}$ delay from address		80	-	ns
tCH	Chip select hold time		0	-	ns
tCS	Chip select setup time	Note 1	60	-	ns
tCSC	Chip select output delay from select		-	125	ns
tCSR	RD, $\overline{RD}$ delay from chip select		80	-	ns
tCSW	WR, $\overline{WR}$ delay from select		80	-	ns
tDD	RD, $\overline{RD}$ to driver disable delay		-	75	ns
tDDD	Delay from RD, $\overline{RD}$ to data		-	120	ns
tDH	Data hold time		60	-	ns
tDIW	RD, $\overline{RD}$ strobe width		150	-	ns
tDOW	WR, $\overline{WR}$ strobe width		150	-	ns
tDS	Data setup time		90	-	ns
tHZ	RD, $\overline{RD}$ to floating data delay		10	75	ns
tMRW	Master reset pulse width		500	-	ns
tRA	Address hold time from RD, $\overline{RD}$		20	-	ns
tRC	Read cycle delay	Note 1	270	-	ns
tRCS	Chip select hold time from RD, $\overline{RD}$		20	-	ns
tWA	Address hold time from WR, $\overline{WR}$		20	-	ns
tWC	Write cycle delay	Note 1	270	-	ns
tWCS	Chip select hold time from WR, $\overline{WR}$		20	-	ns
tXH	Duration of clock high pulse		40	-	ns
tXL	Duration of clock low pulse		40	-	ns
RC	Read cycle = tAR + tDIW + tRC		500	-	ns
WC	Write cycle = tAW + tDOW + tWC		500	-	ns

Note: When using CA82C50A in multiplexed mode ($\overline{ADS}$ operational), its operating frequency in 80C86/88 systems is 3 MHz max.
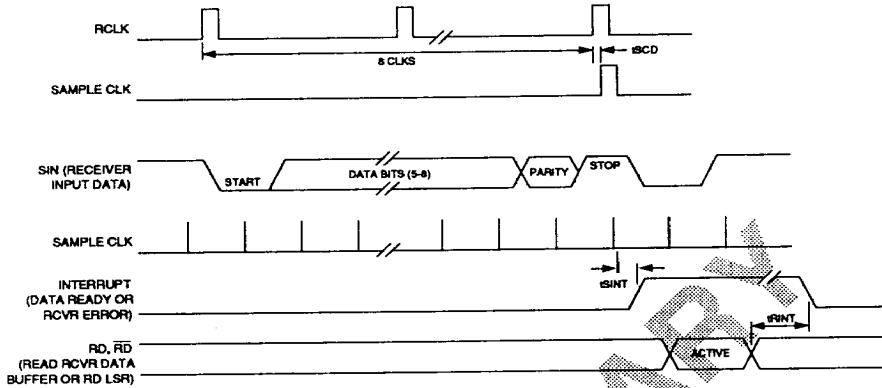
Table 2b : AC CHARACTERISTICS: BRG, RCVR, XMTR & MODEM CONTROL (T_A = –40° to +85°C, V_{DD}= 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
N	Baud divisor		1	2^{16}–1	
tBHD	Baud output positive edge delay		-	250	ns
tBLD	Baud output negative edge delay		-	250	ns
tHW	Baud output up time	t_{XL} = 50 ns	40	-	ns
tLW	Baud output down time	t_{XH} = 50 ns	40	-	ns
tRINT	Delay from RD, $\overline{RD}$ (RD RBR or RD LSR to Reset Interrupt)		-	250	ns
tSCD	Delay from RCLK to sample time		-	250	ns
tSINT	Delay from stop to Set Interrupt		-	1	$\overline{BAUDOUT}$ Cycles
tHR	Delay from WR, $\overline{WR}$ (WR THR) to Reset Interrupt		-	250	ns
tIR	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)		-	250	ns
tIRS	Delay from initial INTR reset to Transmit Start		24	40	$\overline{BAUDOUT}$ Cycles
tSI	Delay from initial write to interrupt		16	48	$\overline{BAUDOUT}$ Cycles
tSTI	Delay from stop to interrupt (THRE)		8	8	$\overline{BAUDOUT}$ Cycles
tMDO	Delay from WR, $\overline{WR}$ (WR MCR) to output		-	500	ns
tRIM	Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)		-	500	ns
tSIM	Delay to Set Interrupt from MODEM input		-	500	ns

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Figure 3 : TIMING DIAGRAMS

a) Write Cycle Timing

* Applicable only when ADS is low

b) Read Cycle Timing
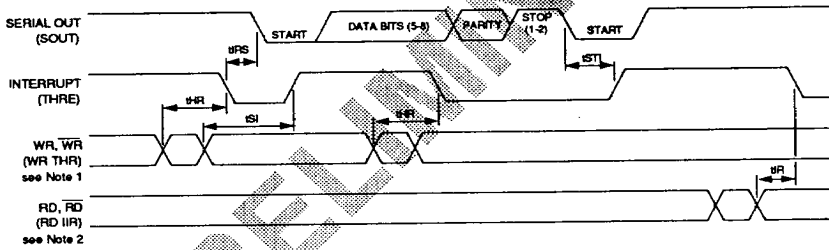

* Applicable only when ADS is low

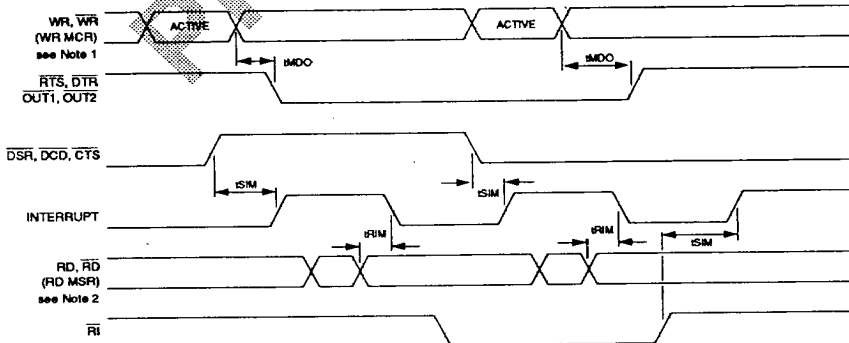## Figure 3 : TIMING DIAGRAMS con't

c) Receiver Timing

d) Transmitter Timing

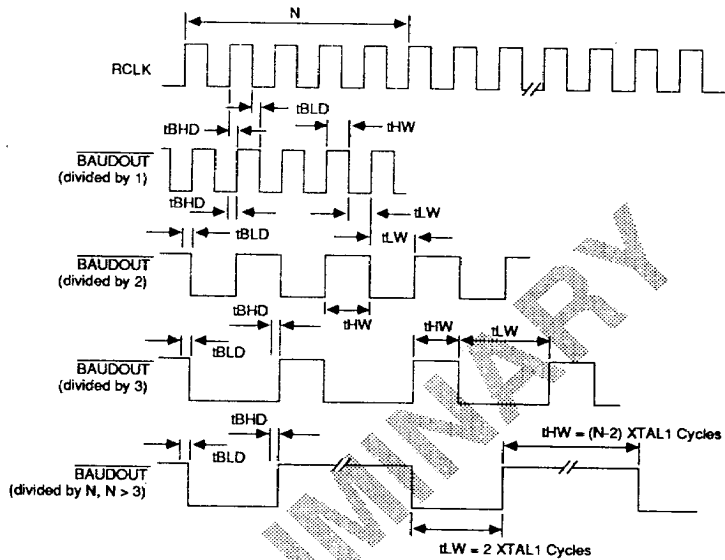
e) Modem Controls Timing

Notes: 1. See Write Cycle Timing
       2. See Read Cycle Timing

Figure 3 : TIMING DIAGRAMS con't

f) BAUDOUT Timing

Table 3 : CAPACITANCE (TA=25°C, VDD=VSS=0V, VIN=+5V or VSS)

Symbol	Parameter	Test Conditions	Typical Values	Units
C_{IN}	Input capacitance	Freq = 1 MHz	15	pF
C_{OUT}	Output capacitance	Unmeasured pins	15	pF
$C_{I/O}$	I/O capacitance	returned to Vss	20	pF

Table 4 : DC CHARACTERISTICS (T_A = –40° to +85°C, V_{DD} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
V_{IH}	Logical one input voltage		2.0	-	V
V_{IL}	Logical zero input voltage		-	0.8	V
V_{TH}	Schmitt trigger logic one input voltage	MR input	2.0	-	V
V_{TL}	Schmitt trigger logic zero input voltage	MR input	-	0.8	V
V_{IH} (CLK)	Logical one clock voltage	External Clock	V_{DD}–0.8	-	V
V_{IL} (CLK)	Logical zero clock voltage	External Clock	-	0.8	V
V_{OH}	Output high voltage	I_{OH} = –2.5 mA	3.0	-	V
		I_{OH} = –100 μA	V_{DD}–0.4	-	V
V_{OL}	Output low voltage	I_{OL} = +2.5 mA	-	0.4	V
I_I	Input leakage current	$V_{IN} = V_{SS}$ or V_{DD}	–1.0	+1.0	μA
I_O	Input/output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	–10.0	+10.0	μA
I_{DDOP}	Operating power supply current	External Clock, Freq=2.4576 MHz, V_{DD}=5.5V, $V_{IN}=V_{DD}$ or V_{SS}, Outputs open	-	6	mA
I_{DDSB}	Standby supply current	V_{DD}=5.5V, $V_{IN}=V_{DD}$ or V_{SS}, Outputs open	-	100	μA

Table 5 : OPERATING CONDITIONS

Operating Voltage Range		+4.5V to +5.5V
Operating Temperature Range	Commercial	0°C to +70°C
	Industrial	–40°C to +85°C

Table 6 : ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	V_{SS} –0.5V to V_{DD} +0.5V
Storage Temperature Range	–65°C to +150°C
Maximum Package Power Dissipation	1 Watt
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
θjc	12°C/W (Cerdip), 17°C/W (LCC)
θja	36°C/W (Cerdip), 41°C/W (LCC)

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REGISTERS

The three types of internal registers in the CA82C50A used in the operation of the device are control, status and data registers. The control registers are the Bit Rate Select Register DLL and DLM, Line Control Register, Interrupt Enable Register and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and Transmitter Holding Register. The Address, Read and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register (LCR[7]) to select the register to be written or read (see Table 7). Individual bits within these registers are referred to by the register mnemonic and the bit number in square brackets. An example, LCR[7] refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from 5 to 8 data bits. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The CA82C50A data registers are double buffered so that read and write operations can be performed at the same time the UART is performing the parallel to serial and serial to parallel conversion. This provides the microprocessor with increased flexibility in its read and write timing.

Table 7 : ACCESSING CA82C50A INTERNAL REGISTERS

Mnemonic	Register	DLAB	A2	A1	A0
RBR	Receiver Buffer Register (read only)	0	0	0	0
THR	Transmitter Holding Register (write only)	0	0	0	0
IER	Interrupt Enable Register	0	0	0	1
IIR	Interrupt Identification Register (read only)	X	0	1	0
LCR	Line Control Register	X	0	1	1
MCR	Modem Control Register	X	1	0	0
LSR	Line Status Register	X	1	0	1
MSR	Modem Control Register	X	1	1	0
SCR	Scratch Register	X	1	1	1
DLL	Divisor Latch (LSB)	1	0	0	0
DLM	Divisor Latch (MSB)	1	0	0	1

Notes: 1. X = Don't Care
2. 0 = Logic Low
3. 1 = Logic High

Line Control Register (LCR)

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described in Table 8.

LCR[0] and LCR[1] word length select bit 0, word length select bit 1: The number of bits in each transmitted or received serial character is programmed per Table 9.

LCR[2] Stop Bit Select: LCR[2] specifies the number of stop bits in each transmitted character. If LCR[2] is a logic zero, one stop bit is generated in the transmitted data. If LCR[2] is a logic one when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR[2] is a logic one when either a 6-, 7- or 8-bit word length is selected, two stop bits are generated. The receiver only checks for one stop bit.

LCR[3] Parity Enable: When LCR[3] is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR[4] Even Parity Select: When parity is enabled (LCR[3]=1), LCR[4]=0 selects odd parity, and LCR[4]=1 selects even parity.

LCR[5] Stick Parity: When LCR[3, 4 and 5] are logic one the Parity bit is transmitted and checked as a logic zero. If

LCR[3 and 5] are one and LCR[4] is a logic zero then the parity bits is transmitted and checked as a logic one. If LCR[5] is a logic zero Stick Parity is disabled.

LCR[6] Break Control: When LCR[6] is set to logic one, the serial output (SOUT) is forced to the spacing (logic zero) state. The break is disabled by setting LCR[6] to logic zero. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s pad character in response to THRE.

2. Set break in response to the next THRE.

3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

LCR[7] Divisor Latch Access Bit (DLAB): LCR[7] must be set high (logic one) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR[7] must be input low to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Table 8 : LCR BIT DEFINITIONS

Bit Number	Function
0	Word Length Select Bit 0 (WLS0)
1	Word Length Select Bit 1 (WLS1)
2	Stop Bit Select (STB)
3	Parity Enable (EN)
4	Even Parity Select (EPS)
5	Stick Parity
6	Set Break
7	Divisor Latch Access Bit (DLAB)

Table 9 : LCR WORD LENGTH SELECTION

LCR[1]	LCR[2]	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits
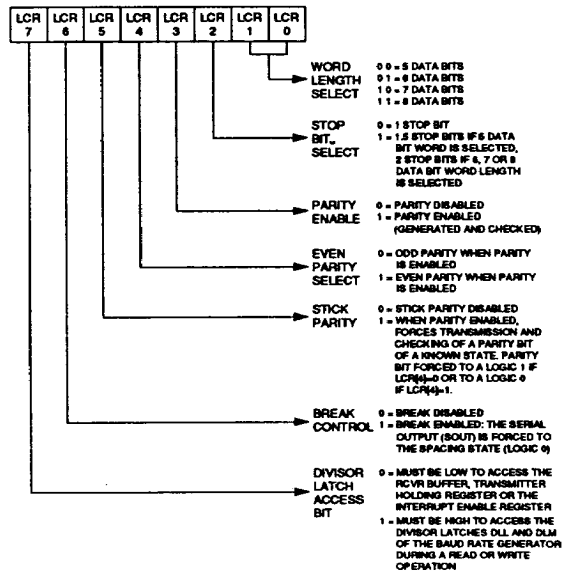
Figure 4 : LINE CONTROL REGISTER

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Line Status Register (LSR)

The LSR is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the CA82C50A.

Three error flags OE, FE and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last charater only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character, with the entire character, including parity and stop bits, logic zero.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and ready to receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the CA82C50A has completed transmission of the last character. If the interrupt is enabled (IER[1]), an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (included Break) and that the CPU may access this data.

Reading LSR clears LSR[1] - LSR[4], (OE, PE, FE and BI).

The contents of the Line Status Register are indicated in Table 10, and are described below.

LSR[0] Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR[0] is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR[1] Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR[2] Parity Error (PE): PE indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR[4]). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR[3] Framing Error (FE): FE indicates that the received character did not have a valid stop bit. LSR[3] is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR[4] Break Interrupt (BI): BI is set high when the received data input is held in the spacing (logic zero) state for longer than a full word transmission time (start bit+data bits+parity+stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR[1] – LSR[4] are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER[2]=1 in the Interrupt Enable Register.

LSR[5] Transmitter Holding Register Empty (THRE): THRE indicates that the CA82C50A is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR[5] is reset low when the CPU loads the Transmitter Holding Register. LSR[5] is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER[1]=1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR[6] Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR[6] is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR[7]: This bit is permanently set to logic zero.

Table 10 : LSR BIT DEFINITIONS

Bit #	Function	Logic 1	Logic 0
0	Data Ready (DR)	Ready	Not Ready
1	Overrun Error (OE)	Error	No Error
2	Parity Error (PE)	Error	No Error
3	Framing Error (FE)	Error	No Error
4	Break Interrupt (BI)	Break	No Break
5	Transmitter Holding Register Empty (THRE)	Empty	Not Empty
6	Transmitter Empty (TEMT)	Empty	Not Empty
7	Not Used		

Modem Control Register (MCR)

The MCR controls the interface with the modem or data set as described below. The MCR can be written and read. The $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$ and $\overline{OUT2}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins.

MCR[0]: When MCR[0] is set high, the $\overline{DTR}$ output is forced low. When MCR[0] is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the CA82C50A may be input into an EIA inverting line driver such as a 1488 to obtain the proper polarity input at the modem or data set.

MCR[1]: When MCR[1] is set high, the $\overline{RTS}$ output is forced low. When MCR[1] is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the CA82C50A may be input into an EIA inverting line driver such as a 1488 to obtain the proper polarity input at the modem or data set.

MCR[2]: When MCR[2] is set high, the $\overline{OUT1}$ output is forced low. When MCR[2] is reset low, the $\overline{OUT1}$ output is forced high. $\overline{OUT1}$ is a user designated output.

MCR[3]: When MCR[3] is set high, the $\overline{OUT2}$ output is forced low. When MCR[3] is reset low, the $\overline{OUT2}$ output is forced high. $\overline{OUT2}$ is a user designated output.
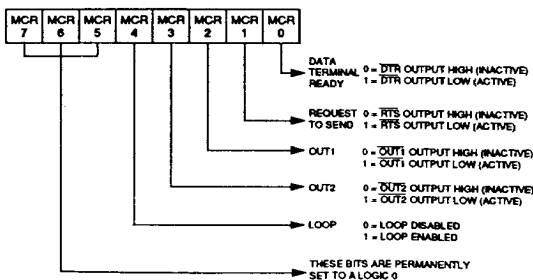
MCR[4]: MCR[4] provides a local loopback feature for diagnostic testing of the CA82C50A. When MCR[4] is set high. Serial Output (SOUT) is set to the marking (logic one) state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the CPU to verify CA82C50A transmit and receive data paths.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. The interrupts are still controlled by the Interrupt Enable Register.

MCR[5] – MCR[7]: Bits are permanently set to logic zero.

Table 11 : MCR BIT DEFINITIONS

Bit #	Function	Logic 1	Logic 0
0	Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
1	Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
2	OUT1	$\overline{OUT1}$ Output Low	$\overline{OUT1}$ Output High
3	OUT2	$\overline{OUT2}$ Output Low	$\overline{OUT2}$ Output High
4	LOOP	LOOP Enabled	LOOP Disabled
5, 6, 7	0		

Figure 5 : MODEM CONTROL REGISTER

Modem Status Register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral device. The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the CA82C50A. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$ (pin 36), $\overline{DSR}$ (pin 37), $\overline{RI}$ (pin 39) and $\overline{DCD}$ (pin 38). MSR[4] – MSR[7] are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled (IER[3]), a change of state in a modem input signal will be reflected by the modem status bits in the IIR register and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The Modem Status Register is described in Table 12.

Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

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MSR[0] Delta Clear to Send (DCTS): DCTS indicates that the CTS input (pin 36) to the CA82C50A has changed state since the last time it was read by the CPU.

MSR[1] Delta Data Set Ready (DDSR): DDSR indicates that the DSR input (pin 37) to the CA82C50A has changed state since the last time it was read by the CPU.

MSR[2] Trailing Edge of Ring Indicator (TERI): TERI indicates that RI input (pin 39) to CA82C50A has changed state (L→H) since it was last read by the CPU.

MSR[3] Delta Data Carrier Detect (DDCD): DDCD indicates that the DCD input (pin 38) to the CA82C50A has changed state since the last time it was read by the CPU.

MSR[4] Clear to Send (CTS): CTS is the status of the CTS input (pin 36) from the modem indicating to the CA82C50A that the modem is ready to receive data from the transmitter output (SOUT). If the CA82C50A is in the loop mode (MCR[4]=1), MSR[4] is equivalent to RTS in the MCR.

MSR[5] Data Set Ready (DSR): This is the status of DSR input (pin 37) from modem to CA82C50A which indicates that the modem is ready to provide received data to the receiver circuitry. If the CA82C50A is in loop mode, (MCR[4]=1), MSR[5] is equivalent to DTR in the MCR.

MSR[6] Ring Indicator (RI): RI indicates the status of the RI input (pin 39). If the CA82C50A is in the loop mode (MCR[4]=1), MSR[6] is equivalent to OUT1 in the MCR.

MSR[7] Data Carrier Detect (DCD): DCD indicates the status of the Data Carrier Detect (DCD) input (pin 38). If the CA82C50A is in the loop mode (MCR[4]=1), MSR[4] is equivalent to OUT2 of the MCR.

The modem status inputs (RI, DCD, DSR and CTS) reflect the modem input lines. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI or DDCD are true and a state change occurs during a read (RD, RD), the state change is not indicated in the MSR. If DCTS, DDSR, TERI or DDCD are false and a state change occurs during a read, the state change is indicated after the read.

For LSR and MSR, setting of status bits is inhibited during status register read (RD, RD) operations. If a status condition is generated during a read (RD, RD), the status bit is not set until the trailing edge of the read (RD, RD).

If a status bit is set during a read (RD, RD, and the same status condition occurs, that status bit will be cleared at the read (RD, RD) trailing edge, instead of being set again.

Table 12 : MSR BIT DEFINITIONS

Bit #	Function
0	Delta Clear to Send (DCTS)
1	Delta Data Set Ready (DDSR)
2	Trailing Edge of Ring Indicator (TERI)
3	Delta Data Carrier Detect (DDCD)
4	Clear to Send (CTS)
5	Data Set Ready (DSR)
6	Ring Indicator (RI)
7	Data Carrier Detect (DCD)

Baud Rate Select Register (BRSR)

A programmable Baud Rate Generator (BRG) divides the clock by any divisor from 1 to $2^{16}-1$ (see BRG description). The BRG output frequency is 16x the data rate:

Divisor # = Frequency Input ÷ (Baud Rate x 16)

Two 8-bit Divisor Latch Registers store the divisor in 16-bit binary format and *must* be loaded during initialization. When either register is loaded, a 16-bit baud counter is also immediately loaded, to prevent long counts on initial load.

Sample Divisor Number Calculation:

Given: Desired Baud Rate 1200 Baud
          Frequency Input 1.8432 MHz
Formula: Divisor # = Frequency Input ÷ (Baud Rate x 16)
          Divisor # = 1843200 ÷ (1200 x 16)
Answer: Divisor # = 96 = 60$_{HEX}$ → DLL = 01100000
                                        DLM = 00000000
Check: Divisor #96 will divide the input frequency 1.8432 MHz down to 19200 which is 16 times the desired baud rate.

Table 13: DIVISOR LATCH BIT DEFINITIONS

Least Significant Bit		Most Significant Bit	
Bit #	Function	Bit #	Function
0	DLL[0]	8	DLM[0]
1	DLL[1]	9	DLM[1]
2	DLL[2]	10	DLM[2]
3	DLL[3]	11	DLM[3]
4	DLL[4]	12	DLM[4]
5	DLL[5]	13	DLM[5]
6	DLL[6]	14	DLM[6]
7	DLL[7]	15	DLM[7]

Receiver Buffer Register (RBR)

The receiver circuitry in the CA82C50A is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit (LSB = Data Bit 0, RBR[0]). Data Bit 0 of a data word (RBR[0]) is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the CA82C50A.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16x clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the CA82C50A, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

Table 14 : RBR BIT DEFINITIONS

Bit #	Function
0	Data - RBR[0]
1	Data - RBR[1]
2	Data - RBR[2]
3	Data - RBR[3]
4	Data - RBR[4]
5	Data - RBR[5]
6	Data - RBR[6]
7	Data - RBR[7]

Transmitter Holding Register (THR)

The Transmitter Holding Register (THR) holds parallel data from the data bus ($D_0 - D_7$) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 (THR[0]) is the first serial data bit transmitted. The THRE flag (LSR[5]) reflects the THR status, the TEMT flag (LSR[5]) indicates if both THR and TSR are empty.

Table 15 : THR BIT DEFINITIONS

Bit Number	Function
0	Data - THR[0]
1	Data - THR[1]
2	Data - THR[2]
3	Data - THR[3]
4	Data - THR[4]
5	Data - THR[5]
6	Data - THR[6]
7	Data - THR[7]

Scratchpad Register (SCR)

This 8-bit Read/Write register has no effect on the CA82C50A. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Table 16 : SCR BIT DEFINITIONS

Bit #	Function
0	Data - SCR[0]
1	Data - SCR[1]
2	Data - SCR[2]
3	Data - SCR[3]
4	Data - SCR[4]
5	Data - SCR[5]
6	Data - SCR[6]
7	Data - SCR[7]

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INTERRUPT STRUCTURE

Interrupt Identification Register (IIR)

The CA82C50A has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the CA82C50A prioritizes interrupts into four levels:

- Receiver Line Status (priority 1)
- Received Data Ready (priority 2)
- Transmitter Holding Register Empty (priority 3)
- Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 17 and are described below.

IIR[0]: IIR[0] can be used in either a hardwired prioritized or polled environment to indicate if an interrupt is pending. When IIR[0] is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When it is high, no interrupt is pending.

IIR[1] and IIR[2]: IIR[1] and IIR[2] are used to identify the highest priority interrupt pending as indicated in Table 17.

IIR[3] – IIR[7]: These five bits of the IIR are logic zero.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) is a Write register used to independently enable the four CA82C50A interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER[0] – IER[3] of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 18 and are described below.

IER[0]: When programmed high (IER[0] = Logic 1), IER[0] enables Received Data Available interrupt.

IER[1]: When programmed high (IER[1] = Logic 1), IER[1] enables the Transmitter Holding Register Empty interrupt.

IER[2]: When programmed high (IER[2] = Logic 1), IER[2] enables the Receiver Line Status interrupt.

IER[3]: When programmed high (IER[3] = Logic 1), IER[3] enables the Modem Status interrupt.

IER[4] – IER[7]: These four bits of the IER are logic zero.

Table 17 : INTERRUPT IDENTIFICATION REGISTER

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE or BI	LSR Read
1	0	0	Second	Received Data Available	Receiver Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is interrupt source or THR Write
0	0	0	Fourth	Modem Status	C̄T̄S̄, D̄S̄R̄, R̄I, D̄C̄D̄	MSR Read

Note: X - Don't Care

Table 18 : REGISTER SUMMARY

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)[1]
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	EDSSI (Enable Modem Status Interrupt)	ELSI (Enable Receiver Line Status Interrupt)	ETBEI (Enable Transmitter Holding Register Empty Interrupt)	ERBFI (Enable Received Data Available Interrupt)
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit 1	Interrupt ID Bit 0	'0' - if Interrupt Pending
LCR	DLAB (Divisor Latch Access Bit)	Set Break	Stick Parity	EPS (Even Parity Select)	PEN (Parity Enable)	STB (Number of Stop Bits)	WLSB1 (Word Length Select) Bit 1	WLSB0 (Word Length Select) Bit 0
MCR	0	0	0	LOOP	OUT2	OUT1	RTS (Request to Send)	DTR (Data Terminal Ready)
LSR	0	TEMT (Transmitter Empty)	THRE (Transmitter Holding Register Empty)	BI (Break Interrupt)	FE (Framing Error)	PE (Parity Error)	OE (Overrun Error)	DR (Data Ready)
MSR	DCD (Data Carrier Detect)	RI (Ring Indicator)	DSR (Data Set Ready)	CTS (Clear to Send)	DDCD (Delta Data Carrier Detect)	TERI (Trailing Edge Ring Indicator)	DDSR (Delta Data Set Ready)	DCTS (Delta Clear to Send)
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Note: 1. LSB, Data Bit 0 is the first bit transmitted or received

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DR (LSR[0])
ERBFI (IER[0])

THRE (LSR[5])
ETBEI (IER[1])

INTRPT
PIN 30

OE (LSR[1])
PE (LSR[2])
FE (LSR[3])
BI (LSR[4])
ELSI (IER[2])

DCTS (MSR[0])
DDSR (MSR[1])
TERI (MSR[2])
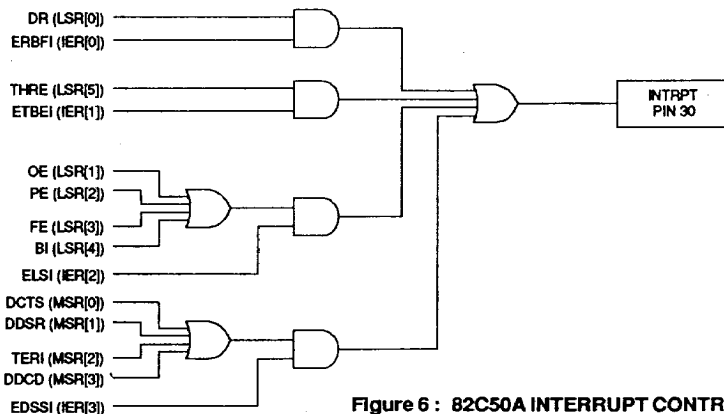DDCD (MSR[3])
EDSSI (IER[3])

Figure 6 : 82C50A INTERRUPT CONTROL STRUCTURE

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR). Transmitter Shift Register (TSR) and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5 – 8 bit word, the word is written through D_0 - D_7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word written causes THRE to be reset to zero. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a H → L transition from the idle state. When a transition is detected, a counter is reset, and counts the 16x clock to $7^1/_2$, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid bit sample of the start bit. The start bit is verified to prevent the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR[0], LCR[1]), number of stop bits LCR[2], if parity is used LCR[3], and the polarity of parity LCR[4]. Status information for the receiver is provided in the Line Status Register. When a character is transferred from the Receiver Shift Register to the Receiver Buffer Register, the Data Received indication in LSR[0] is set high. The CPU reads the Receiver Buffer Register through D_0 - D_7. Thes read resets LSR[0]. If D_0 - D_7 are not read prior to a new character transfer from the RSR to RBR, the overrun error status indication is set in LSR[1]. The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR[2]. There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR[3].

The center of the start bit is defined as clock count $7^1/_2$. If data into the SIN is a symmetrical square wave, the data cell centers will occur within ±3.125% of the actual center, giving an error margin of 46.875%. The start bit can begin as much as one 16x clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, at standard ANSI/CCITT bit rates. The oscillator driving the BRG may be provided with an external crystal to the $XTAL_1$ and $XTAL_2$ pins, or an external clock into $XTAL_1$. In either case, a buffered clock output, $\overline{BAUDOUT}$ is provided for other system clocking. If two CA82C50As are used on the same board, one can use a crystal, with the buffered clock output routed directly to $XTAL_1$ of the other CA82C50A.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency or crystal input, with the $\overline{BAUDOUT}$ providing an output 16x the data rate. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at $XTAL_1$). The on-chip oscillator is optimized for a 10 MHz crystal.

The BRG can use any of three different popular crystals to provide standard baud rates. The frequency of these three common crystals on the market are 1.8432 MHz, 2.4576 MHz and 3.072 MHz. With these standard crystals, standard bit rates from 50 to 38.4 kbps are available. The following tables illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

Table 19 : BAUD RATES WITH 1.8432 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

Table 20 : BAUD RATES WITH 2.4576 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

Table 21 : BAUD RATES WITH 3.072 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

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Reset

After powerup, the CA82C50A Master Reset schmitt trigger input (MR) should be held high for TMRW ns to reset the CA82C50A circuits to an idle mode unitl initialization. A high on MR causes the following:

• Initialize transmitter and receiver internal clock counters.

• Clear Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. Modem Control Register (MCR) and Line Control Register (LCR) are also cleared. All discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not affected.

Following removal of the reset condition (MR low), the CA82C50A remains in the idle mode until programmed.

A hardware reset of the CA82C50A sets THRE and TEMT status bits in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

Table 22 gives a summary of the effects of a Master Reset on the CA82C50A.

Table 22 : RESET OPERATIONS

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced, 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	Bits 5 and 6 High, all other Bits Low
MODEM Status Register	Master Reset	Bits 0-3 Low, Bits 4-7 Input Signal
SOUT	Master Reset	High
Interrupt (RCVR Errors)	Read LSR/MR	Low
Interrupt (RCVR Data Ready)	Read RBR/MR	Low
Interrupt (THRE)	Read IIR, Write THR/MR	Low
Interrupt (Modem Status Changes)	Read MSR/MR	Low
OUT2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT1	Master Reset	High

PROGRAMMING

The CA82C50A is programmed by the control registers LCR, IER, DLL, DLM and MCR. These control words define the character length, number of stop bits, parity, baud rate and modem interface.

While the Control registers can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the CA82C50A is programmed and operational, these registers can be updated any time the CA82C50A is not transmitting or receiving data.

Software Reset

A software reset of the CA82C50A is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Crystal Operation

The CA82C50A crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. Table 23 shows the required crystal parameters and crystal circuit configuration, respectively.

When using an external clock source, the $XTAL_1$ input is driven and the $XTAL_2$ output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

The maximum frequency of the CA82C50A is 10 MHz with an external clock or a crystal attached to $XTAL_1$ and $XTAL_2$. Using the external clock or crystal, and a divide by one divisor, the maximum $\overline{BAUDOUT}$ is 10 MHz and the maximum data rate is 625 kbps.

Table 23 : TYPICAL CRYSTAL OSCILLATOR CIRCUIT

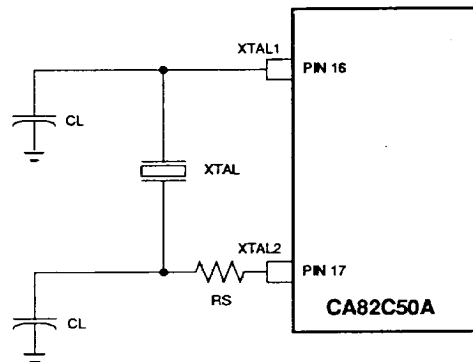| Parameter	
Frequency	1.0 to 10 MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance (C_L)	20 or 32 pF (typical)
R_{SERIES} (Max)	100 Ω (f = 10 MHz, C_L = 32 pF) 200 Ω (f = 10 MHz, C_L = 20 pF)

Figure 7 : CRYSTAL OSCILLATOR CIRCUIT

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