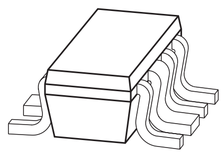
GaAs MMIC

CGY 196

Data Sheet

- Multiband Power Amplifier [800 … 3500 MHz]
- DECT, PHS, PWT, Bluetooth, ISM900, ISM2400, WLL
- Single Voltage Supply
- Operating voltage range: 2 V to 6 V
- P_{OUT} = 25.5 dBm at V_D = 2.4 V
- P_{OUT} = 26.0 dBm at V_D = 3.0 V
- P_{OUT} = 29.0 dBm at V_D = 5.0 V
- Overall power added efficiency up to 50%
- Easy external matching



SCT-598

ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	**Marking**	**Ordering Code** (taped)	**Package**
CGY 196	D6s	Q62702-G0080	SCT-598

Maximum Ratings

Parameter	**Symbol**	**Value**	**Unit**
Positive supply voltage	V_D	6	V
Supply current	I_D	1.0	A
Maximum input power	P_{IN_max}	20	dBm
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	– 55 … + 150	°C
Total power dissipation ($T_S \leq$ 80 °C) T_S: Temperature at soldering point	P_{tot}	1.0	W
Pulse peak power	P_{Pulse}	2.0	W

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel-soldering point	R_{thChS}	70	K/W

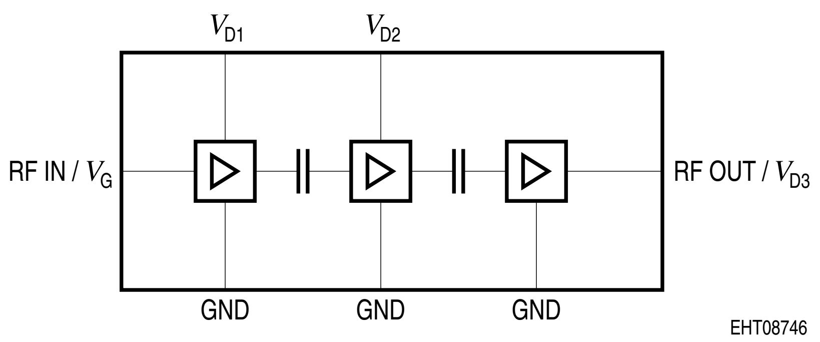


Figure 1 Functional Block Diagram

Pin Configuration

Pin No.	Symbol	Configuration
1	RF IN/V_G	RF input power + Gate voltage [0 V internal]
2	GND	RF and DC ground
3	V_{D2}	Pos. drain voltage of the 2nd stage
4	N.C.	Not connected
5	N.C.	Not connected
6	RF OUT/V_{D3}	RF output power/Pos. drain voltage of the 3rd stage
7	GND	RF and DC ground
8	V_{D1}	Pos. drain voltage of the 1st stage

DC Characteristics

Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Drain current stage 1 - 3	I_{DSS1}	30	45	75	mA	V_{D1} = 3 V
	I_{DSS2}	45	65	110	mA	V_{D2} = 3 V
	I_{DSS3}	230	340	515	mA	V_{D3} = 3 V
Transconductance stage 1 - 3	G_{FS1}	50	90	130	mS	V_D = 3 V, I_D = 50 mA
	G_{FS2}	80	130	170	mS	V_D = 3 V, I_D = 300 mA
	G_{FS3}	150	220	300	mS	V_D = 3 V, I_D = 300 mA

Determination of Permissible Total Power Dissipation for Continuous and Pulse Operation

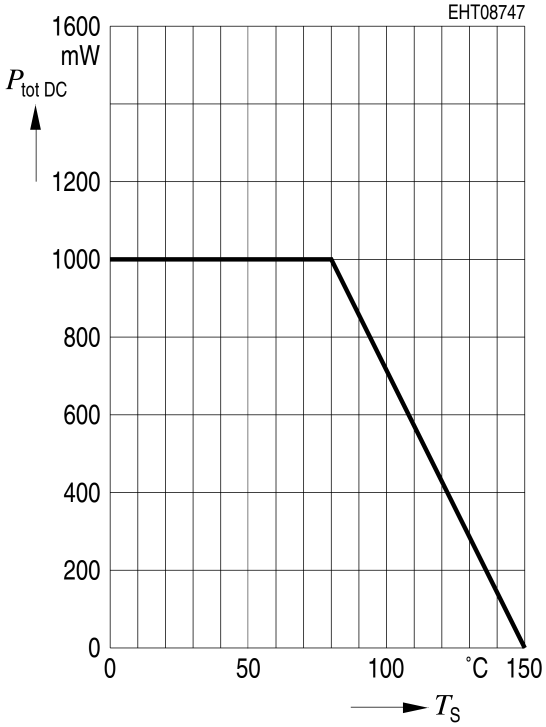
The dissipated power is the power which remains in the chip and heats the device. It does not contain RF signals which are coupled out consistently.

a) Continuous Wave/DC Operation

For the determination of the permissible total power dissipation $P_{tot\text{-}DC}$ from the diagram below it is necessary to obtain the temperature of the soldering point T_S first. There are two cases:

- When R_{thSA} (soldering point to ambient) is not known: Measure T_S with a temperature sensor at the leads were the heat is transferred from the device to the board (normally at the widest source or ground lead for GaAs). Use a small sensor of low heat transport, for example a thermoelement (< 1 mm) with thin wires or a temperature indicating paper while the device is operating.
- When R_{thSA} is already known: $T_S = P_{Diss} \times R_{thSA} + T_A$

Permissible Total Power Dissipation in DC Operation



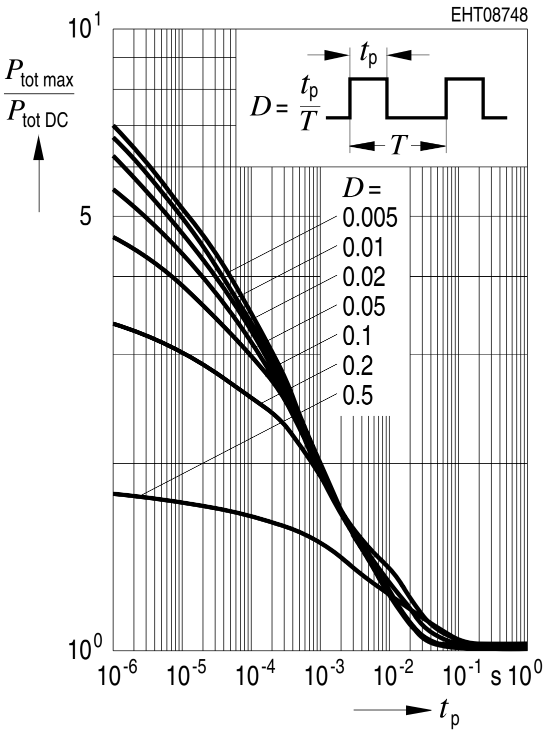
b) Pulsed Operation

For the calculation of the permissible pulse load $P_{\text{tot-max}}$ the following formula is applicable:

$P_{\text{tot-max}} = P_{\text{tot-DC}} \times \text{Pulse factor} = P_{\text{tot-DC}} \times (P_{\text{tot-max}}/P_{\text{tot-DC}})$

Use the values for $P_{\text{tot-DC}}$ as derived from the above diagram and for the pulse factor = $P_{\text{tot-max}}/P_{\text{tot-DC}}$ from the following diagram to get a specific value.

Pulse Factor



$P_{tot\text{-}max}$ should not exceed the absolute maximum rating for the dissipated power

P_{Pulse} = "Pulse peak power" = 2 W

c) Reliability Considerations

This procedure yields the upper limit for the power dissipation for continuous wave (cw) and pulse applications which corresponds to the maximum allowed channel temperature. For best reliability keep the channel temperature low. The following formula allows to track the individual contributions which determine the channel temperature.

T_{Ch} =	(P_{Diss}/Pulse Factor ×	R_{thChS}) +	T_S
Channel temperature (= junction temperature)	Power dissipated in the chip, divided by the applicable pulse factor (= 1 for DC and CW). It does not contain decoupled RF-power	R_{th} of device from channel to soldering point	Temperature of soldering point, measured or calculated

Electrical Characteristics, 3.0 V DECT-Application, f = 1.89 GHz
T_A = 25 °C, f = 1.89 GHz, Z_S = Z_L = 50 Ω, unless otherwise specified

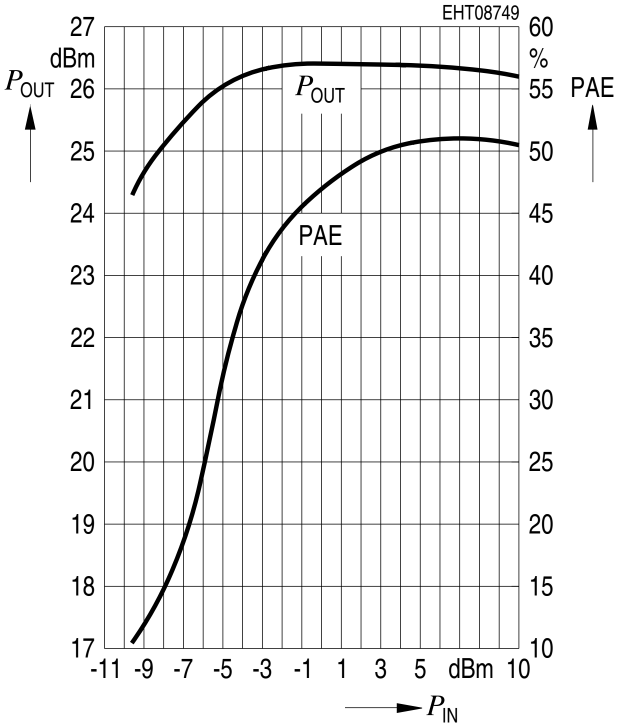
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_{DD}	–	300	500	mA	V_D = 3.0 V; P_{IN} = + 0 dBm
Supply current	I_{DD}	–	450	700	mA	V_D = 3.0 V; P_{IN} = – 10 dBm
Gain	G	27	30	33	dB	V_D = 3.0 V; P_{IN} = – 10 dBm
Output Power	P_O	24.0	26.0	27.0	dBm	V_D = 3.0 V; P_{IN} = 0 dBm
Overall Power added Efficiency	PAE	35	45	–	%	V_D = 3.0 V; P_{IN} = + 0 dBm
Overall Power added Efficiency	PAE	–	50	–	%	V_D = 3.0 V; P_{IN} = 3 dBm
Supply current	I_{DD}	–	450	–	mA	V_D = 4.8 V; P_{IN} = – 10 dBm
Supply current	I_{DD}	–	330	600	mA	V_D = 4.8 V; P_{IN} = 0 dBm
Gain	G	–	32	–	dB	V_D = 4.8 V; P_{IN} = – 10 dBm
Output Power	P_O	26.5	28	30	dBm	V_D = 4.8 V; P_{IN} = 3 dBm
Overall Power added Efficiency	PAE	30	40	–	%	V_D = 4.8 V; P_{IN} = 3 dBm
Overall Power added Efficiency	PAE	–	45	–	%	V_D = 4.8 V; P_{IN} = 5 dBm
Off Isolation	-S21	–	40	–	dB	V_D = 0 V; P_{IN} = 0 dBm
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 0 dBm, $V_D \leq$ 3.6 V, Z_S = 50 Ω Load VSWR = 20:1 for all phase

Electrical Characteristics, 3.0 V DECT-Application, f = 1.89 GHz (cont'd)
T_A = 25 °C, f = 1.89 GHz, $Z_S = Z_L$ = 50 Ω, unless otherwise specified

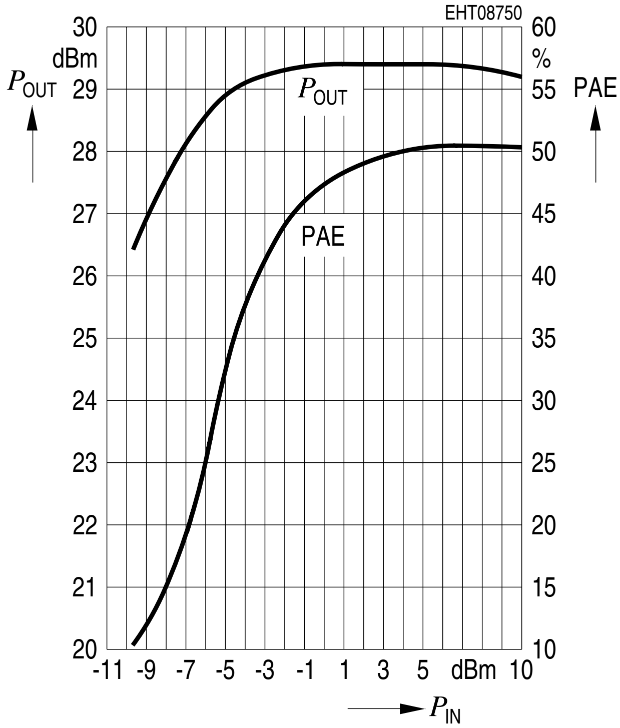
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 3 dBm, $V_D \leq 5.0$ V, Z_S = 50 Ω Load VSWR = 20:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level.			–	P_{IN} = 0 dBm, $V_D \leq 3.6$ V, Z_S = 50 Ω Load VSWR = 10:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level.			–	P_{IN} = 3 dBm, $V_D \leq 5.0$ V, Z_S = 50 Ω Load VSWR = 10:1 for all phase

Electrical Characteristics (3.0 V DECT-Application, f = 1.89 GHz)

Output Power and Power Added Efficiency, V_D = 3.3 V, duty cycle 10%



Output Power and Power Added Efficiency, V_D = 5.0 V, duty cycle 10%



pulsed mode: T = 417 µs, duty cycle 12.5%

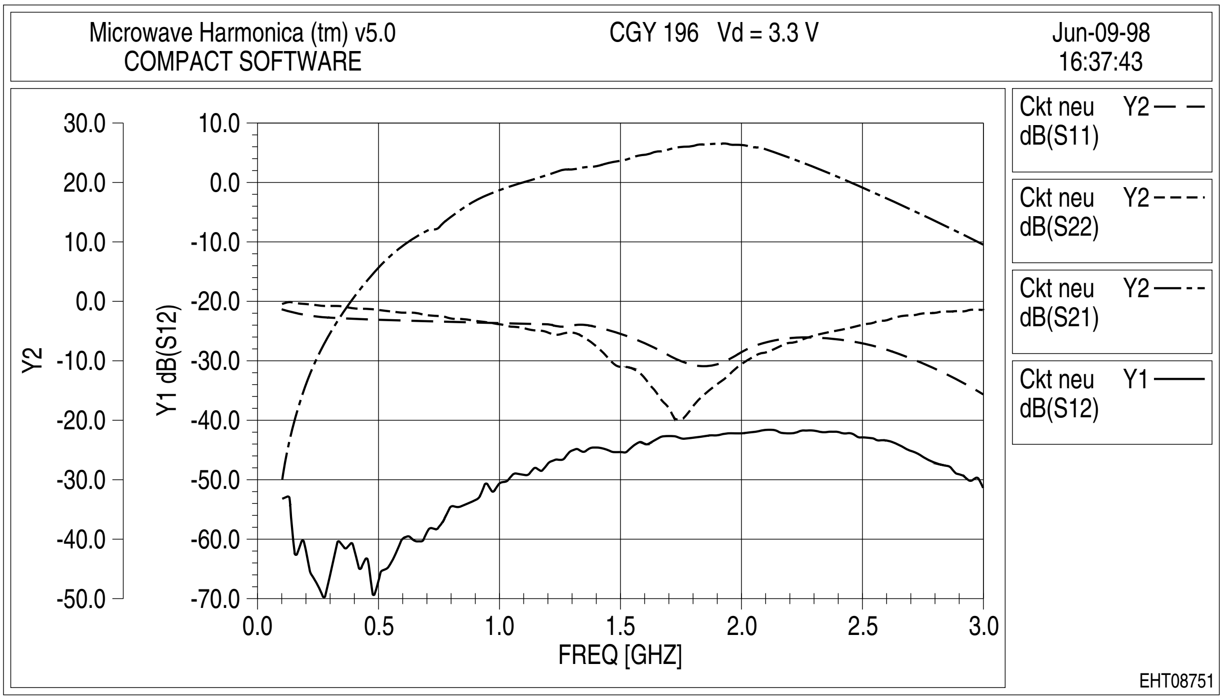
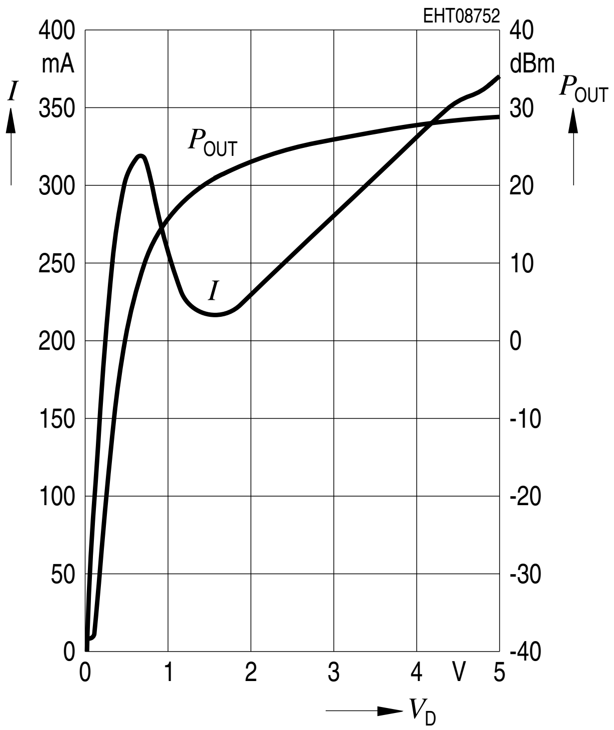
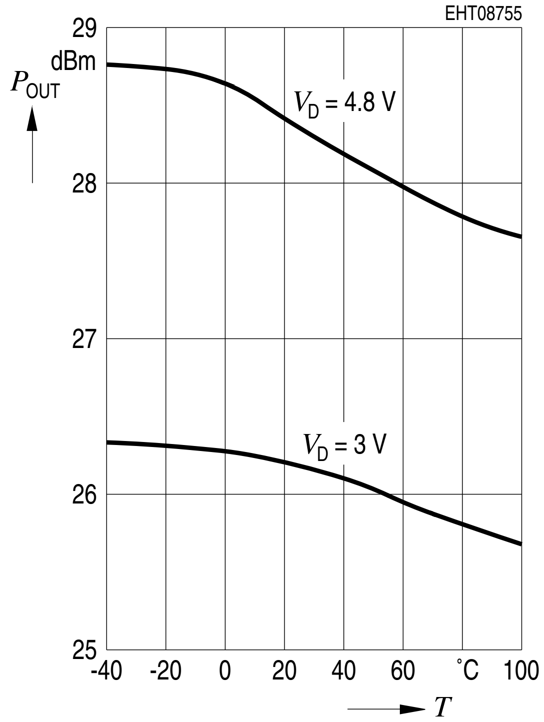


Figure 2 **S-Parameter**, pulsed mode: T = 417 µs, Duty Cycle 12.5%, P_{IN} = 0 dBm, V_D = 3.3 V

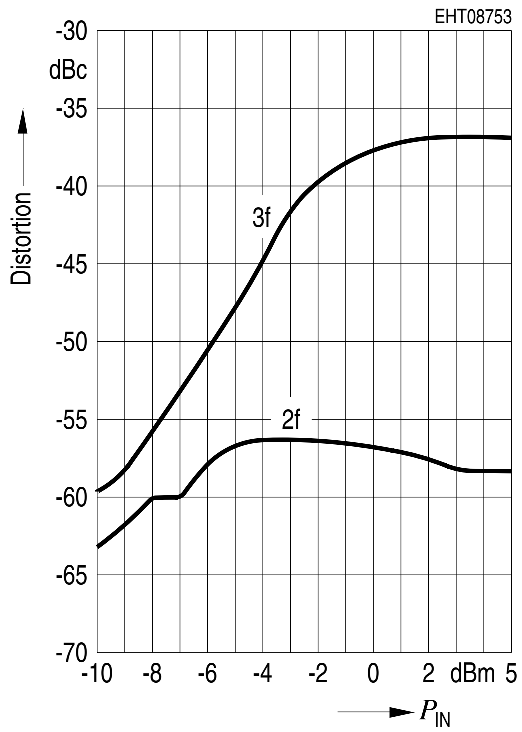
P_{OUT}, I_D = *f* (V_D), P_{IN} = 0 dBm
(pulsed mode: T = 417 µs,
duty cycle 12.5%)



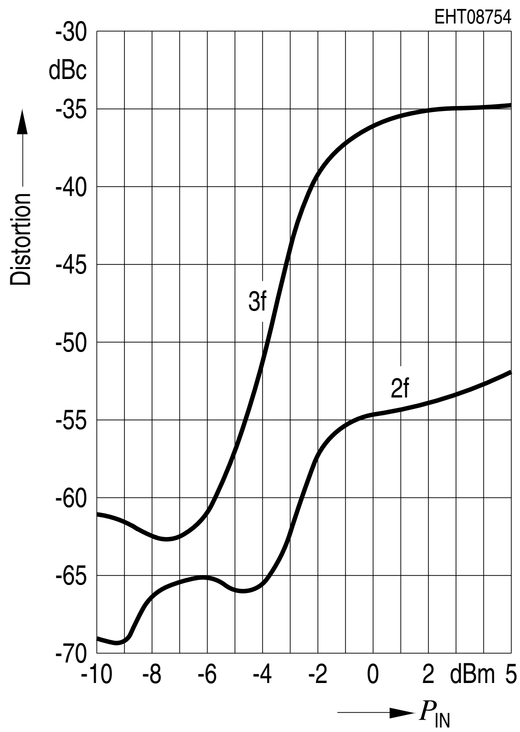
P_{OUT} vs. T, V_D = 3.0 V,
duty cycle = 10%, P_{IN} = 0 dBm



Harmonic Distortion, V_D = 3.3 V



Harmonic Distortion, V_D = 4.8 V



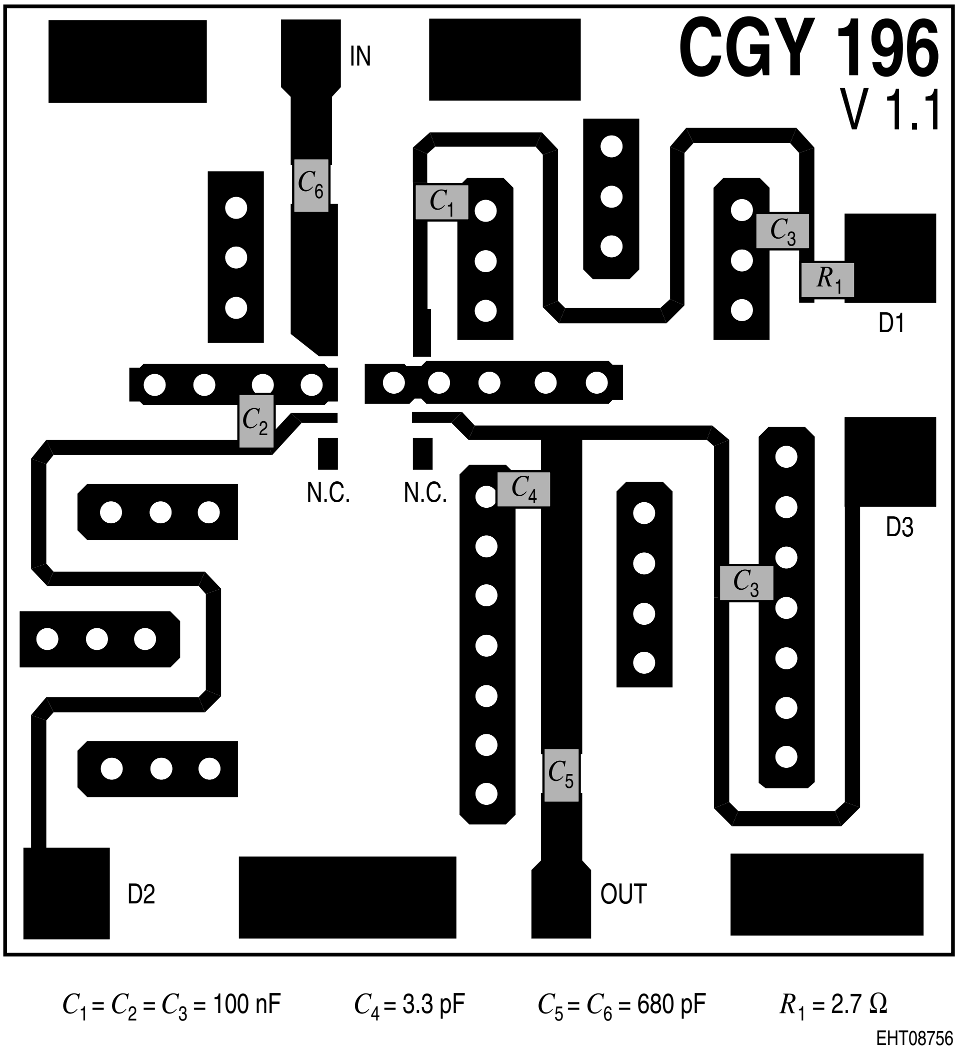


Figure 3 Test Board Layout (3.0 V DECT-Application, f = 1.89 GHz)

Electrical Characteristics 2.4 V DECT-Application f = 1.89 GHz

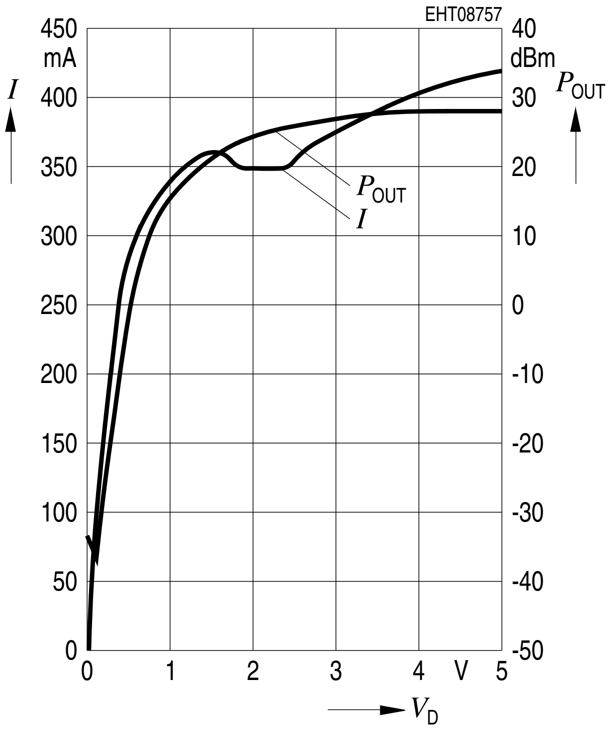
T_A = 25 °C, f = 1.89 GHz, Z_S = Z_L = 50 Ω, unless otherwise specified

Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_{DD}	–	340	–	mA	V_D = 2.4 V; P_{IN} = + 0 dBm
Supply current	I_{DD}	–	450	–	mA	V_D = 2.4 V; P_{IN} = – 10 dBm
Output Power	P_O	–	25.5	–	dBm	V_D = 2.4 V; P_{IN} = 0 dBm
Overall Power added Efficiency	PAE	–	44	–	%	V_D = 2.4 V; P_{IN} = + 0 dBm
Supply current	I_{DD}	–	320	–	mA	V_D = 2.2 V; P_{IN} = + 0 dBm
Supply current	I_{DD}	–	450	–	mA	V_D = 2.2 V; P_{IN} = – 10 dBm
Output Power	P_O	–	24.7	–	dBm	V_D = 2.2 V; P_{IN} = 0 dBm
Overall Power added Efficiency	PAE	–	42	–	%	V_D = 2.2 V; P_{IN} = + 0 dBm
Supply current	I_{DD}	–	380	–	mA	V_D = 3.0 V; P_{IN} = + 0 dBm
Supply current	I_{DD}	–	450	–	mA	V_D = 3.0 V; P_{IN} = – 10 dBm
Output Power	P_O	–	27.0	–	dBm	V_D = 3.0 V; P_{IN} = 0 dBm
Overall Power added Efficiency	PAE	–	44	–	%	V_D = 3.0 V; P_{IN} = + 0 dBm
Off Isolation	-S21	–	35	–	dB	V_D = 0 V; P_{IN} = 0 dBm
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 0 dBm, $V_D \leq$ 3.0 V, Z_S = 50 Ω Load VSWR = 20:1 for all phase

Electrical Characteristics 2.4 V DECT-Application f = 1.89 GHz (cont'd)
T_A = 25 °C, f = 1.89 GHz, Z_S = Z_L = 50 Ω, unless otherwise specified

Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 3 dBm, $V_D \leq$ 5.0 V, Z_S = 50 Ω Load VSWR = 20:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level.			–	P_{IN} = 0 dBm, V_D = 3.0 V, Z_S = 50 Ω Load VSWR = 10:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level.			–	P_{IN} = 3 dBm, V_D = 5.0 V, Z_S = 50 Ω Load VSWR = 10:1 for all phase

$\boldsymbol{P_{OUT}, I_D = f(V_D)}$, P_{IN} = 0 dBm
(pulsed mode: T = 417 µs, duty cycle 12.5%),
2.4 V Application



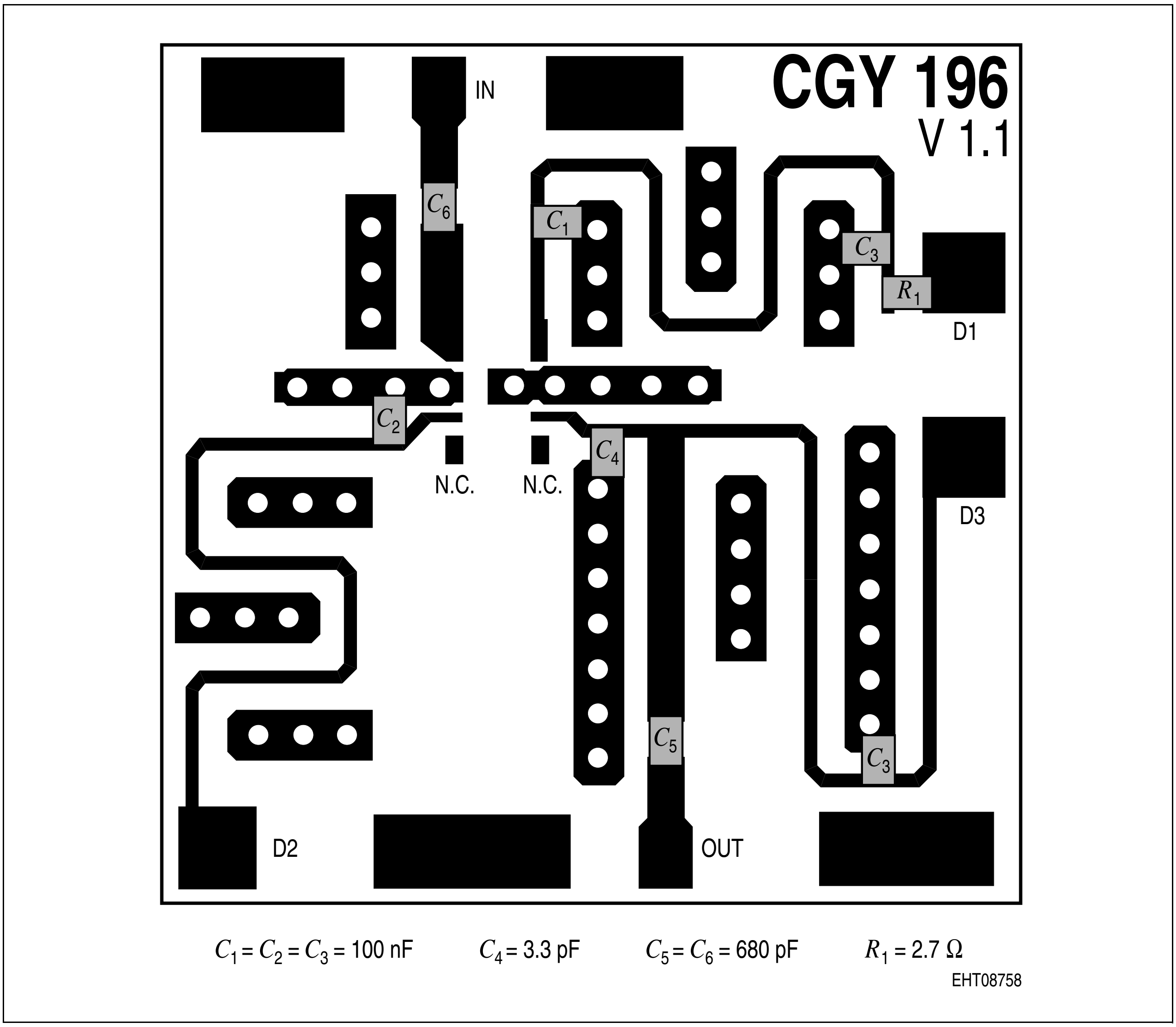


Figure 4 Test Board Layout (2.4 V DECT-Application, f = 1.89 GHz)

Electrical Characteristics (2.4 GHz ISM-Application)
T_A = 25 °C, f = 2.40 GHz, Z_S = Z_L = 50 Ω, unless otherwise specified

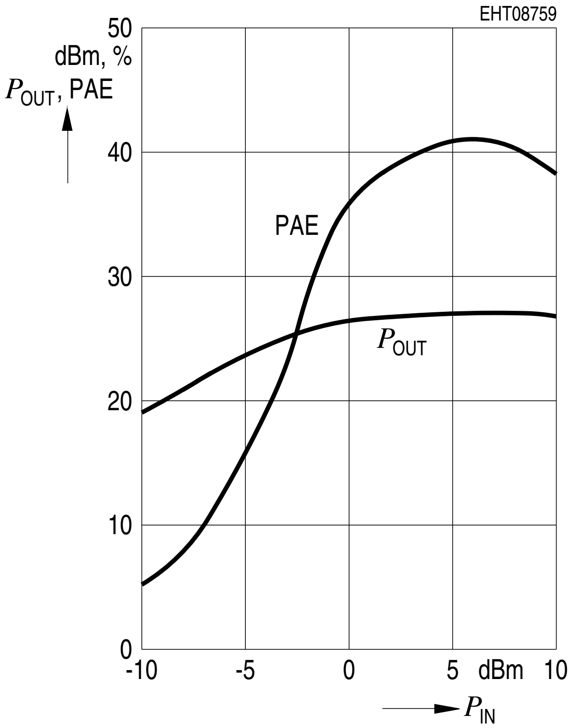
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_{DD}	–	300	–	mA	V_D = 3.3 V; P_{IN} = + 3 dBm
Supply current	I_{DD}	–	450	–	mA	V_D = 3.3 V; P_{IN} = – 10 dBm
Output Power	P_O	–	26.0	–	dBm	V_D = 3.3 V; P_{IN} = + 3 dBm
Overall Power added Efficiency	PAE	–	40	–	%	V_D = 3.3 V; P_{IN} = + 3 dBm
Off Isolation	-S21	–	34	–	dB	V_D = 0 V; P_{IN} = 3 dBm
Supply current	I_{DD}	–	300	–	mA	V_D = 4.8 V; P_{IN} = + 6 dBm
Supply current	I_{DD}	–	450	–	mA	V_D = 4.8 V; P_{IN} = – 10 dBm
Output Power	P_O	–	27.5	–	dBm	V_D = 4.8 V; P_{IN} = + 6 dBm
Overall Power added Efficiency	PAE	–	40	–	%	V_D = 4.8 V; P_{IN} = + 6 dBm
Off Isolation	-S21	–	34	–	dB	V_D = 0 V; P_{IN} = 3 dBm
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 3 dBm, $V_D \leq$ 3.6 V, Z_S = 50 Ω Load VSWR = 20:1 for all phase
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 6 dBm, $V_D \leq$ 5.0 V, Z_S = 50 Ω Load VSWR = 20:1 for all phase

Electrical Characteristics (2.4 GHz ISM-Application) (cont'd)
T_A = 25 °C, f = 2.40 GHz, Z_S = Z_L = 50 Ω, unless otherwise specified

Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Stability	–	All spurious output more than 70 dB below desired signal level			–	P_{IN} = 3 dBm, V_D = 3.6 V, Z_S = 50 Ω Load VSWR = 10:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level			–	P_{IN} = 6 dBm, V_D = 5.0 V, Z_S = 50 Ω Load VSWR = 10:1 for all phase

Electrical Characteristics (2.4 GHz ISM-Application)

P_{OUT}, PAE = f (P_{IN}), V_D = 3.3 V,
f = 2.4 GHz (pulsed mode: T = 417 µs,
duty cycle 12.5%



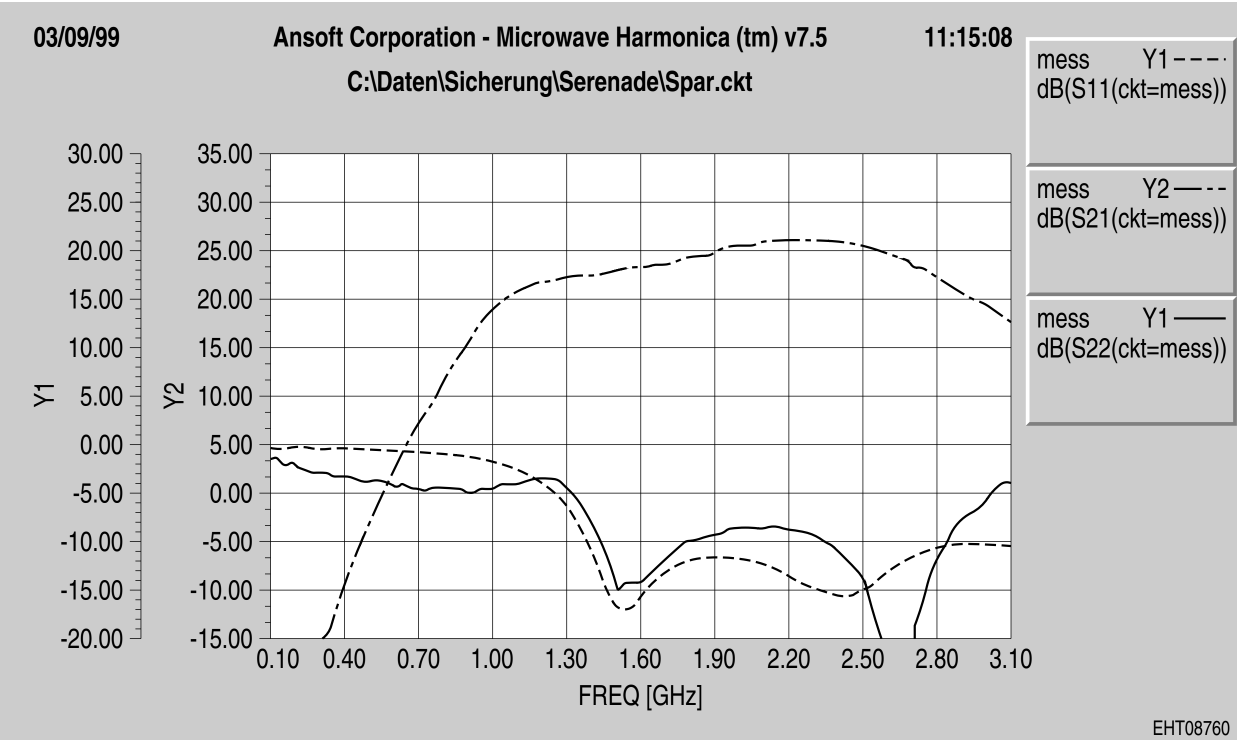
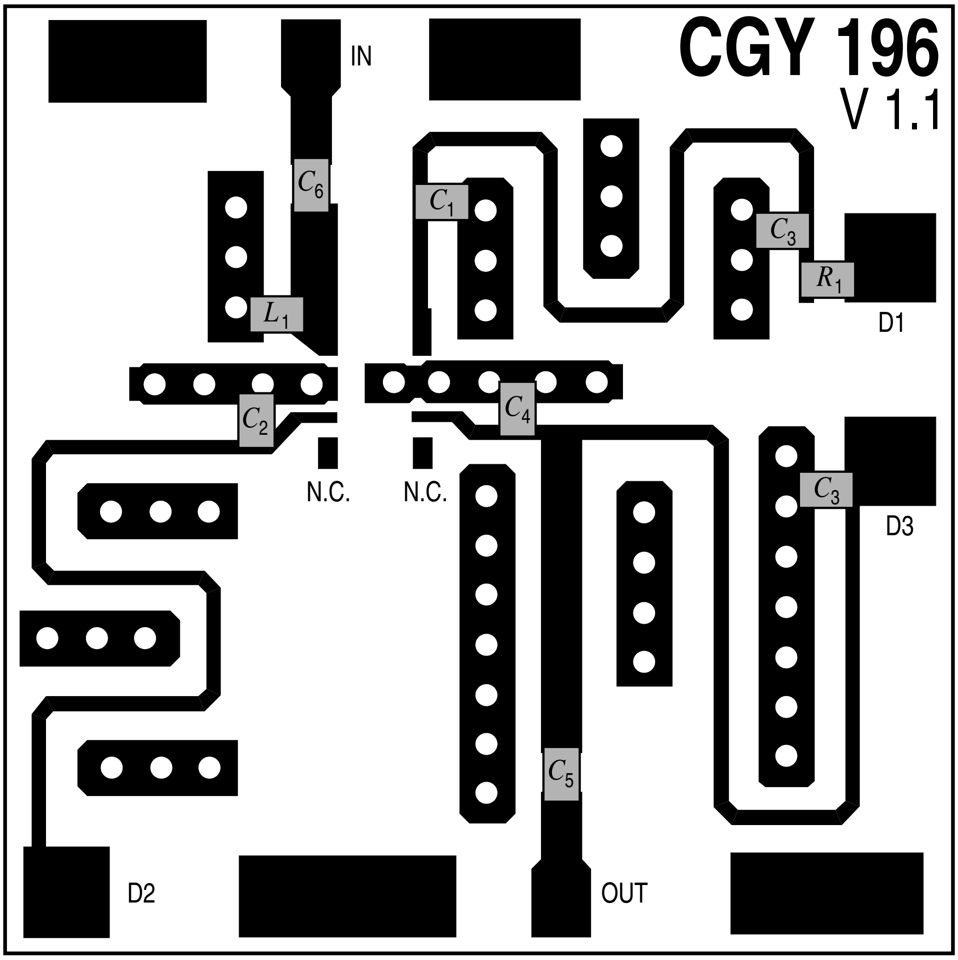


Figure 5 **S-Parameter**
V_D = 3.3 V, P_{IN} = 0 dBm (pulsed mode: T = 417 µs, duty cycle 12.5%)



$C_1 = C_2 = C_3 = 100$ nF $C_4 = 1.8$ pF $C_5 = C_6 = 1$ nF $R_1 = 2.7\ \Omega$ $L_1 = 3.9$ nH

Figure 6 Test Board Layout (2.4 GHz ISM - Application)

Electrical Characteristics (900 MHz ISM-Application)
T_A = 25 °C, f = 0.90 GHz, Z_S = Z_L = 50 Ω, unless otherwise specified

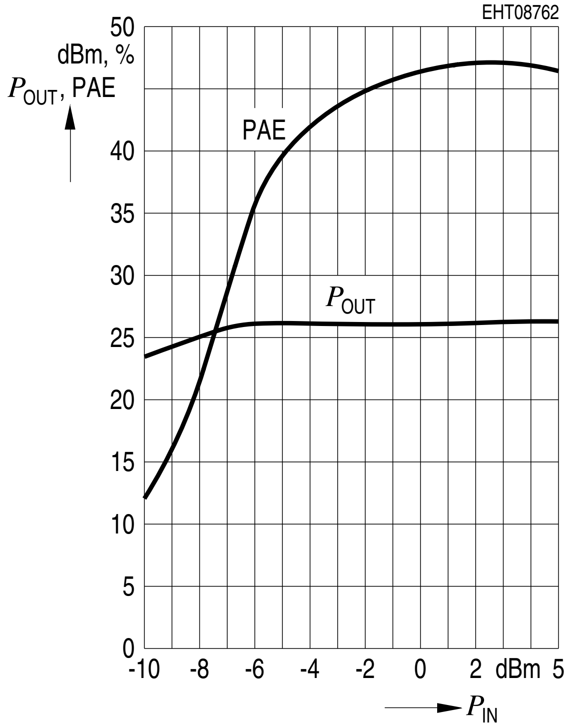
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_{DD}	–	300	–	mA	V_D = 3.3 V; P_{IN} = + 3 dBm
Supply current	I_{DD}	–	450	–	mA	V_D = 3.3 V; P_{IN} = – 10 dBm
Output Power	P_O	–	26.0	–	dBm	V_D = 3.3 V; P_{IN} = + 3 dBm
Overall Power added Efficiency	PAE	–	40	–	%	V_D = 3.3 V; P_{IN} = + 3 dBm
Off Isolation	-S21	–	34	–	dB	V_D = 0 V; P_{IN} = 3 dBm
Supply current	I_{DD}	–	300	–	mA	V_D = 4.8 V; P_{IN} = + 6 dBm
Supply current	I_{DD}	–	450	–	mA	V_D = 4.8 V; P_{IN} = – 10 dBm
Output Power	P_O	–	27.5	–	dBm	V_D = 4.8 V; P_{IN} = + 6 dBm
Overall Power added Efficiency	PAE	–	40	–	%	V_D = 4.8 V; P_{IN} = + 6 dBm
Off Isolation	-S21	–	34	–	dB	V_D = 0 V; P_{IN} = 3 dBm

Electrical Characteristics (900 MHz ISM-Application) (cont'd)
T_A = 25 °C, f = 0.90 GHz, Z_S = Z_L = 50 Ω, unless otherwise specified

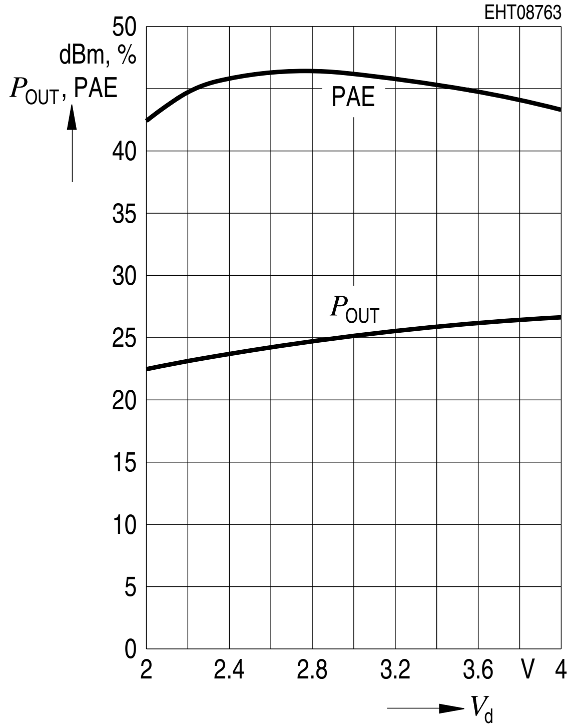
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 3 dBm, $V_D \leq$ 3.6 V, Z_S = 50 Ω Load VSWR = 20:1 for all phase
Load mismatch	–	No module damage for 10 s			–	P_{IN} = 6 dBm, $V_D \leq$ 5.0 V, Z_S = 50 Ω Load VSWR = 20:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level			–	P_{IN} = 3 dBm, V_D = 3.6 V, Z_S = 50 Ω Load VSWR = 10:1 for all phase
Stability	–	All spurious output more than 70 dB below desired signal level			–	P_{IN} = 6 dBm, V_D = 5.0 V, Z_S = 50 Ω Load VSWR = 10:1 for all phase

Electrical Characteristics
(900 MHz ISM-Application)

P_{OUT}, PAE = f (P_{IN}), V_D = 3.5 V,
f = 900 MHz [CW])



P_{OUT}, PAE = f (V_D), P_{IN} = 0 dBm,
f = 900 MHz [CW])



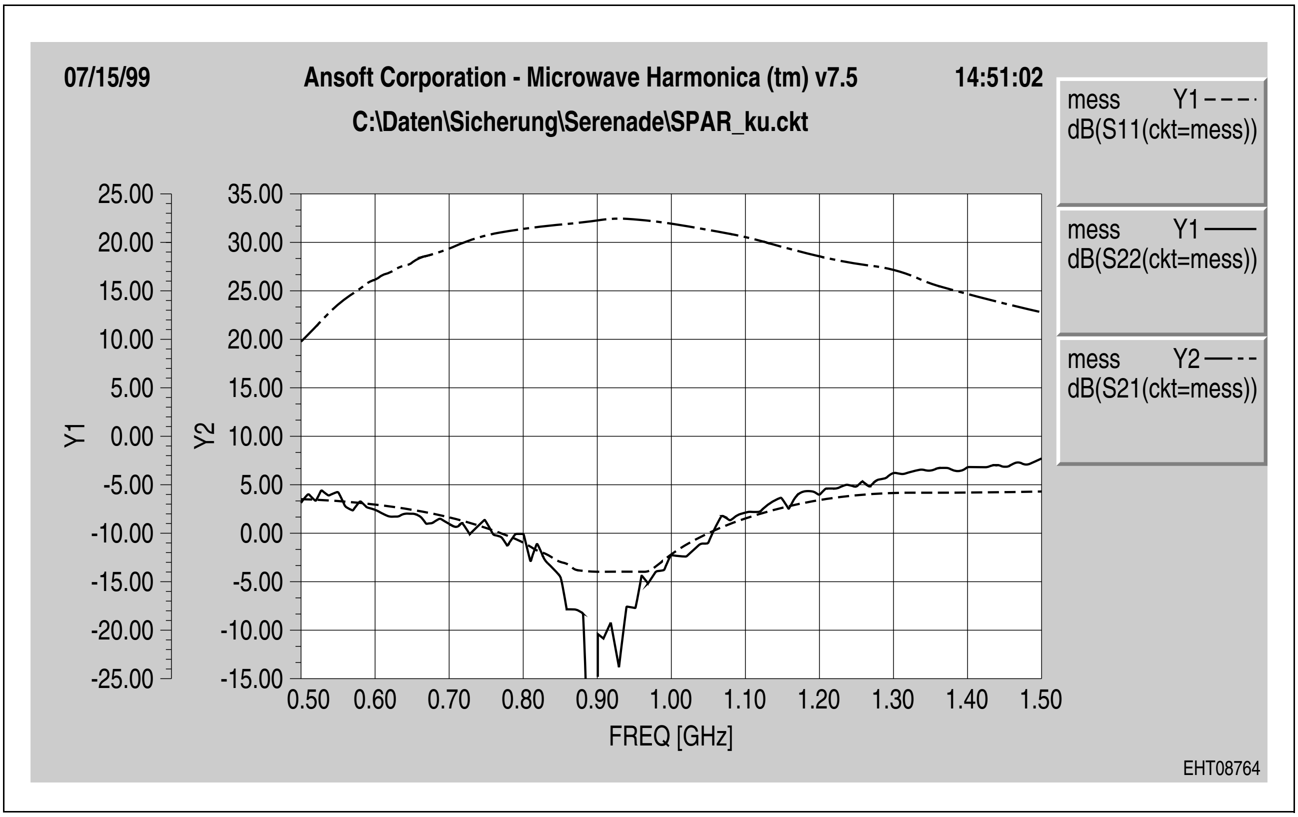


Figure 7 **S-Parameter**, V_D = 3.5 V, P_{IN} = – 5.5 dBm [cw mode]

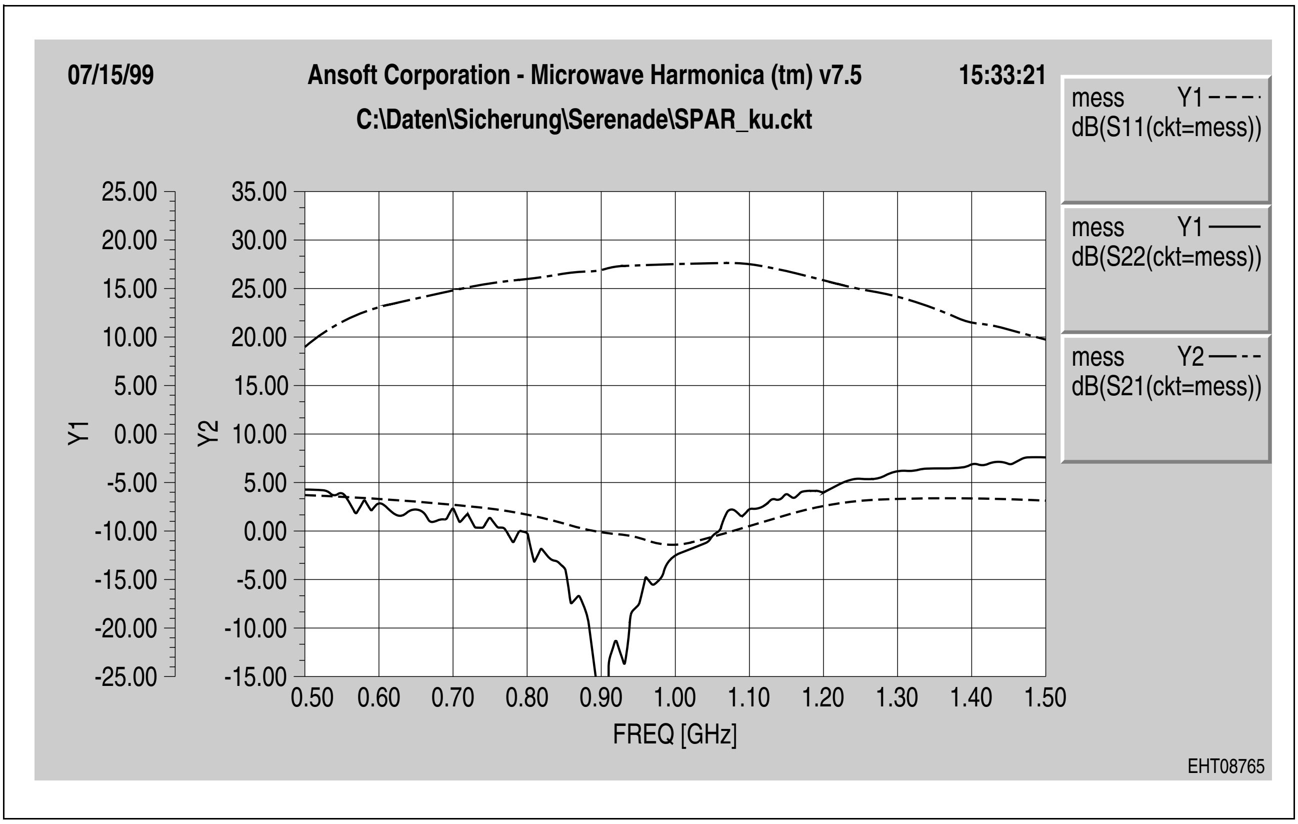


Figure 8 **S-Parameter**, V_D = 3.5 V, P_{IN} = – 0.5 dBm [cw mode]

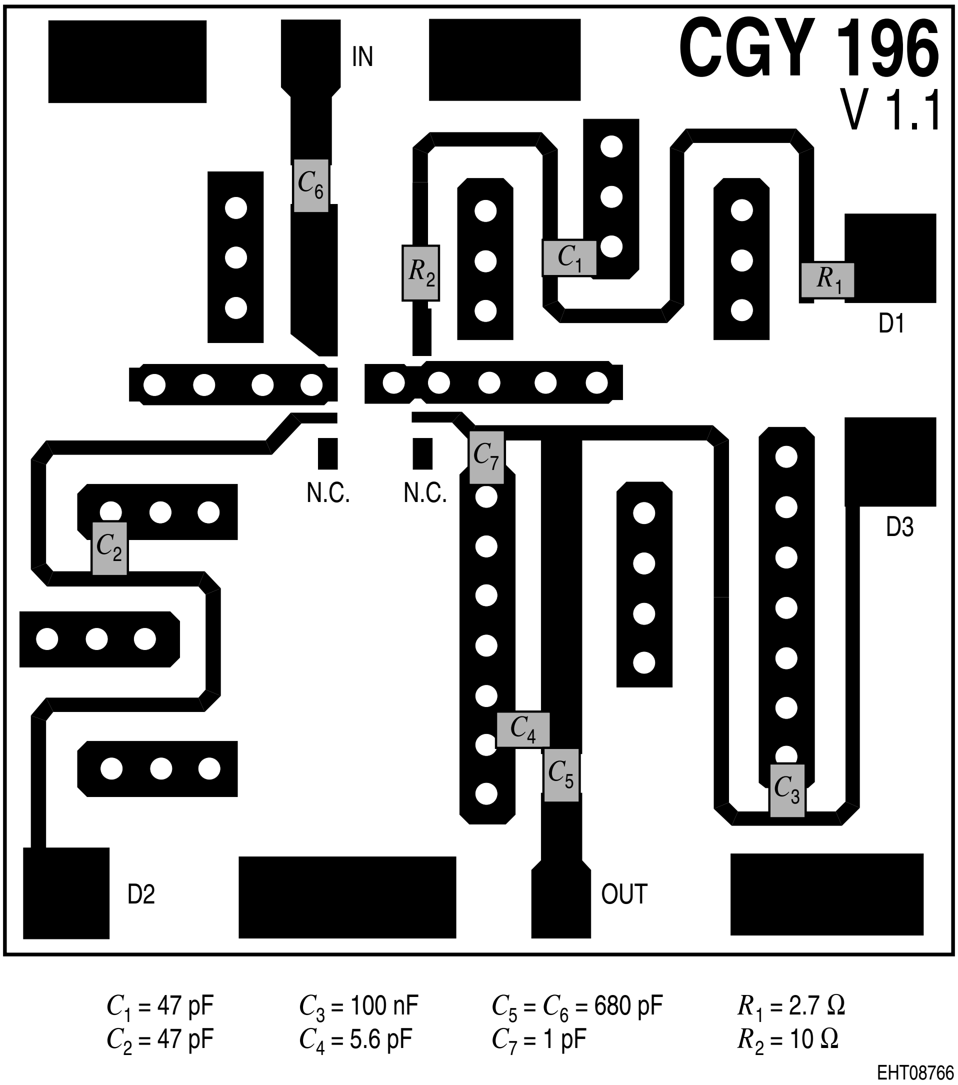
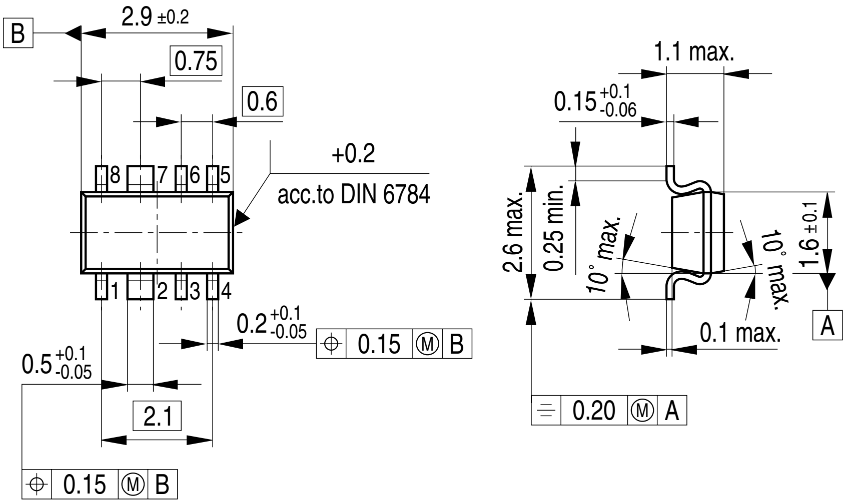


Figure 9 Test Board Layout (900 MHz ISM - Application)

Package Outlines

SCT-598
(Special Package)



GPW09182

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm