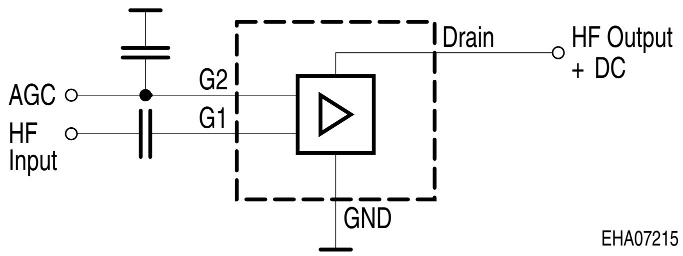
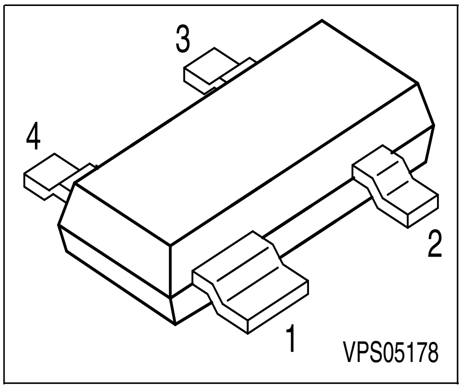
Silicon N-Channel MOSFET Tetrode

- For low noise, high gain controlled input stages up to 1GHz
- Operating voltage 9V
- Integrated bias network





ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precaution!

Type	Marking	Pin Configuration				Package
BF 1009S	JLs	1 = S	2 = D	3 = G2	4 = G1	SOT-143

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	12	V
Continuos drain current	I_D	25	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Gate 1 (external biasing)	$+V_{G1SE}$	3	V
Total power dissipation, $T_S \leq 76$ °C	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

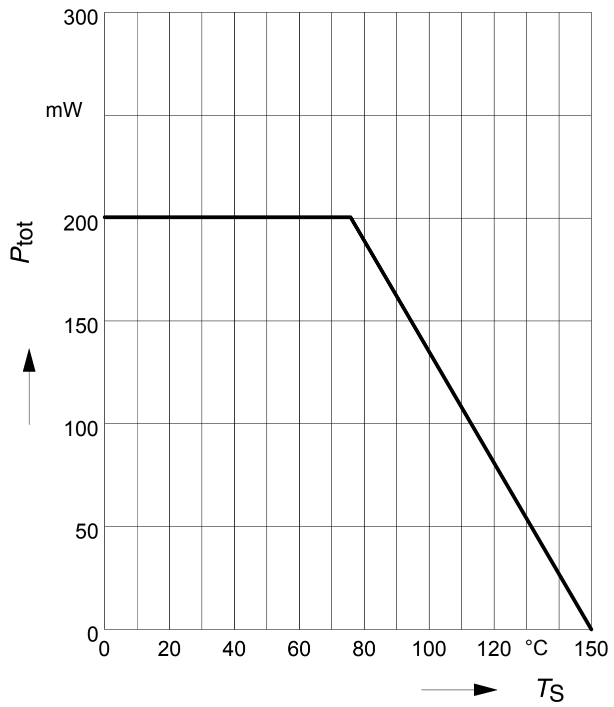
Channel - soldering point	R_{thchs}	≤370	K/W

Note:
It is not recommended to apply external DC-voltage on Gate 1 in active mode.

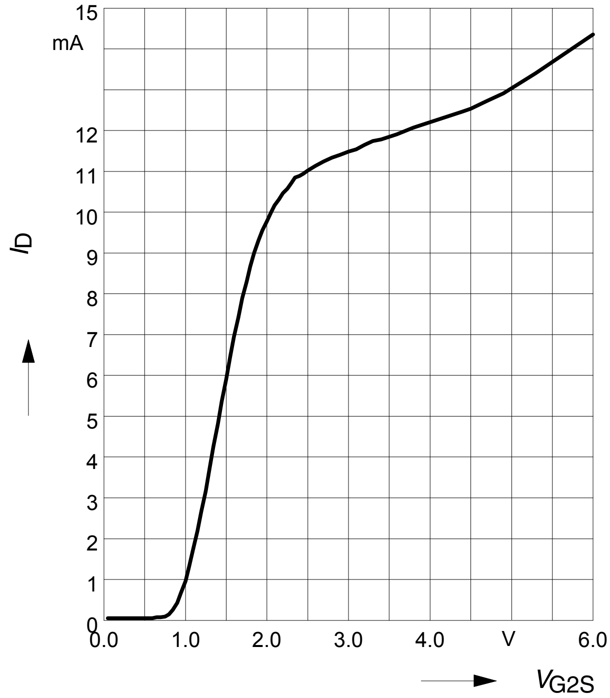
Electrical Characteristics at T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Drain-source breakdown voltage I_D = 300 µA, V_{G1S} = 0 V, V_{G2S} = 0 V	$V_{(BR)DS}$	16	-	-	V
Gate 1 - source breakdown voltage $+I_{G1S}$ = 10 mA, V_{G2S} = 0 V, V_{DS} = 0 V	$+V_{(BR)G1SS}$	8	-	12	
Gate 2 source breakdown voltage $\pm I_{G2S}$ = 10 mA, V_{G1S} = 0 V, V_{DS} = 0 V	$\pm V_{(BR)G2SS}$	10	-	16	
Gate 1 source current V_{G1S} = 6 V, V_{G2S} = 0 V	$+I_{G1SS}$	-	-	60	µA
Gate 2 source leakage current $\pm V_{G2S}$ = 8 V, V_{G1S} = 0 V, V_{DS} = 0 V	$\pm I_{G2SS}$	-	-	50	nA
Drain current V_{DS} = 9 V, V_{G1S} = 0 , V_{G2S} = 6 V	I_{DSS}	-	-	500	µA
Operating current (selfbiased) V_{DS} = 9 V, V_{G2S} = 6 V	I_{DSO}	10	14	19	mA
Gate 2-source pinch-off voltage V_{DS} = 9 V, I_D = 100 µA	$V_{G2S(p)}$	-	0.9	-	V
AC characteristics					
Forward transconductance (self biased) V_{DS} = 9 V, V_{G2S} = 6 V	g_{fs}	26	30	-	mS
Gate 1-input capacitance (self biased) V_{DS} = 9 V, V_{G2S} = 6 V, f = 1 MHz	C_{g1ss}	-	2.1	2.7	pF
Output capacitance (self biased) V_{DS} = 9 V, V_{G2S} = 6 V, f = 1 MHz	C_{dss}	-	0.9	-	
Power gain (self biased) V_{DS} = 9 V, V_{G2S} = 6 V, f = 800 MHz	G_{ps}	18	22	-	dB
Noise figure (self biased) V_{DS} = 9 V, V_{G2S} = 6 V, f = 800 MHz	F_{800}	-	1.4	-	
Gain control range (self biased) V_{DS} = 9 V, VG2S = 6 ... 0V, f = 800 MHz	ΔG_{ps}	40	50	-	

Total power dissipation $P_{tot} = f\,(T_S)$

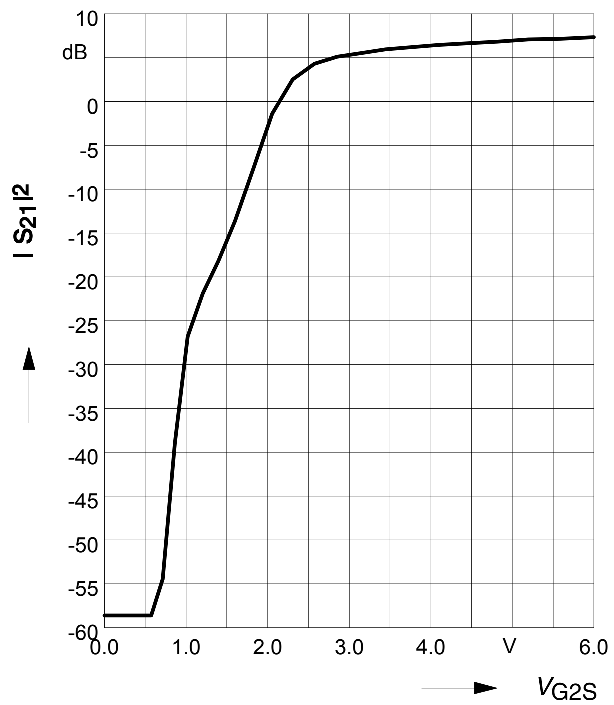


Drain current $I_D = f\,(V_{G2S})$



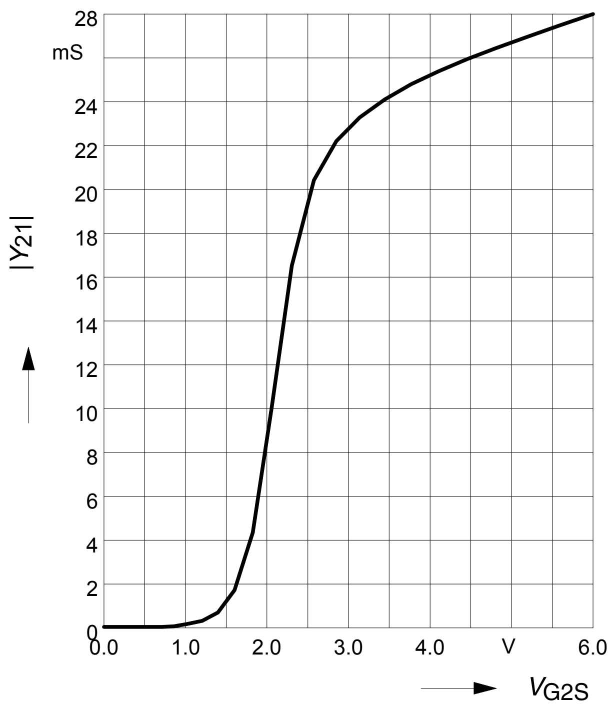
Insertion power gain

$|\,S_{21}\,|^2 = f\,(V_{G2S})$



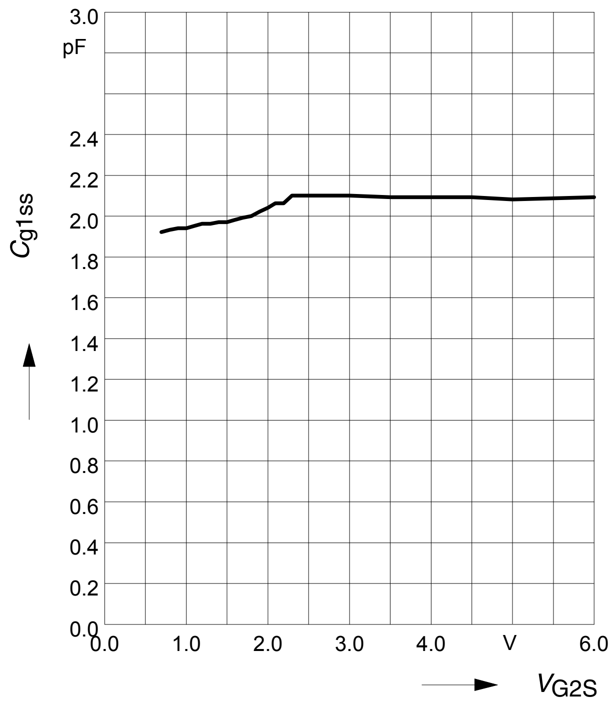
Forward transfer admittance

$|\,Y_{21}\,| = f\,(V_{G2S})$



Gate 1 input capacitance $C_{g1ss} = f(V_{g2s})$

f = 200MHz



Output capacitance $C_{dss} = f(V_{G2S})$

f = 200MHz