82560
HOST INTERFACE AND MEMORY CONTROLLER

- **Host Interface to the IBM PC/XT/AT and PS/2™ Buses for 82590, 82592, and 82588 LAN Controllers**
- **Allows 32-, 16-, and 8-Bit Data Transfers**
- **Supports Local Static RAM**
  - **—Up to 32 Kilobytes**
  - **—Programmable Access Time**
- **Zero-Wait-State Host Interface Option**
- **Dual-Channel DMA Controller with Ring Buffer Management Scheme**
- **Implements Tightly Coupled Interface Mode to 82590/82592**
  - **—Automatic Retransmission upon Collision**
  - **—Transmit Chaining**
  - **—Back-to-Back Frame Reception**
  - **—Automatic Buffer Reclamation**
  - **—Address PROM or Other Peripheral Support**
  - **—Interfaces Memory-Mapped or I/O-Mapped Adapters**
- **CHMOS III Technology**
- **68-Lead PLCC Package**

The 82560 Host Interface and Memory Controller is a companion chip for the Intel 82590 and 82592 Advanced CSMA/CD LAN Controllers as well as the Intel 82588. The 82560 interfaces these controllers to IBM PC/XT/AT and PS/2 systems. It integrates all the interface functions required to implement a nonintelligent, locally buffered LAN solution. The zero wait state and 32-bit data transfers improve the system performance by minimizing the LAN's requirement for Host bandwidth. The 82560's DMA performs data transfers between the LAN controller and the ring-configured local memory. Ring buffer implementation results in highly efficient use of the local memory. The 82560 supports the 82590 and 82592 in their Tightly Coupled Interface (TCI) mode. Without CPU intervention, the 82560 performs transmit chaining, automatic retransmission, back-to-back frame reception, and frame reclamation. The TCI support reduces the software and hardware overhead between frame transfers, and increases the average sustained transfer rate. Combined with the 82590 or 82592, the 82560 provides a high-performance LAN solution for industry standard or custom CSMA/CD networks.

November 1988
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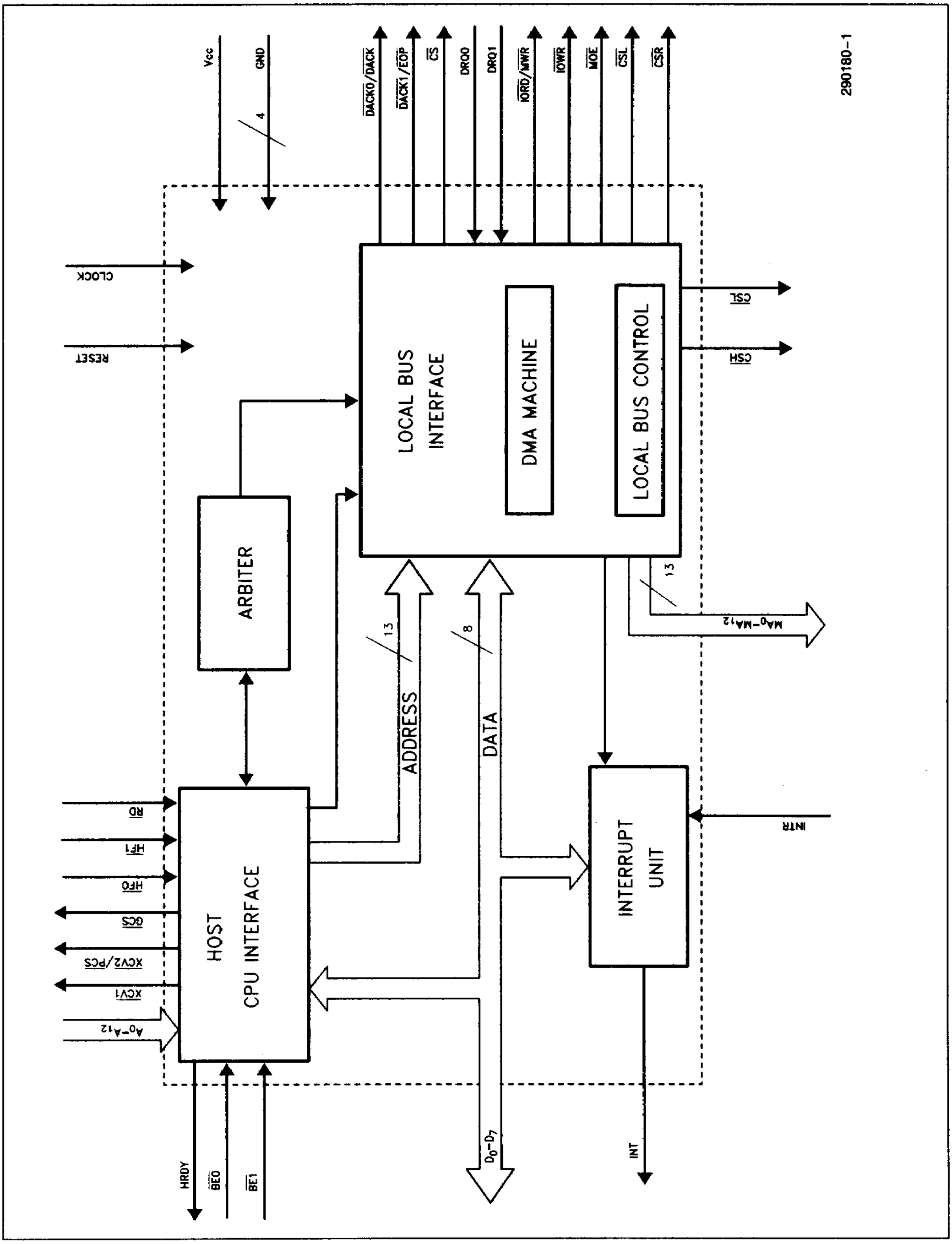


Figure 1. 82560 Block Diagram

Table 1. 82560 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	5, 23, 57	I	**POWER:** Connected to +5V power supply.
V_{SS}	10, 29, 43, 63	I	**GROUND:** Ground connection.
CLK	11	I	**CLOCK INPUT:** This is the system clock input for the 82560. It controls the internal operations of the 82560 and its cycle timing.
RESET	42	I	**RESET:** Active high. When active it resets the 82560 to a known passive state.
D_0–D_7	40, 41, 44–49	I/O	**82560 DATA BUS:** Tri-state bus. Used for programmatic access to the 82560 registers. They are also used in the tightly coupled interface (TCI) mode.
A_0–A_{12}	26–39	I	**ADDRESS LINES:** The 13 address lines select either an 82560 register, or an address in the Local Memory.
$\overline{HF0}$, $\overline{HF1}$	25, 24	I	**HOST FUNCTION SELECT:** These two inputs indicate the type of access requested by the host. These signals are generated by external decode logic and are completely asynchronous to the 82560 system clock. The proper combinations for each access type are shown below: **HOST FUNCTION** **$\overline{HF1}$ — $\overline{HF0}$ — Access Type** 1 — 1 — Idle (No Access Being Requested) 1 — 0 — Request to Access Shared Portion of Local Memory 0 — 1 — Request to Access 82560 Registers or the Slave Controller (SCS) 0 — 0 — Request to Access External PROMs or Latches ($\overline{GCS}$)
$\overline{RD}$	17	I	**READ:** Active low. This signal is used to indicate the direction of the host transfer. When active, data is being read from the destination (RAM, 560, or GCS port).
HRDY	20	O	**HOST READY:** Active high. This signal from the 82560 is activated when the device on the Local Bus of the LAN adapter is ready to accept data (write cycle) or to output data (read cycle). When no access is being requested by the host (i.e., both $\overline{HF0}$ and $\overline{HF1}$ are high), this signal is tri-stated in the normal mode, and is driven high in the pipeline mode.
$\overline{XCV1}$	22	O	**TRANSCEIVER ENABLE 1:** Enables the transceiver that connects the lower byte of the host and Local data buses. In pipeline mode it enables the transceiver during non-memory host cycles.
$\overline{XCV2}/\overline{PCS}$	21	O	**TRANSCEIVER ENABLE 2:** Enables the transceiver that connects the upper byte of the host and Local data buses. In pipeline mode it enables the latch during memory host cycles.
INT	50	O	**INTERRUPT OUT:** This signal is a logical OR of all enabled interrupt requests. When active it indicates an interrupt request to the CPU. This signal is tristated after reset.
$\overline{GCS}$	59	O	**GENERAL CHIP SELECT:** Active low. This signal is asserted by the 82560 when the host requests access to external ROMs or latches.

Table 1. 82560 Pin Description (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{\text{BE0}}$</td><td>18</td><td>I</td><td><b>BYTE ENABLE:</b> Active low. This signal is asserted in 16- or 32-bit-wide host memory cycles to select the lower memory bank. It may be connected to the processor's A_0 pin.</td></tr>
<tr><td>$\overline{\text{BE1}}$</td><td>19</td><td>I</td><td><b>BYTE ENABLE 1:</b> Active low. This signal is asserted in 16- or 32-bit-wide host memory cycles to select the upper memory bank. It may be connected to the processor's BHE signal. These two signals are connected as follows:
<table>
<tr><th>Host Bus</th><th>Local Bus</th><th>$\overline{\text{BE0}}$</th><th>$\overline{\text{BE1}}$</th></tr>
<tr><td>8-Bit</td><td>8-Bit</td><td>0</td><td>0</td></tr>
<tr><td>8-Bit</td><td>16-Bit</td><td>SA0</td><td>1</td></tr>
<tr><td>16-Bit</td><td>16-Bit</td><td>SA0</td><td>$\overline{\text{SHBE}}$</td></tr>
<tr><td>16-Bit</td><td>32-Bit</td><td>SA1</td><td>SA1</td></tr>
<tr><td>32-Bit*</td><td>32-Bit</td><td>$\overline{\text{BE0}}$ + $\overline{\text{BE1}}$</td><td>$\overline{\text{BE2}}$ + $\overline{\text{BE3}}$</td></tr>
</table>
*80386 address pins
+ stands for logical OR</td></tr>
<tr><td>DRQ0</td><td>54</td><td>I</td><td><b>DMA REQUEST CHANNEL 0:</b> Active high. This is an input from the LAN controller or other peripherals, it requests DMA service. The DMA cycles are run on an on-demand basis, and are prioritized between themselves (two channels) and with the host cycles on an alternating basis. In 82590 Tightly Coupled mode this signal is sampled by the 82560 at the last clock of the Read or Write signal along with $\overline{\text{DACK1}}$/$\overline{\text{EOP}}$ to determine the state of the transmit or receive process (see Tightly Coupled Interface for more details).</td></tr>
<tr><td>DRQ1</td><td>52</td><td>I</td><td><b>DMA REQUEST CHANNEL 1:</b> Active high. This is an input from the LAN controller or other peripherals, requesting DMA service. The DMA cycles are run on an on-demand basis, and are prioritized between themselves (two channels) and with the host cycles on an alternating basis. In Tightly Coupled mode this signal is sampled by the 82560 at the last clock of the Read or Write signal (see Tightly Coupled Interface for more details).</td></tr>
<tr><td>$\overline{\text{DACK0}}$/$\overline{\text{DACK}}$</td><td>55</td><td>O</td><td><b>Dual Function:</b> This is a dual function pin which serves as $\overline{\text{DACK0}}$, DMA acknowledge for Channel 0, in all modes except the Tightly Coupled Interface mode. It serves as $\overline{\text{DACK}}$, DMA acknowledge for both channels, in Tightly Coupled Interface mode.
<b>DMA ACKNOWLEDGE0:</b> Active low. Acknowledge DMA requests on channel 0. During special chip select cycles, this signal is controlled by the CPU.
<b>DMA ACKNOWLEDGE:</b> Active low. Acknowledge DMA requests on either channel 0, or channel 1. It operates in this mode only when programmed for Tightly Coupled Interface with the 82590 or 82592. This pin can be directly connected to the $\overline{\text{DACK0}}$/$\overline{\text{DACK}}$ pin of the 82590 or 82592 LAN controllers.</td></tr>
<tr><td>$\overline{\text{DACK1}}$/$\overline{\text{EOP}}$</td><td>53</td><td>I/O</td><td><b>Dual Function:</b> This is a dual function, bidirectional pin which serves as DACK1, DMA acknowledge for channel 1, in all modes except 8259X Tightly Coupled Interface mode. It serves as $\overline{\text{EOP}}$, End of Process indicator, an input, during this Tightly Coupled Interface mode.
<b>DMA ACKNOWLEDGE1:</b> Output. Active low. DMA acknowledge for channel 1. During Special Chip Select (SCS) cycles this signal is controlled by the CPU and can be used for accessing the 8259X port 1. The output level is determined by the address of the SCS.</td></tr>
</table>

Table 1. 82560 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{DACK1}$/$\overline{EOP}$	53	I/O	**END OF PROCESS:** Input. In the Tightly Coupled Interface mode, this input, along with the DRQ pin, is sampled by the 82560 at the last clock of the Read or Write signal. The combination of the two pins indicates the status of the Transmit or Receive process. When low, the EOP signal indicates that the active DMA service should be terminated.
$\overline{IOWR}$	56	O	**I/O WRITE.** Active low. This is the write strobe to the LAN controller or I/O device. It is asserted when data is being written to the LAN controller by either the Host CPU or the 82560 internal DMA. During pipeline read transfers it is the write control signal to the buffer.
$\overline{IORD}$/$\overline{MWR}$	58	O	**Dual Function:** Active low. This signal is used for two different operations. It is a control signal during read cycles from the LAN controller or another I/O device. It is a write strobe during write cycles to the local memory. **I/O READ:** Active low. It is asserted when data is being read from the LAN controller by either the host CPU or the 82560 internal DMA. During pipeline write transfers it is the read control signal to the buffer. **MEMORY WRITE:** Active low. It is asserted when data is being written to local memory.
INTR	51	I	**INTERRUPT REQUEST:** This signal when active indicates an interrupt request. It is usually connected to the interrupt output of the LAN controller. It may be programmed as active high or low, level or edge triggered, and it can also be masked.
MA0–12	9–1, 68	O	**MEMORY ADDRESS 0–12:** These 13 address lines can support two 8-kilobyte or 8-kiloword banks of static memory.
$\overline{CSL}$	62	O	**RAM CHIP SELECT (LOW BANK):** Active low. This signal is activated during all static-RAM accesses in 8-bit mode, even-byte accesses in 16-bit mode, and even-word accesses in 32-bit mode.
$\overline{CSH}$	61	O	**RAM CHIP SELECT (HIGH BANK):** Active low. This signal is activated during odd-byte accesses in 16-bit mode or odd-word accesses in 32-bit mode.
$\overline{MOE}$	60	O	**MEMORY OUTPUT ENABLE:** Active low. This signal is used to enable the memory array's output buffers during memory read cycles.
GPI	16	I	**GENERAL PURPOSE:** Input. This is a general purpose input pin, its state may be read by the CPU.
$\overline{CS}$	12	O	**CHIP SELECT:** Active low. This pin is normally connected to the Chip Select input of the LAN controller or other peripherals. It is activated during non-DMA accesses to the LAN controller. The CPU activates this signal when it accesses addresses 0, 1, 2, or 3 in the Special Chip Select address space of the 82560.
RSV1, RSV2	13, 14	I	These pins are reserved and should be tied to V_{CC}.

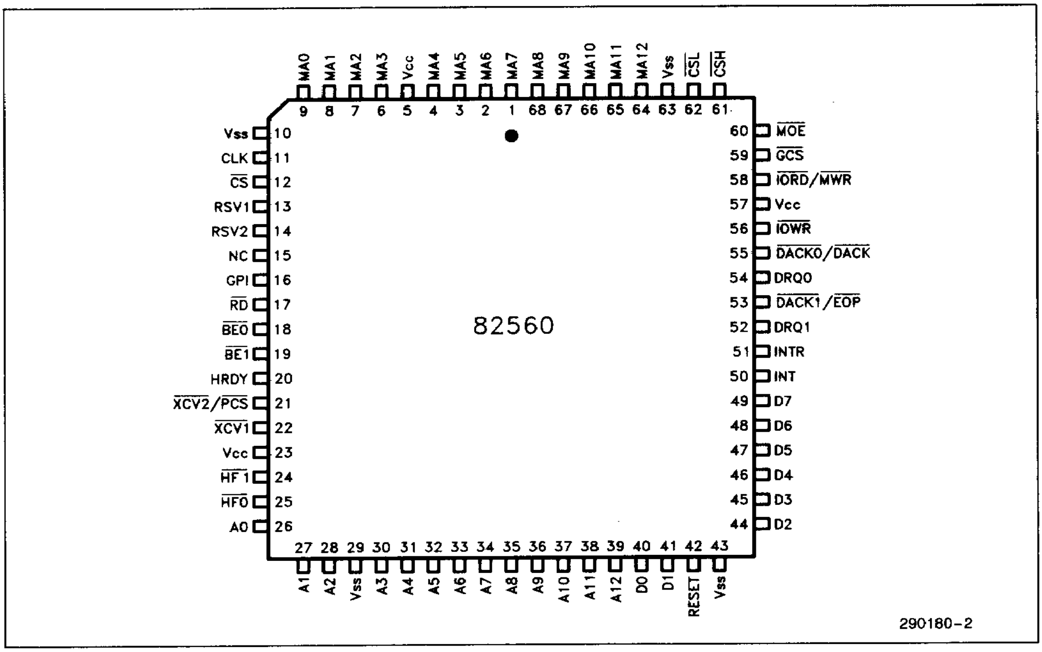


Figure 2. 82560 PLCC Pinout

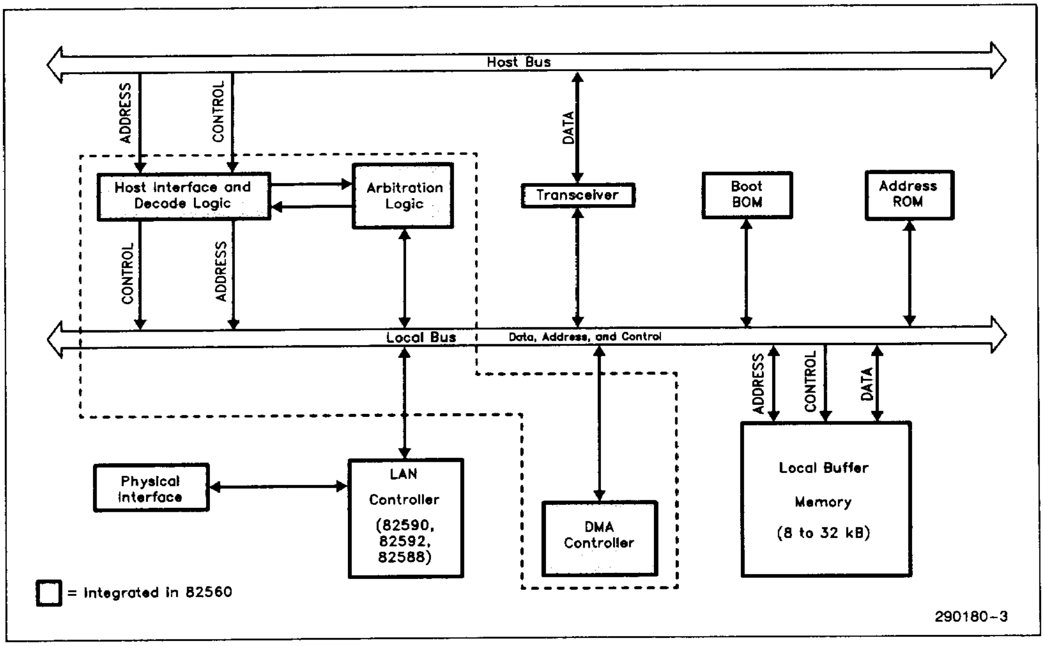


Figure 3. Nonintelligent, Buffered Adapter Architecture

FUNCTIONAL OVERVIEW

The 82560 is a dual-port memory controller using interrupt logic and DMA to implement a nonintelligent, buffered LAN adapter for the IBM PC/XT/AT bus. This type of adapter uses on-board memory as a buffer to store frames during transmission and reception. It also uses on-board DMA to transfer data between its local memory and the LAN controller. A block diagram of the buffered, nonintelligent LAN adapter is shown in Figure 3. The architecture is termed nonintelligent because it does not use an onboard CPU to process the transmit or receive frames. The host CPU processes the frames and programs the DMA and LAN controllers. The host interface logic, arbitration logic, and the bus transceivers connect the host bus to the adapter's local bus. They also control all host accesses to the local bus. The local memory is shared by the host and the LAN controller. It stores information that the host wishes to transfer to the LAN controller, and information received by the LAN controller which should be read by the host. The memory can be shared in two ways—mapping into the host memory space, or mapping into the host I/O space. The DMA controller transfers data between the local buffer memory and the LAN controller. The host CPU may use either string move instructions or a system DMA channel to move data into the buffer memory. The host also accesses the LAN controller registers, the DMA controller registers the boot ROM, and the address ROM through the local bus.

The 82560 integrates the host interface, arbitration logic, memory control logic, interrupt logic, and DMA into one component. It replaces 20–30 MSI and SSI components (see Figure 1). It also provides a Tightly Coupled Interface to the 82588, 82590, and 82592 LAN controllers, and an efficient buffer management scheme, which allows the 82588/82560, 82590/82560, and 82592/82560 combinations to handle time-critical processes such as retransmission, buffer reclamation, and continuous back-to-back frame reception without host CPU intervention. This improves the overall data throughput in the network; and, consequently, system performance. The following discussion describes the 82560 interface to the PC/XT/AT bus, its support of locally buffered memory, and the operation of DMA and the Tightly Coupled Interface (including the buffer management scheme).

HOST INTERFACE

The host interface port connects the 82560 to the PC-bus through external decode logic and bus transceivers. The external decode logic generates the HF0 and HF1 signals indicating the kind of access the host desires. When the request is detected by the 82560 (non-pipeline mode) it deasserts the HRDY signal, thereby suspending the host cycle. HRDY is reactivated when the local device being accessed by the host is ready to accept (Write cycle) or output (Read cycle) data. HRDY reactivation time is programmable as mentioned in the register section; it is described in detail in the *82560 Reference Manual.* The request undergoes arbitration, and, if granted, the 82560 activates the XCV1 and XCV2 signals. The XCV signals control the transceiver(s) which interfaces the host data bus to the local data bus. By using one or both transceiver control signals the 82560 can support an 8-, 16-, or 32-bit-wide bus. Once the arbiter grants the host access, the 82560 begins the local bus cycle by generating the appropriate address and control signals.

The host CPU can access the internal registers of the 82560, the local memory controlled by the 82560, or other devices—such as Boot ROM or external Latch—that share the same bus as the 82560. Table 2 lists the various access types that can be requested by the host.

Table 2. Host Access Types

Access Type	$\overline{\text{HF1}}$	$\overline{\text{HF0}}$	Address	Cycle Status Indications
82560 Registers	0	1	Between 8h and 3Fh	HRDY
Local Memory Access	1	0	User Defined	HRDY, Memory Control Signals, $\overline{\text{XCV}}$ Signals
GCS Access (Boot ROM) (General Chip Select)	0	0	User Defined	HRDY, $\overline{\text{GCS}}$, $\overline{\text{IOWR}}$, $\overline{\text{IORD/MWR}}$
Special Chip Select	0	1	Less Than 8h	HRDY, $\overline{\text{DACK}}$ Lines, $\overline{\text{CS}}$, $\overline{\text{IOWR}}$, $\overline{\text{IORD/MWR}}$

The 82560 provides eight semaphore ports to resolve contention in a shared resource system. Only the most significant bit of these ports is used. The CPU writes all 0's to the port to clear it. When the port is read, its current value is reported and the most significant bit becomes a 1 at the end of the cycle. The 82560 also supports devices on the local bus other than memory and the LAN controller. These devices can be accessed in two ways: by using the General Chip Select (GCS) signal, or by using the Special Chip Select (SCS) addresses in the 82560 register space. The first method typically supports EPROMs, external latches, and similar devices. The second method is used for accessing the registers of controllers which use the 82560 DMA channels; e.g., the 82590, 82592, or 82588. Each address in the SCS port provides a unique combination of the DACK0-, DACK1-, and CS-pin output states. The CPU activates the chip select of the device being accessed by asserting or deasserting the appropriate signals.

The host CPU can access the 82560 registers and other devices on the local bus at any time. However, local memory can only be accessed by the host after the 82560 memory control registers are initialized. The host accesses local memory in two ways: Page Access or Sequential (I/O mapped or pipeline) Access. After reset, the memory access is I/O-mapped mode but host access to local memory is disabled. The 82560 must be configured for the appropriate memory access mode before local memory can be accessed by the host.

The 82560 memory control logic provides the signals required to interface to static memory. The 82560 can address up to 32 kB of local memory. Each memory address can refer to a byte, a word, or a double word of local memory. Thus the 82560 with its two memory chip selects (low to high bank) and its MOE and MWR outputs, can support 8-, 16-, or 32-bit-wide local buses.

In Page Access mode the local memory is mapped into the host memory space. In this mode the host can directly access local memory through a fixed size window which can be moved around in local memory space. This window is referred to as a "page". Figure 5 shows the paging scheme. The page size can vary from 1 kilobyte to 8 kilowords, and can be located anywhere in local memory. The exact location of the page in the local memory is defined by a page register. By reprogramming the page register the user can relocate the page in local memory.

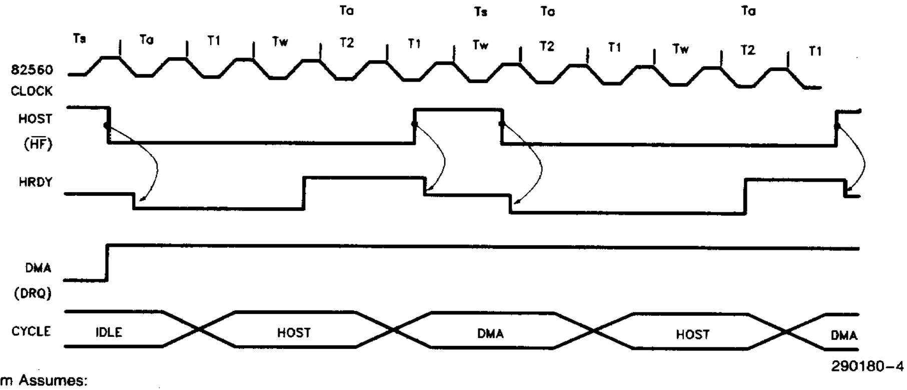
In I/O-mapped Access mode the memory is mapped into the host I/O address space. Data is transferred between host and local memory using host DMA or string I/O instructions. The 82560 can be programmed to support memory accesses through a single I/O port. The I/O port is defined by an address programmed into an 82560 register. The 82560 maintains the current address, which is updated each time a memory cycle is run. The host does not directly access the local memory. It outputs the I/O address onto the A0–A12 address lines, with the HF lines indicating a memory access. If the I/O address matches the address programmed into the 82560, then the 82560 executes the local memory cycle by outputting the current address onto the memory address lines MA0–12.

The 82560 can be configured to interface with the host in a pipeline mode. In this mode, transparent or edge-trigged latches are needed to isolate the host and local bus during memory cycles. Data is written to the latch (from the host bus) and copied (from the latch) to the local memory. In the host read cycles, data is copied from the latch to the host bus. In anticipation of the next host memory request (sequential), the 82560 then copies the next byte or word from local memory to the latch. Thus the host CPU can operate with 0 wait states by reading from and writing to the latch.

ARBITER

All requests for access to devices on the local bus, whether by the host or by the 82560 DMA, undergo arbitration. The host requests are indicated on the HF lines; the DMA requests are indicated on the DRQ lines. Figure 4 shows the basic arbitration cycle of the 82560. Arbitration for the local bus is pipelined. It can take place at any time when the 82560 is idle, or one clock before the end of the current local bus cycle. All requests are sampled on the falling edge of the 82560 clock. Arbitration is completed within one clock cycle. The resultant local bus cycle is started on the falling edge of the next clock. If more than one request is active, arbitration is resolved on an alternating priority basis.

The 82560 deactivates its HRDY line when a host request is detected; the request is synchronized and then arbitrated. If the request is granted, the appropriate local bus cycle begins. After a programmable number of clock cycles HRDY will be reactivated, and the handshake with the host will be complete. DMA requests are synchronized and acknowledged once DMA has been granted access to the local bus. The acknowledge lines are kept inactive until the DMA is granted access to the local bus.



This Diagram Assumes:
The default priority bit to be 1 (bit 7 of the master mode)
I/O or MEM wait states to be 1 clock (Tw = 1)
Non-Pipeline Mode
In the case of host read cycles (in any mode) or host write cycles (in pipeline mode only), "Twh" cycles will be asserted in addition to "Tw", between "T1" and "T2" of the host cycles

Figure 4. 82560 Arbitration Cycles

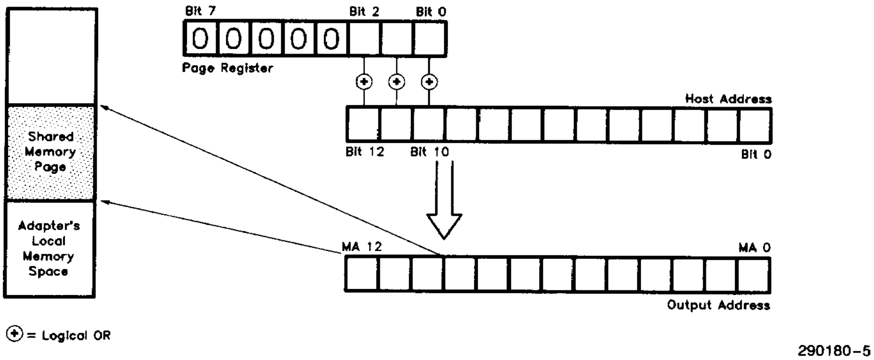


Figure 5. Page Mechanism

DMA MACHINE

The 82560 provides two DMA channels. Each channel can access 16 kb of memory address, and has request and acknowledge lines and address registers. The DMA normally operates in the Demand mode, and becomes active in response to a DMA request being granted. The requests come in on the DRQ lines and, if granted, are acknowledged by the DACK lines becoming active. Each channel has a control register that includes an enable bit, a direction bit, and output enable bits ($\overline{CS}$, $\overline{DACK0}$, and $\overline{DACK1}$ are active low signals that can be enabled/disabled during DMA cycles). Each channel also has a base, current, stop, lower-limit, and upper-limit register. The current address register (CAR) is incremented after every DMA transfer except when in double host bus mode. The lower-limit register points to the beginning of the ring buffer; the upper-limit register points to the end of the ring buffer. The 82560 performs the wraparound (lower limit to CAR), each time the CAR equals the upper limit. When the contents of the CAR equal those of the stop register, DMA transfer stops and the 82560 generates an interrupt to the CPU. When the double host bus mode is invoked, the DMA machine will alternately activate low and high banks of memory and will increment the address after each high-bank transfer.

LOOSELY COUPLED MODE

The 82560 performs flyby DMA transfers (read from slave and write to memory or vice versa). The operation continues until the current address register equals the stop register or until the DRQ is removed. When the stop register is reached, the 82560 generates an interrupt.

82590 TIGHTLY COUPLED MODE

The Tightly Coupled Interface is a hardware interface between the 82560 and the 82590. This interface allows transmission and reception events to be processed without CPU intervention. It allows the implementation of the time-critical CSMA/CD processes: automatic retransmission, buffer reclamation, and continuous frame reception and transmission. The basic interface is a two-signal DMA handshake between the 82560 and the 82590; this occurs over the DRQ and $\overline{\text{EOP}}$ pins. The 82590 provides the status of the current transmit or receive process, or requests another DMA cycle at the end of each DMA cycle. When configured for the Tightly Coupled Interface, the 82560 and the 82590 use a specific interrupt scheme to minimize CPU overhead and to improve data throughput. The 82590 will not generate interrupts when events occur that can be handled by the 82560 without CPU intervention. Figure 5 illustrates the Tightly Coupled Interface mechanism. Table 3 lists the various combination of the DRQ and $\overline{\text{EOP}}$ signals, and the events they represent.

Table 3. DMA Handshake Encoding

DRQ	$\overline{\text{EOP}}$	Event Status
0	0	Operation Done
0	1	Idle
1	0	Retry Request
1	1	New DMA Transfer Request

If both DRQ and $\overline{\text{EOP}}$ are sampled high, the Current Address Register of the channel is incremented and another DMA cycle begins. If a frame is transmitted or received without errors, both DRQ and EOP are low at the end of the DMA cycle and the 82560 will generate an interrupt. If DRQ is high and EOP is low, a collision occured during transmission, or an error occurred during reception. In this case the Current Address Register will be reloaded with the value in the Base Address Register; and, once again, it will point to the beginning of the frame structure in memory.

The $\overline{\text{DACK1}}/\overline{\text{CS1}}.\overline{\text{EOP}}$ pin of the 82590 is multiplexed and requires external logic to derive the EOP and CS1 signals (see 82590 data sheet). Because the 82560 integrates this logic, its $\overline{\text{DACK1}}/\overline{\text{EOP}}$ pin can be connected (with a pullup resistor) directly to the $\overline{\text{DACK1}}/\overline{\text{CS1}}/\overline{\text{EOP}}$ pin of the 82590, and its $\overline{\text{DACK0}}/\overline{\text{DACK}}$ pin can be connected directly to the DACK pin of the 82590. For more details, see the 8259X Users Manual.

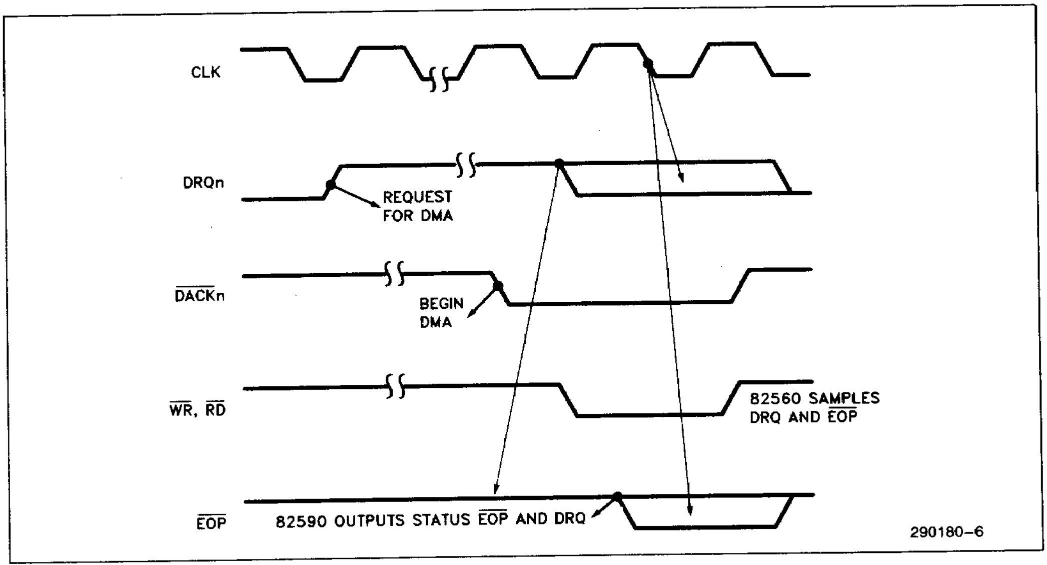


Figure 6. 82560, 82590 DMA Handshake

Transmit

The 82590 can transmit consecutive frames without using the CPU to issue the Transmit command each time. This improves data throughput during transmission and eliminates CPU overhead. The CPU can place multiple transmit frames in memory, with each frame separated from the next by a Transmit Command byte. (For further information see 82590 and 82592 user manuals.) The 82560 supports transmit chaining. It also supports automatic retransmit on collision (provided that the maximum number of collisions is not reached). In this case the current address register is reloaded with the value of the base address register, and the DMA transfer is resumed without CPU involvement. If the maximum number of collisions has been reached, or if transmit failed for any other reason, the 82560 will need CPU intervention. Thus it will generate an interrupt to the CPU. At the end of transmission of each frame, the 82560 updates the status byte (indicating the number of collisions) in the memory.

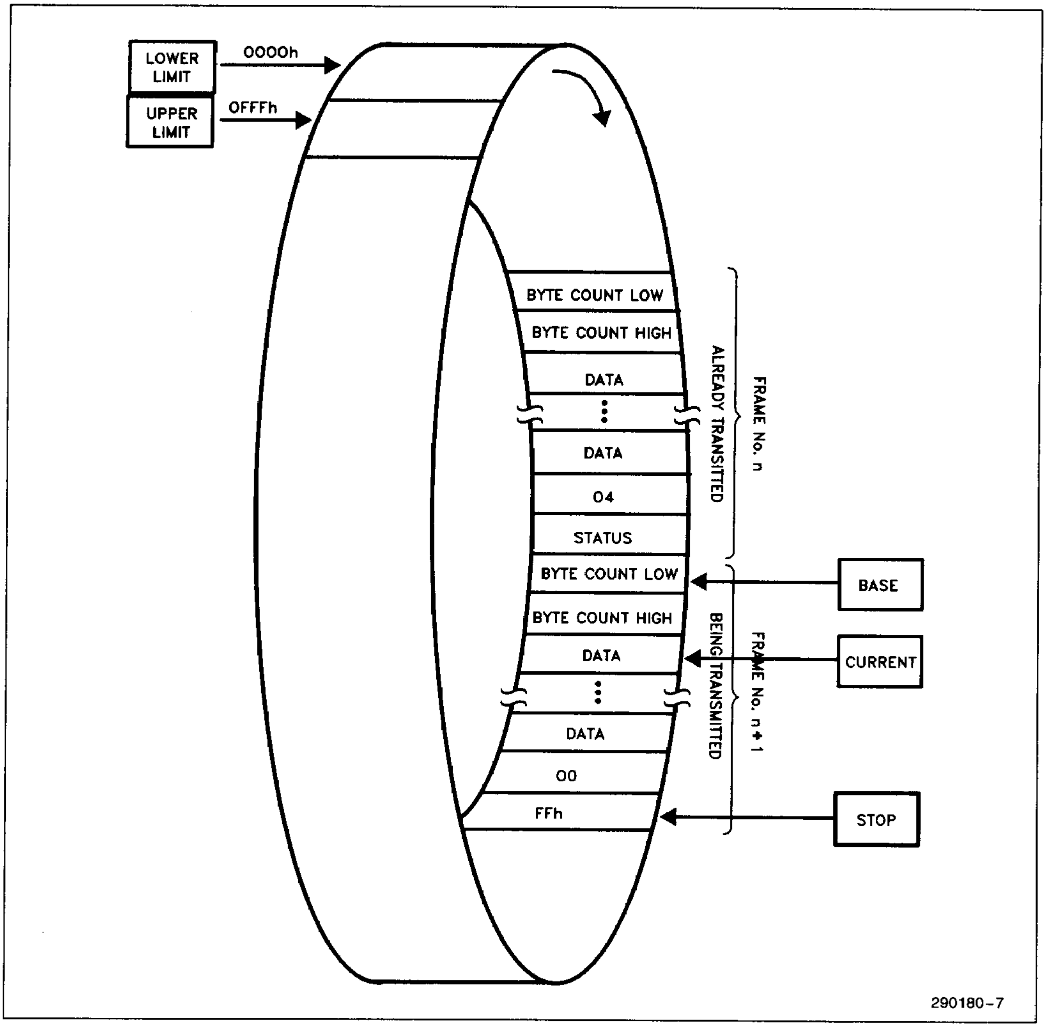


Figure 7. Example of a 4-kB Transmit Ring Buffer

Receive

Immediately after a channel is enabled for receive, the 82560 will write FFh into the first two bytes of the frame (pointed to by the base register). The current address register is loaded with the contents of the base register and is incremented twice (past the two reserved bytes). If an error occurs during reception, and the save bad frame bit is 0, the CAR is reloaded with the content of the BAR and incremented past the two reserved bytes; however, if the save bad frame bit is set, the CAR is incremented for the next frame and the 82560 generates an interrupt to the CPU. If no error occurs, the last two bytes received (which are always stored in 82560 internal registers) are copied back to the first two bytes of the frame. These are the byte counts. If the 82590 generates an interrupt on each frame reception the 82560 will relay that interrupt to the CPU. At this time the value of the CAR will be copied into BAR, FF will be written into the next two bytes, and CAR will be incremented as before to point to the new frame reception area.

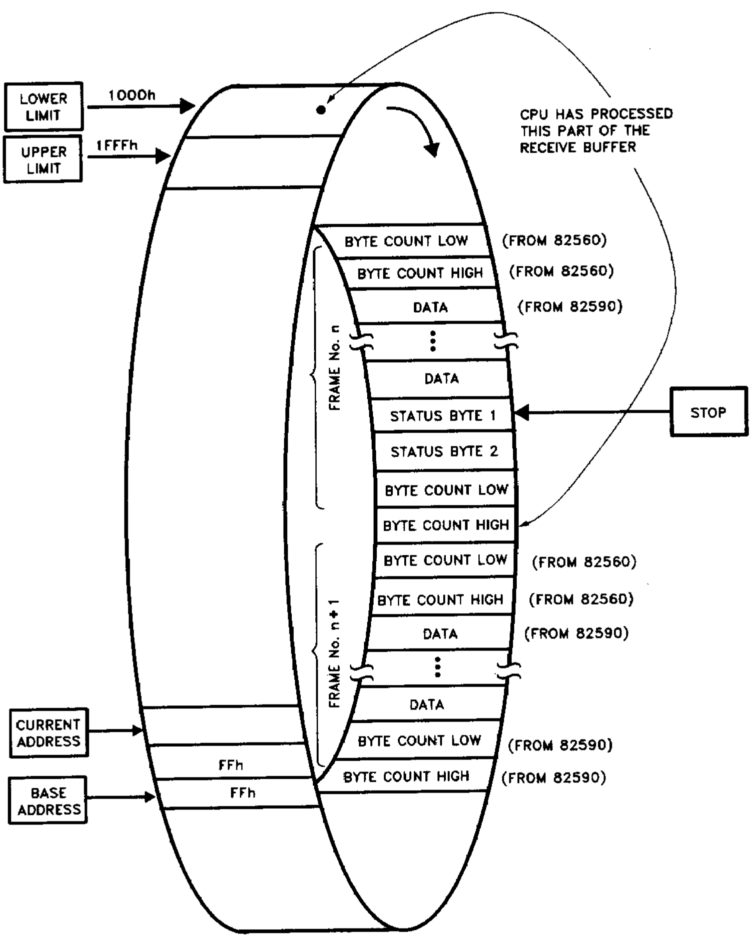


Figure 8. Example of a 4-kB Receive Ring Buffer

Table 4. Address Map

RESERVED	3Fh		
HOST MODE REGISTER	2Fh		
STOP 0	2Eh 2Dh 2Ch	3Eh 3Dh 3Ch	STOP 1
RESERVED	2Bh	3Bh	
UPPER LIMIT REGISTER 0	2Ah 29h 28h	3Ah 39h 38h	UPPER LIMIT REGISTER 1
RECEIVE TEMP. REGISTERS	27h	37h	
LOWER LIMIT REGISTER 0	26h 25h 24h	36h 35h 34h	LOWER LIMIT REGISTER 1
DMA CONTROL REGISTER 0	23h	33h	DMA CONTROL REGISTER 1
BASE ADDRESS REGISTER 0* — Base Current Bit = 1	22h 21h 20h	32h 31h 30h	BASE ADDRESS REGISTER 1 — Base/Current Bit = 1
CURRENT ADDRESS REGISTER 0† — Base Bit = 0	22h 21h 20h	32h 31h 30h	CURRENT ADDRESS REGISTER 1‡ — Base Bit = 0
DMA MODE REGISTER	1Fh		
HOST ADDRESS REGISTER H	1Eh 1Dh 1Ch		
SELECT REGISTER	1Bh 1Ah		
RESERVED	19h 18h		
INT MASK REGISTER	17h		
INT CONTROL/STATUS REGISTER	16h		
82588 STATUS 2 REGISTER	15h		
82588 STATUS 1 REGISTER	14h		
RESERVED	13h		
CONTROL REGISTER	12h		
IDENTIFICATION REGISTER	11h		
MASTER MODE REGISTER	10h		
SEMAPHORES	0Fh ↑ 08h		

	$\overline{CS}$	$\overline{DACK1}$	$\overline{DACK0}$	
SCS PORTS§	1	1	1	07h
	1	1	0	06h
	1	0	1	05h
	1	0	0	04h
	0	1	1	03h
	0	1	0	02h
	0	0	1	01h
	0	0	0	00h

* Base/Current bit refers to the read cycles only. When writing, both base and current are updated.

† 0 refers to DMA channel 0.

‡ 1 refers to DMA channel 1.

§ In the 8259X, address 03h and 05h are used for accessing Port 0 and Port 1 respectively.

NOTE:
When writing to 3-byte registers, the most significant byte (higher address) should be written last. The value written into the most significant bytes should be 0. The third bytes are reserved for possible future use.

82588 TIGHTLY COUPLED MORE

The 82560 supports a Tightly Coupled Interface (TCI) with the 82588. This interface allows transmit and receive events to be processed without CPU intervention. It allows the combination of the 82588 and 82560 to implement time-critical, CSMA/CD events: automatic retransmission, buffer reclamation, and continuous frame reception (see 82588 Reference Manual). When configured for the 82588 TCI mode, the 82560 uses the 82588 INT pin to determine if an event has occurred. The 82560 then reads the 82588 status register(s) to determine the cause of the interrupt. If the interrupt is due to a collision during transmission, a good frame reception, or errors during frame reception then the 82560 will update its DMA address registers and issue the 82588 the commands necessary for minimizing CPU intervention. The 82560 will regenerate all 82588 interrupts except those generated when a collision occurs during transmission (with the maximum retry count not exceeded). Because transmit and receive interrupts are time-critical processes the 82560 automatically acknowledges such interrupts to reduce dependency on the CPU. It will regenerate the interrupt on its INTOUT pin unless the interrupt is due to a transmit collision.

If the 82588 issues an interrupt due to a collision during transmission, and the maximum retry count has not been exceeded, the 82560 will automatically reload the Current Address Register with the value in the Base Address Register, acknowledge the interrupt, and issue a retransmit command to the 82588. If the interrupt is due to the reception of a good frame, the 82560 will update its Base and Current Address Registers and prepare for a new incoming frame. If the interrupt is due to a receive frame error, the 82560 will reclaim the buffer by resetting the Current Address Register to the beginning of the frame buffer.

If the 82588 is unable to transmit due to having exceeded the maximum retry count or a Lost-CTS condition or a Lost-CRS condition, an interrupt is generated; the 82560 will not update its DMA address registers. It will, however, acknowledge the 82588 interrupt and regenerate the interrupt on its INOUT pin.

PROGRAMMING

The 82560 registers may be logically grouped into Device Configuration registers, Status registers and DMA address registers. Table 4 shows all of the 82560 registers and their addresses. All registers except receive temporary registers, 82588 status 1 and 2 registers, and the identification register, which are read only, are read/write registers.

The registers can be accessed by the host CPU. The $\overline{RD}$ signal indicates the direction of data transfer between the 82560 and the CPU. The actual data transfer takes place over the 82560's 8-bit data bus lines (D_7-D_0). The address of the register being accessed is taken from the address lines A_5-A_0.

Since the 82560's data bus is 8-bits wide, all access to its registers is on a byte basis. If a register is longer than 1 byte, each byte has to be accessed individually through its unique address in the 82560 register space.

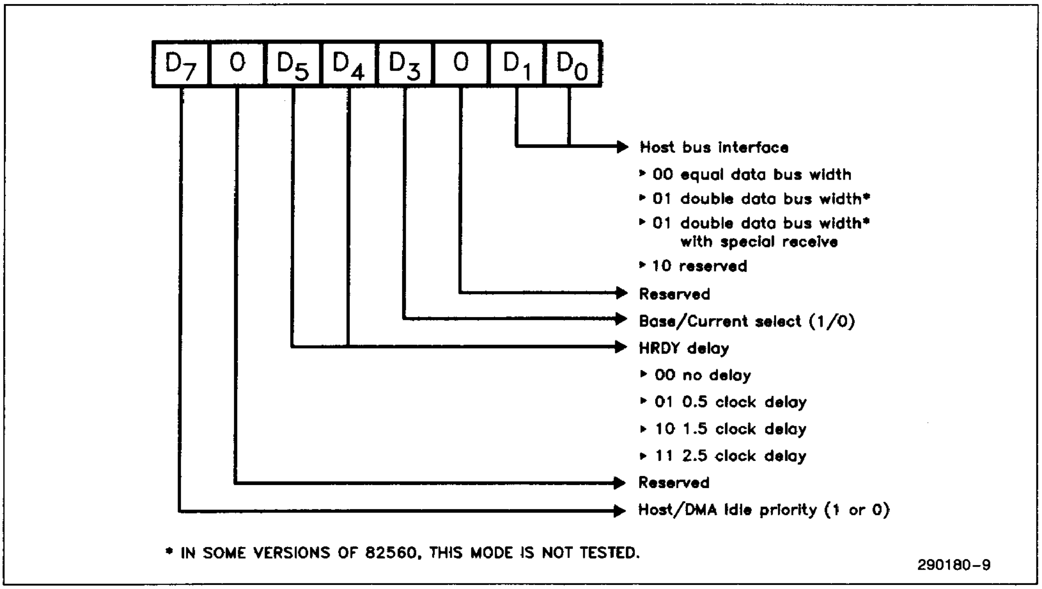
On power-up or reset, the 82560 registers are set to a default configuration. The user must initialize the 82560 for the proper system configuration.

The SCS ports occupy eight addresses in the 82560 register space. The SCS ports should not be thought of as registers. They are merely addresses in the register space which, when addressed, activate a combination of the $\overline{DACK0}$, $\overline{DACK1}$ or $\overline{CS}$ pins. The particular combination of these pins signal levels depends on the SCS port address being accessed. The semaphore ports allow resource sharing in a dual processor (intelligent adapter) environment. Each port can be used as a semaphore to implement mutual exclusion.

CONFIGURATION REGISTERS

By programming these registers, the 82560 can be tailored to support different PCs, slaves and memories. The memory access mode (I/O or memory mapped) and the type of DMA support (loosly or tightly coupled) can also be programmed.

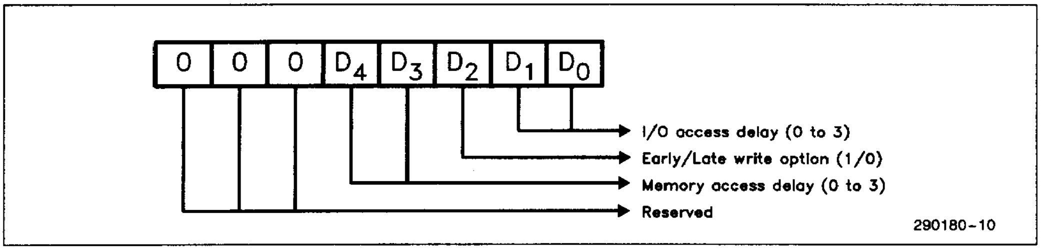
MASTER MODE REGISTER (10h)


D7 0 D5 D4 D3 0 D1 D0
Host bus interface
▸ 00 equal data bus width
▸ 01 double data bus width*
▸ 01 double data bus width* with special receive
▸ 10 reserved
Reserved
Base/Current select (1/0)
HRDY delay
▸ 00 no delay
▸ 01 0.5 clock delay
▸ 10 1.5 clock delay
▸ 11 2.5 clock delay
Reserved
Host/DMA idle priority (1 or 0)

* IN SOME VERSIONS OF 82560, THIS MODE IS NOT TESTED.

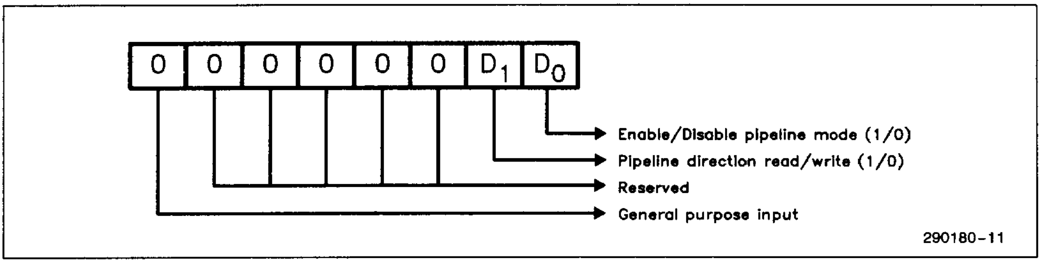
290180-9

CONTROL REGISTER (12h)


0 0 0 D4 D3 D2 D1 D0
I/O access delay (0 to 3)
Early/Late write option (1/0)
Memory access delay (0 to 3)
Reserved

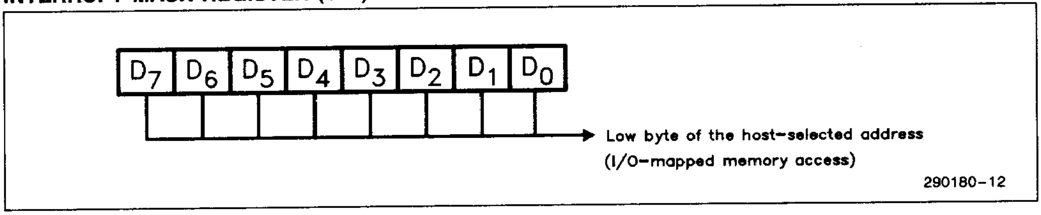
290180-10

HOST MODE REGISTER (2Fh)

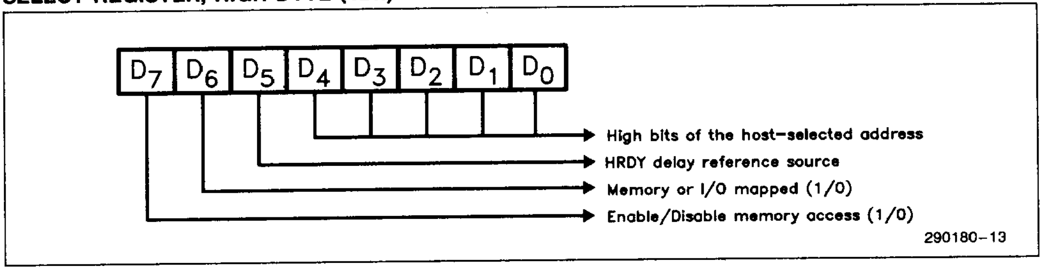

0 0 0 0 0 0 D1 D0
Enable/Disable pipeline mode (1/0)
Pipeline direction read/write (1/0)
Reserved
General purpose input

290180-11

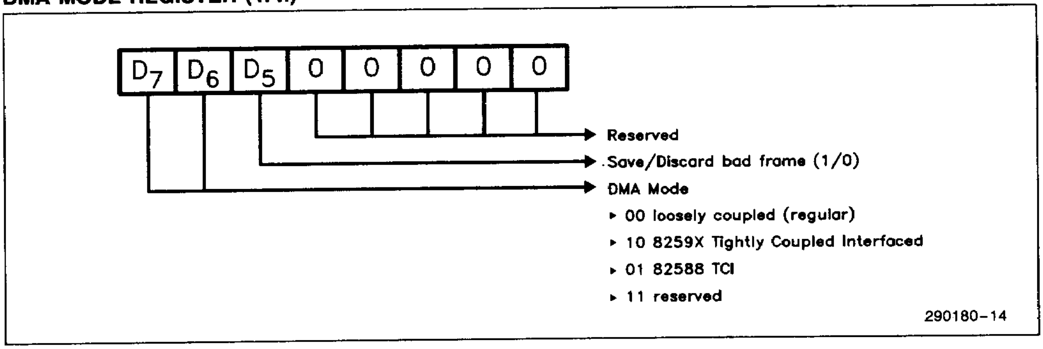
INTERRUPT MASK REGISTER (17h)


D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
Low byte of the host-selected address (I/O-mapped memory access)
290180-12

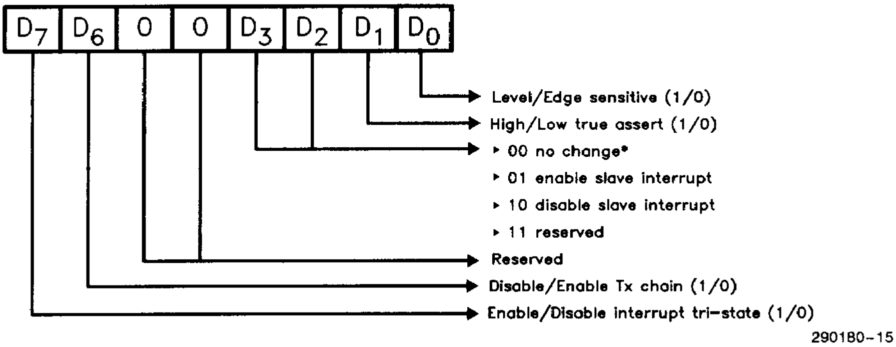
SELECT REGISTER, HIGH BYTE (1Bh)


D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
High bits of the host-selected address
HRDY delay reference source
Memory or I/O mapped (1/0)
Enable/Disable memory access (1/0)
290180-13

DMA MODE REGISTER (1Fh)


D_7 D_6 D_5 0 0 0 0 0
Reserved
Save/Discard bad frame (1/0)
DMA Mode
▸ 00 loosely coupled (regular)
▸ 10 8259X Tightly Coupled Interfaced
▸ 01 82588 TCI
▸ 11 reserved
290180-14

INTERRUPT MASK REGISTER (17h)


D7
D6
0
0
D3
D2
D1
D0
Level/Edge sensitive (1/0)
High/Low true assert (1/0)
▸ 00 no change*
▸ 01 enable slave interrupt
▸ 10 disable slave interrupt
▸ 11 reserved
Reserved
Disable/Enable Tx chain (1/0)
Enable/Disable interrupt tri-state (1/0)
290180-15

*Whenever one of these bits is "1" while writing to this register, other bits are not affected.

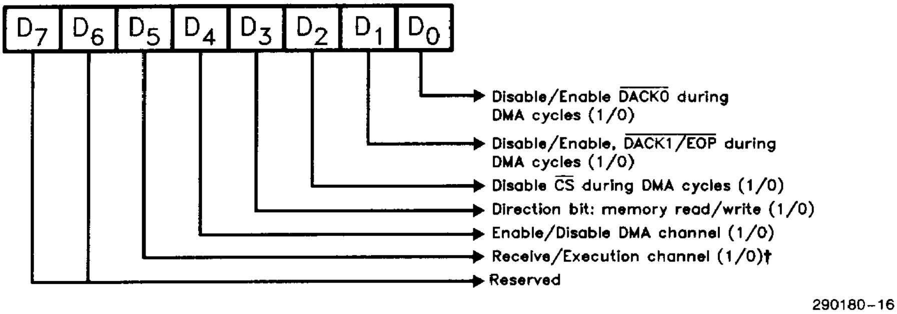
Host Address Registers

Contain the initial memory address when the host accesses memory in I/O mapped or pipeline mode.

Identification/Software Reset Register

Writing to this address will reset the chip. Reading from it will provide the user with 82560 stepping information.

MASTER MODE REGISTER (10h) DMA Control Register* (23h or 33h)


D7
D6
D5
D4
D3
D2
D1
D0
Disable/Enable $\overline{\text{DACK0}}$ during DMA cycles (1/0)
Disable/Enable, $\overline{\text{DACK1}}/\overline{\text{EOP}}$ during DMA cycles (1/0)
Disable $\overline{\text{CS}}$ during DMA cycles (1/0)
Direction bit: memory read/write (1/0)
Enable/Disable DMA channel (1/0)
Receive/Execution channel (1/0)†
Reserved
290180-16

D5	D3	DMA Channel Function
0	0	Transmit
0	1	Dump (588 or 590/592)
1	0	Reserved (Do Not Use)
1	1	Receive

*Each DMA channel has its own control register.
†The following table shows the encoding of bits 3 and 5:

INTERRUPTS

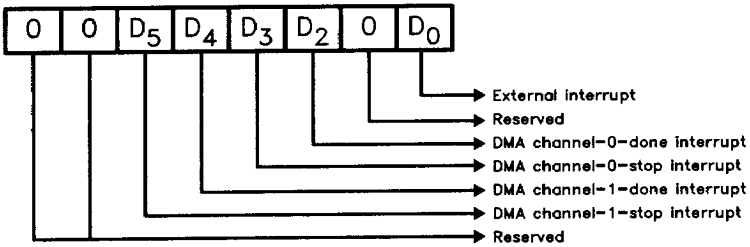
In the non-tightly coupled mode, the 82560 will generate an interrupt when the Current Address register equals the Stop register or when the interrupt input pin is active.

In the tightly coupled modes, the conditions for generating Stop register interrupts are the same however, the 82560 will generate 82590 interrupts only if its source was one of the following.

- Transmission of every frame, or last frame, in the chain is completed (programmable).
- Transmission failed because of a collision, and the maximum number of Transmit retries is reached.
- Transmission failed for a reason other than collision; e.g., lost CRS/CTS.
- Reception failed, and the Save Bad Frame bit is set.
- Reception completed.

The interrupt control register is read by the interrupt routines to determine the exact source of the interrupt.

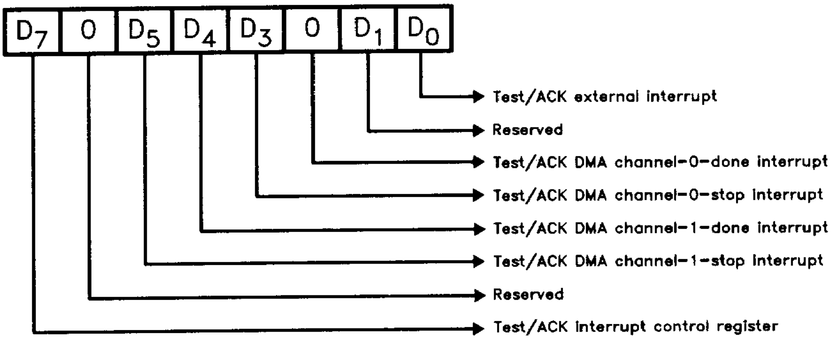
INTERRUPT STATUS READ REGISTER (16h)


0
0
D_5
D_4
D_3
D_2
0
D_0
External interrupt
Reserved
DMA channel-0-done interrupt
DMA channel-0-stop interrupt
DMA channel-1-done interrupt
DMA channel-1-stop interrupt
Reserved

290180-17

NOTE:
The interrupt control register is written to acknowledge and reset the interrupt.

INTERRUPT CONTROL WRITE REGISTER (16h)


D_7
0
D_5
D_4
D_3
0
D_1
D_0
Test/ACK external interrupt
Reserved
Test/ACK DMA channel-0-done interrupt
Test/ACK DMA channel-0-stop interrupt
Test/ACK DMA channel-1-done interrupt
Test/ACK DMA channel-1-stop interrupt
Reserved
Test/ACK interrupt control register

290180-18

SYSTEM INTERACTION

A typical 82560 system interaction is described below.

1. The CPU configures the 82560 by writing to configuration registers.

2. The CPU accesses the local memory (through the 82560) and prepares a block of transmit frames.

3. The CPU writes the proper addresses into the 82560's DMA address registers, (base, current, lower limit upper limit and stop).

4. The CPU writes to the 82560's DMA control registers to configure and enable the channels.

5. The CPU issues a transmit command to the 82590.

6. The 82560 responds to the 82590's DMA request by transferring data from memory to the 82590.

7. Upon completion of transmission, the 82560 sends an interrupt to the CPU.

8. The CPU reads the 82560 interrupt control register to find the source of the interrupt.

9. The CPU issues a command to the 82590 to clear its interrupt. (If the source of the interrupt was the 82590.)

10. The CPU acknowledges the 82560 interrupt by writing a "1" into the corresponding interrupt control register bit(s).

APPLICATIONS

Figure 9 shows a buffered, nonintelligent StarLAN adapter for the IBM PC bus (using the 82560 and the 82590). Figure 10 shows a buffered, nonintelligent Ethernet adapter for the IBM PC bus (using the 82560, 82592, 82C501 and the 82502).

82560 MACHINE CYCLE

The 82560 machine cycle can be broken down into three basic cycles: Idle (T_{IDLE}), Arbitration (T_A) and Transfer (T_{TSF}). The machine cycle begins when a request (HF or DRQ) becomes active and the 82560 is in the idle state (T_{IDLE}). The requests are synchronized and then undergo arbitration (T_A). Once arbitration is completed, the transfer cycle (T_{TSF}) begins.

Synchronization (T_S) is completed on the falling edge of the clock. If the previous cycle was non-idle, arbitration begins and is completed within one clock period (by the next falling edge of the clock).

The Transfer cycle consists of the following sequential states: the first transfer state (T_1), memory or I/O wait states (T_W), and the second transfer state (T_2). There may be another transfer state, T_{wh} (wait host), during host read or pipeline cycles. When no requests are pending, and the 82560 is not in the transfer or arbitration cycle, it is said to be in the idle state (T_{IDLE}). If the previous cycle was non-idle, the arbitration period (T_A and T_2 of the previous cycle will be done in parallel. (See Figure 4.)

T_W is the programmable portion of the transfer cycle. It can be zero to three clocks long depending on the programmed memory or I/O access delays. If the programmed delay is zero, then there will be no T_W; the first state of the transfer cycle will be T_1. During T_2 the transfer cycle is completed unless the cycle is a host read cycle. In that case the cycle will be extended by inserting T_{wh}. The 82560 will remain in T_{wh} until the HF lines are deasserted. Once HF lines are deasserted, T_2 will begin and one clock period later the bus cycle is complete.

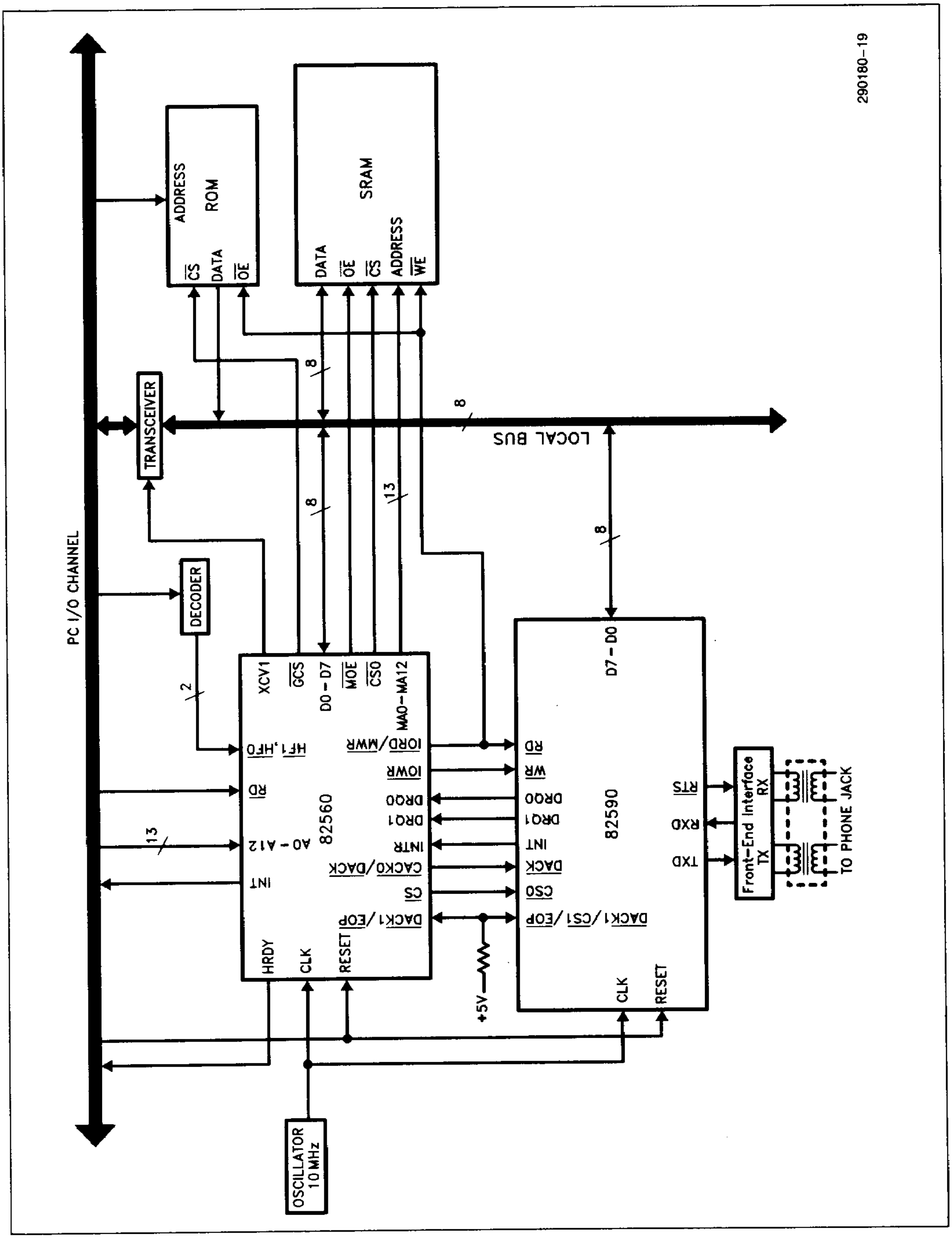


Figure 9. 590 High-Integration Adapter (560 and 590)

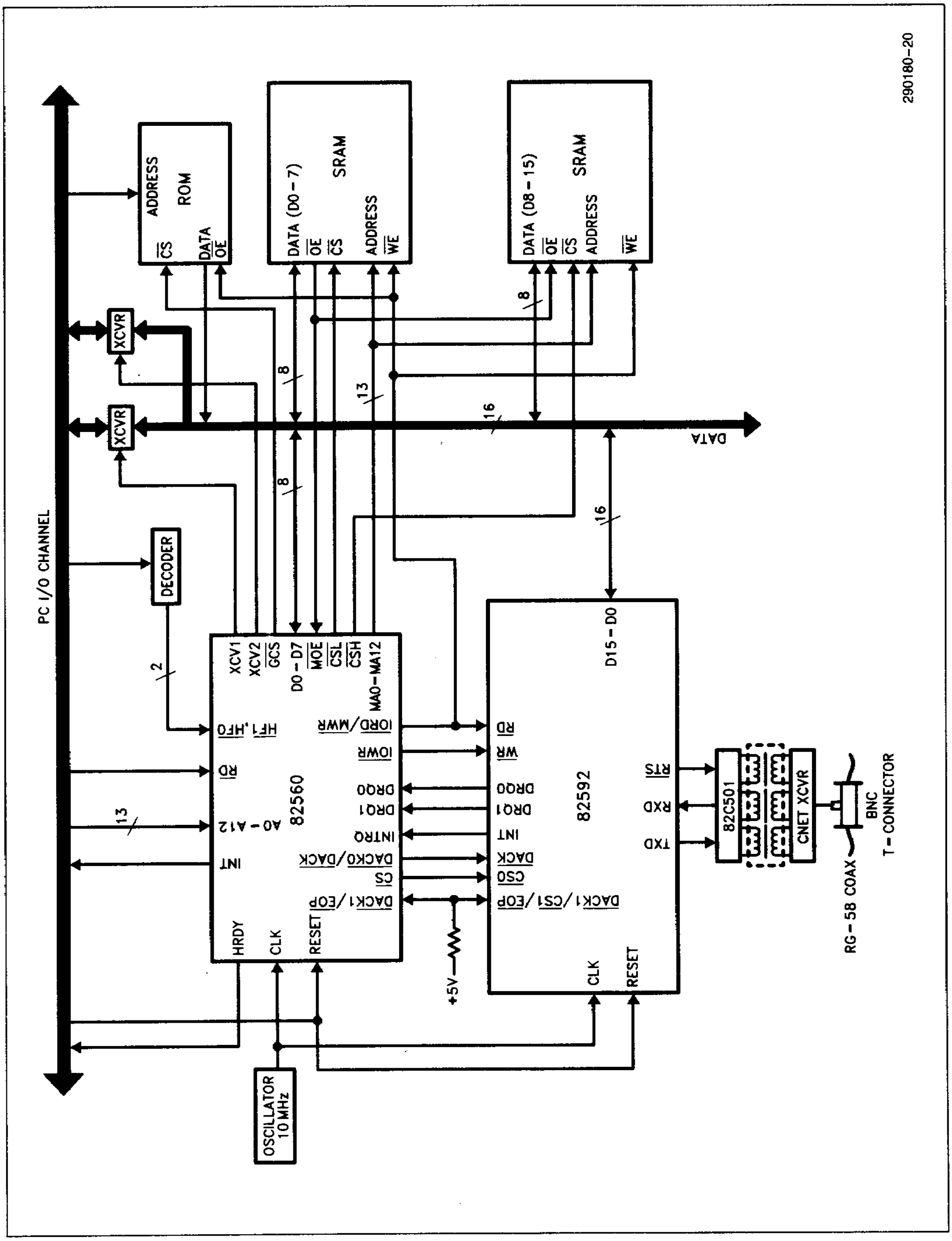


Figure 10. Cheapernet Adapter (82560, 82592, 82C501 and 82502)

ABSOLUTE MAXIMUM RATINGS*

Case Temperature (TC)
under Bias .... 0°C to +85°C

Storage Temperature .... −65°C to +150°C

Voltage on any Pin with
Respect to Ground .... −0.5V to V_{CC} + 0.5V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS TC = 0°C to +85°C, V_{CC} = +5V ±10%

CLK pin has MOS levels (see V_{MIL}, V_{MIH}) All other signals have TTL levels (see V_{IL}, V_{IH}, V_{OL}, V_{OH}).

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (TTL)	−0.5	+0.8	V	
V_{IH}	Input High Voltage (TTL)	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (TTL)		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (TTL)	2.4	V_{CC}	V	I_{OH} = −400 μA
V_{MIL}	Input Low Voltage (MOS)	−0.5	0.6	V	
V_{MIH}	Input High Voltage (MOS)	V_{CC} − 0.6	V_{CC} + 0.5	V	
I_{LI}	Input Leakage Current		±10	μA	0 = V_{IN} = V_{CC} −0.45
I_{LO}	I/O Leakage Current		∓10	μA	0.45 = V_{OUT} = V_{CC} −0.45
C_{IN}	Capacitance of Input Buffer		10	pF	FC = 1 MHz
C_{OUT}	Capacitance of Input/Output Buffer		20	pF	FC = 1 MHz
I_{CC}	Power Supply Current		50	mA	10 MHz

A.C. CHARACTERISTICS C_L on all outputs is 50 pF. The user should add 0.2 ns/pF up to 100 pF

Symbol	Parameter	Min	Max	Test Conditions
SYSTEM CLOCK INPUT PARAMETERS				
T1	CLK Cycle Period	100		(Note 1)
T2	CLK Low Time	45		(Note 1)
T3	CLK High Time	45		(Note 1)
T4	CLK Rise Time		5	(Note 2)
T5	CLK Fall Time		5	(Note 3)
HOST ACCESS CYCLE—NON PIPELINE MODE PARAMETERS				
T6	HF or DREQ Setup Time	10		
T7	HF Active Time (Low)	2*T1+10		(Note 5)
T8	HF Inactive Time (High)	T1+10		
T9	HF to HRDY Low		50	
T10	HF Active to HDRY High	2*T1+50	(Note 4)	(Note 9)
T11	HRDY High to HF Inactive	0		(Note 5)

A.C. CHARACTERISTICS

C_L on all outputs is 50 pF. The user should add 0.2 ns/pF up to 100 pF (Continued)

Symbol	Parameter	Min	Max	Test Conditions
HOST ACCESS CYCLE—NON PIPELINE MODE PARAMETERS (Continued)				
T12	HF Inactive to HRDY Float		75	
T13	HF Active to XCVR Lines Low	T1 + T2	2*T1 + T2 + 75	(Note 6)
T14	HF Inactive to XCVR Lines High	(Note 7)	75	
T15	HF Active to $\overline{\text{RD}}$ Low		T1 + T2 + 10	
T16	$\overline{\text{RD}}$ Hold after HF Inactive	0		
T17	HF Active to Input Add. Valid		−20	
T18	Address Hold after HF Inactive	0		(Note 8)
T19	HF Active to 82560 Data Valid		3*T1 + 80	(Note 9)
T20	Data Hold after HF Inactive	T1 + T2		
T21	HF Active to 82560 Add Valid (MAn).		2*T1 + T2 + 75	(Note 9)
T22	Add Valid or Chip Select Active Time	2*T1	(Note 10)	
T23	HF Active to $\overline{\text{CS}}$ Active		2*T1 + T2 + 50	(Note 9)*
T24	$\overline{\text{CS}}$ Enveloping Controls	20		
T25	Control Active Time	(Note 11)	(Note 11)	
T26	HF to Data Valid		3*T1-30	
T27	Data Hold after HRDY High	(Note 12)		
HOST ACCESS CYCLE—PIPELINE MODE PARAMETERS				
T28	HF Active Time	T1 + 10	(Note 13)	(Note 9)
T29	HF Active to Port CS Active		2*T1 + 75	(Note 6)
T30	HF Inactive to HRDY Low		75	
T31	HRDY Low to HRDY High		(Note 14)	
T32	Port CS Active Time	2*T1	(Note 14)	
T33	HF Inactive to Buffer Write	10		
T34	Write Active Time	T1-10	T1 + 10	
DMA PARAMETERS				
T35	DRQn High or INTR to Clock Low Setup Time	50		(Note 15)
T36	DRQn Low to Clock Low, Hold Time	10		
T37	$\overline{\text{EOP}}$ Pulse Width	T1		
T38	Address Delay Time		T2 + 75	
T39	$\overline{\text{CS}}$, $\overline{\text{CSn}}$, $\overline{\text{DAKn}}$ Delay Time		T2 + 50	
T40	$\overline{\text{CSn}}$ Delay Time (Slave to SRAM Flyby)		50	
T41	$\overline{\text{IORD}}$__$\overline{\text{MWR}}$, $\overline{\text{IOWR}}$ Delay Time		45	
T42	$\overline{\text{IORD}}$__$\overline{\text{MWR}}$, $\overline{\text{IOWR}}$ Active Time	(Note 16)	(Note 16)	

A.C. CHARACTERISTICS

C_L on all outputs is 50 pF. The user should add 0.2 ns/pF up to 100 pF (Continued)

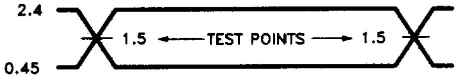
Symbol	Parameter	Min	Max	Test Conditions
INTERRUPT PARAMETERS				
T43	Interrupt Delay Time		75	
T44	Interrupt Gap	3*T1-10		
RESET PARAMETERS				
T45	Reset Setup Time	50		
T46	Reset Active Time (High)	4*T1		

*For pin HRDY 4 mA.

NOTES:

1. Measured at $V_{CC}/2$.
2. 3.2V to 1.8V.
3. 1.8V to 3.2V.
4. The following configuration affect the HRDY output going active (high).
   Legend:
   TID—The configuration of HRDY delay (master mode register, TID = 0,.5,1.5,2.5).
   TIO—The configuration of I/O access delay (Control register,
   TIO = 0,1,2,3).
   TMEM—The configuration of MEM access delay (Control register, TMEM = 0,1,2,3).
   "If bit 5 of Register at Address 1BH then (TID+2)*T1+75
   else [TID+TIO(or TMEM)+2]*T1+75"
5. The user should not that the XCVR lines goes inactive immediately after HF inactivation.
6. Provided that the HOST wins arbitration.
7. In the case of HOST write cycle the XCVR lines will go high at the end of the 82560 cycle even if HF lines are still active. In the case of HOST read cycles, the 82560 will terminate the local cycle after HF lines are inactivated.
8. Address lines are latched at the end of T1 of 82560 HOST bus cycles.
9. The maximum time specified assumes that the HOST wins the arbitration. If the HOST loses the arbitration to a DMA request two possible scenerios are:
   a) Arbitration lost to a single DMA cycle. In this case [(greater of TIO and TMEM)+2]*T1 should be added to the max. time.
   b) Arbitration lost to a DMA cycle which is followed by four locked DMA cycles. In this case [(greater of TIO and TMEM)*5 + 10]*T1 should be added to the max. time. This might happen in the rare case when the HOST request coincides with the last receive or transmit transfer, in the TCI mode.
10. [TIO(or TMEM)+2]*T1+10.
    In the case of long (HF) HOST memory read requests, it would be extended until the request is removed.
11. Min = [TIO(or TMEM)+1]*T1-10, Max = [TIO(or TMEM)+1]*T1+10.
12. This parameter depends on T10. In terms of machine states, data remains valid until the end of the cycle (end of state T2).
13. (TMEM + 2)*T1+75+ Tsystem.
    Tsystem = delay from HRDY to HF inactive.
    This maximum time refers to a second memory request immediately following a first one, assuming that the first one was not delayed by a DMA cycle.
14. [TIO(or TMEM)+2]*T1+75.
15. This is an asynchronous signal (DRQn only in its leading edge). It is internally synchronized. Meeting this parameter, assures recognition on the next clock.
16. Min = [(greater of TIO and TMEM)+1]*T1+T2+10
    Max = [(greater of TIO and TMEM)+1]*T1+T2+10

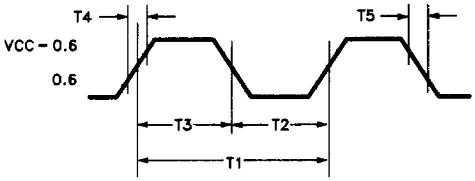
A.C. TESTING INPUT & OUTPUT WAVEFORM



290180-21

A.C. Testing Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 1.5V for both a Logic "1" and "0".

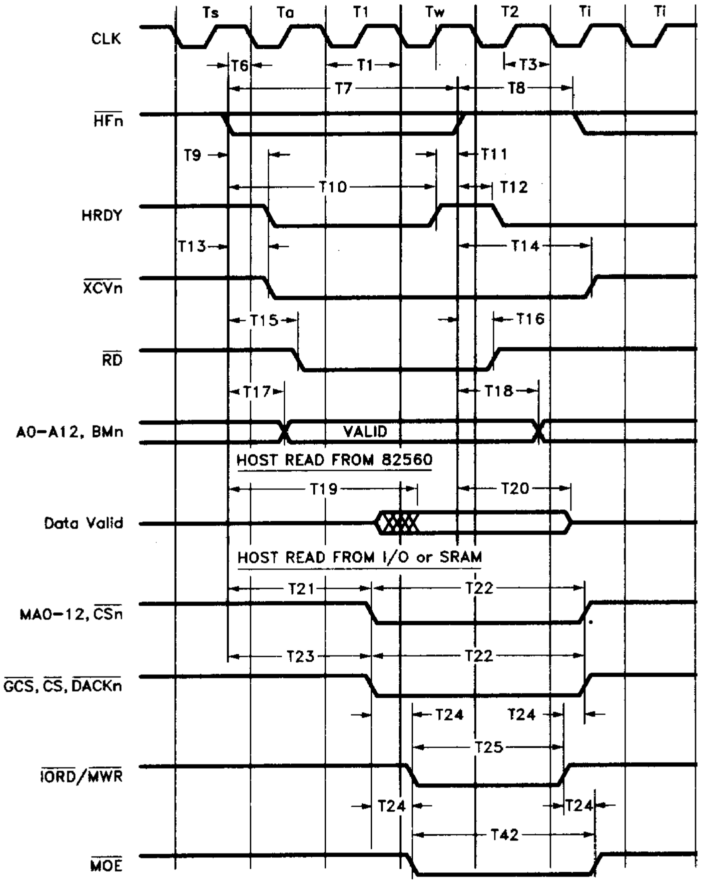
SYSTEM CLOCK TIMING



290180-22

WAVEFORMS

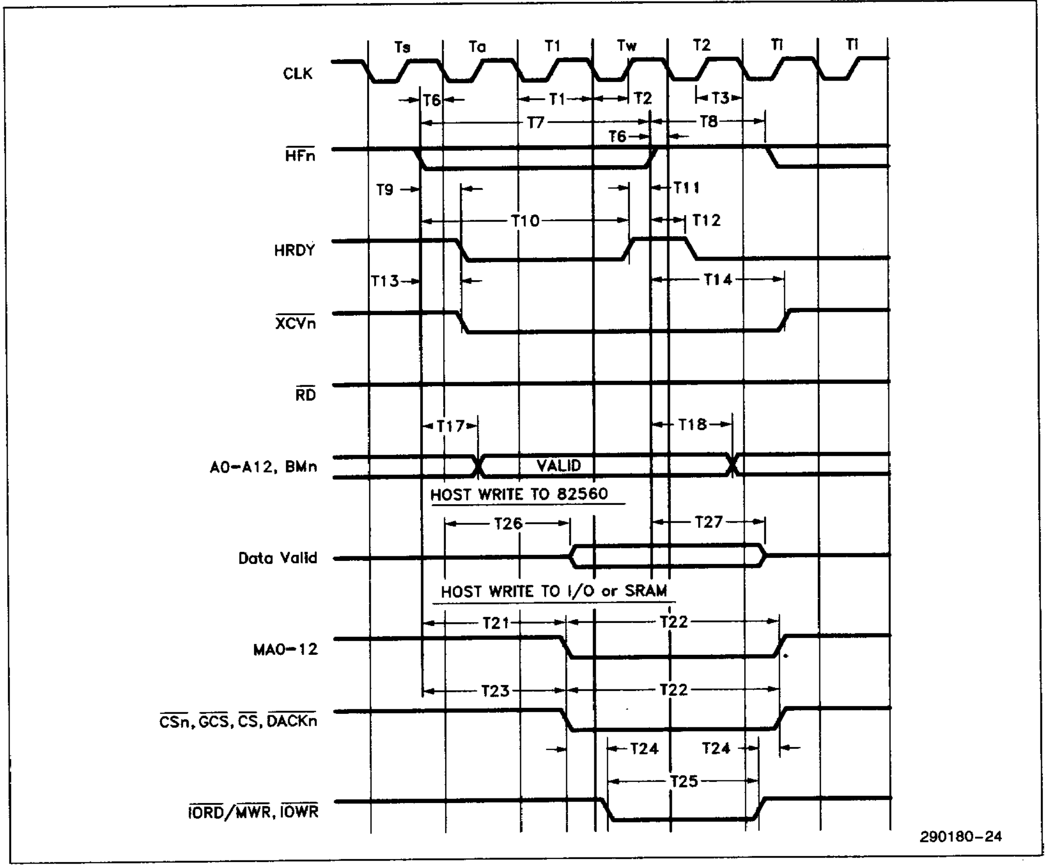
HOST READ CYCLE—NON PIPELINE MODE



290180-23

WAVEFORMS (Continued)

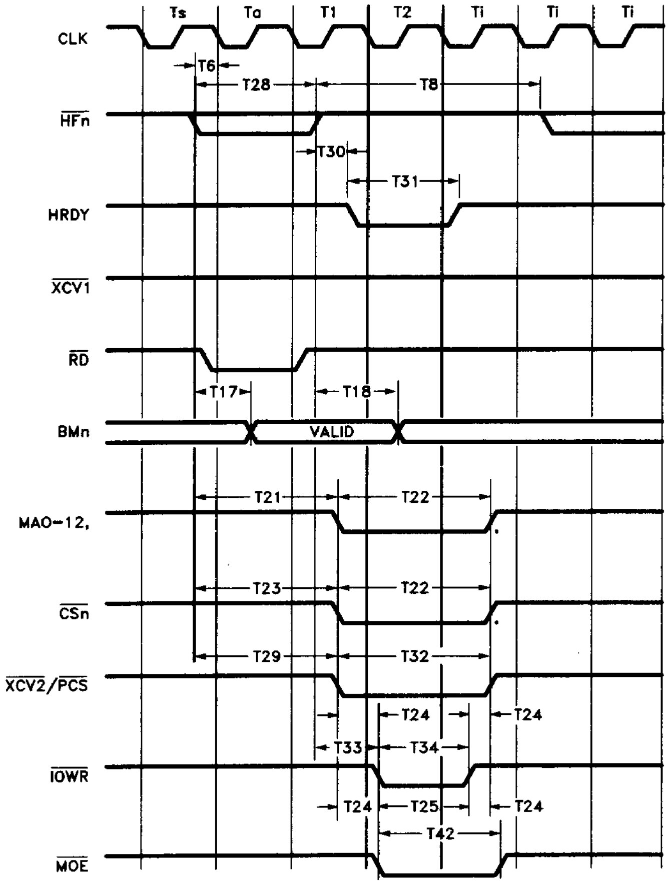
HOST WRITE CYCLE—NON PIPELINE MODE



290180–24

WAVEFORMS (Continued)

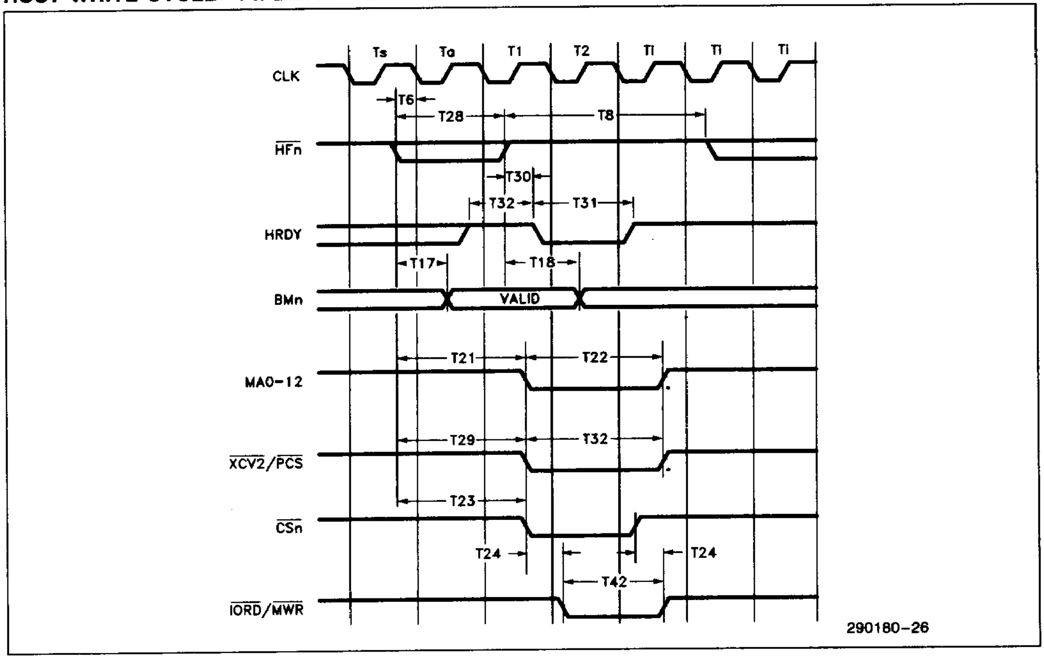
HOST READ CYCLE—PIPELINE MODE



290180-25

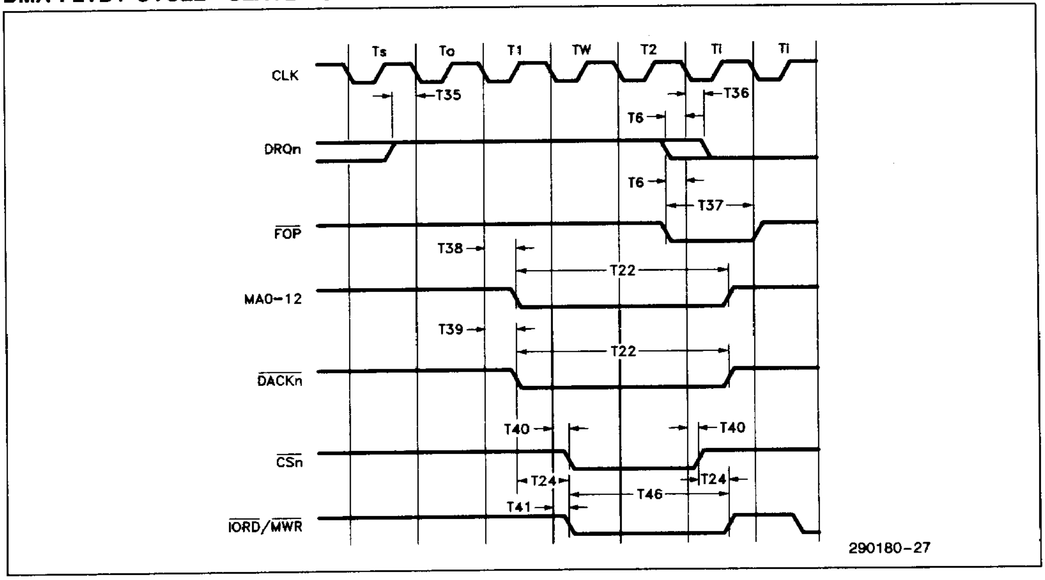
WAVEFORMS (Continued)

HOST WRITE CYCLE—PIPELINE MODE



290180-26

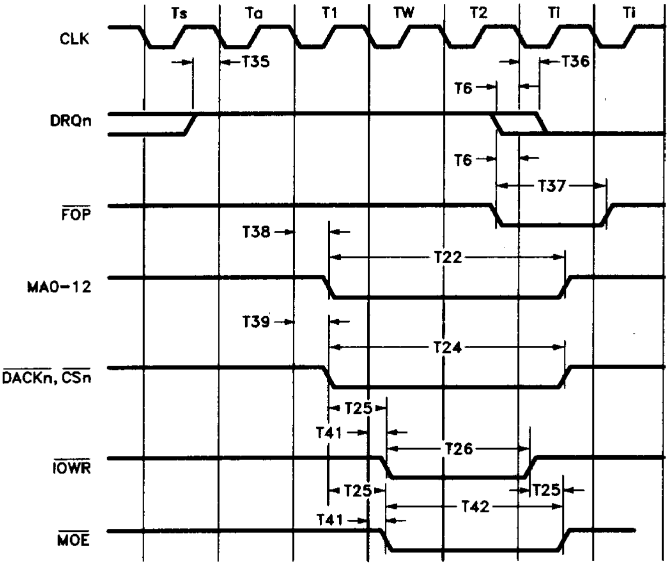
DMA FLYBY CYCLE—SLAVE TO SRAM



290180-27

WAVEFORMS (Continued)

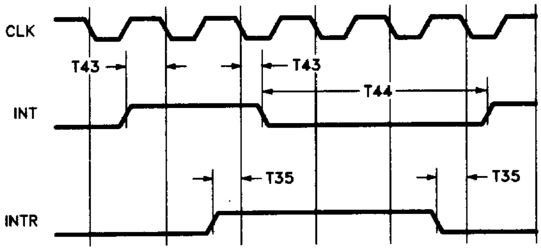
DMA FLYBY CYCLE—SRAM TO SLAVE



290180-28

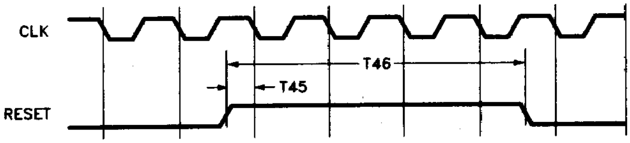
WAVEFORMS (Continued)

INTERRUPT



290180-29

RESET



290180-30