DENSE-PAC
MICROSYSTEMS

8 Megabit CMOS SRAM
DPS256S32AW

ADVANCED INFORMATION

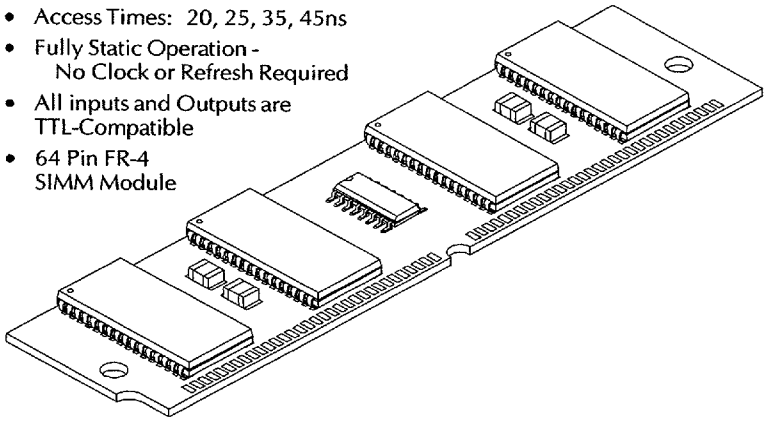
DESCRIPTION:

The DPS256S32AW is a 256K x 32 high-density, static RAM module comprised of eight 128K x 8 monolithic SRAM's, an advanced high-speed CMOS decoder, resistor network and decoupling capacitors surface mounted on a FR-4 SIMM substrate.

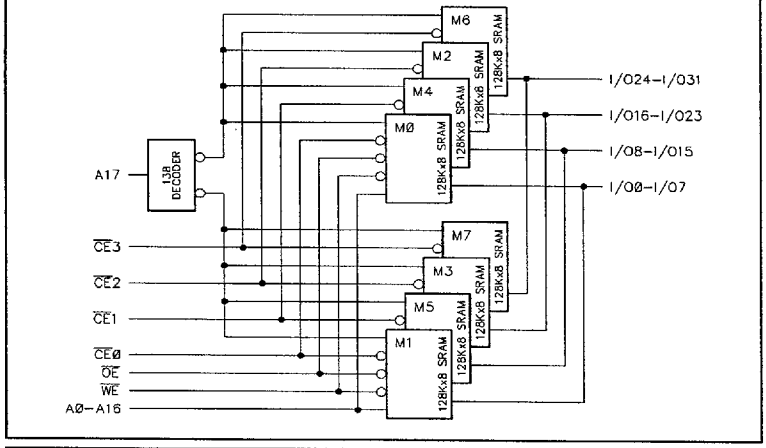
The DPS256S32AW operates from a single +5V supply and all input and output pins are completely TTL-compatible.

FEATURES:

- Configuration: 256K x 32, 512K x 16, 1M x 8
- Access Times: 20, 25, 35, 45ns
- Fully Static Operation - No Clock or Refresh Required
- All inputs and Outputs are TTL-Compatible
- 64 Pin FR-4 SIMM Module



FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM

TOP VIEW

INDEX

1	VSS	
2	N.C.	
3	N.C.	
4	I/O0	
5	I/O8	
6	I/O1	
7	I/O9	
8	I/O2	
9	I/O10	
10	I/O3	
11	I/O11	
12	VDD	
13	A0	
14	A7	
15	A1	
16	A8	
17	A2	
18	A9	
19	I/O12	
20	I/O4	
21	I/O13	
22	I/O5	
23	I/O14	
24	I/O6	
25	I/O15	
26	I/O7	
27	VSS	
28	$\overline{WE}$	
29	A15	
30	A14	
31	$\overline{CE1}$	
32	$\overline{CE0}$	
33	$\overline{CE3}$	
34	$\overline{CE2}$	
35	A17	
36	A16	
37	$\overline{OE}$	
38	VSS	
39	I/O24	
40	I/O16	
41	I/O25	
42	I/O17	
43	I/O26	
44	I/O18	
45	I/O27	
46	I/O19	
47	A3	
48	A10	
49	A4	
50	A11	
51	A5	
52	A12	
53	VDD	
54	A13	
55	A6	
56	I/O20	
57	I/O28	
58	I/O21	
59	I/O29	
60	I/O22	
61	I/O30	
62	I/O23	
63	I/O31	
64	VSS	

PIN NAMES	
A0 - A17	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE}$0 - $\overline{CE}$3	Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Operating Temp.	0	+25	+70	°C

CAPACITANCE[4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	90	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	90		
C_{OE}	Output Enable	90		
$C_{I/O}$	Data Input/Output	30		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -4.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS[3]		
Symbol	Parameter	Max.	Unit
T_{STC}	Storage Temperature	-40 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

DC OPERATING CHARACTERISTICS: Over operating ranges						
Symbol	Characteristics	Test Conditions		COMMERCIAL Min.	COMMERCIAL Max.	Unit
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-40	+40	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-10	+10	µA
I_{CC}	Operating Supply Current	Cycle = min., Duty = 100%, I_{OUT} = 0mA	x8		565	mA
			x16		690	
			x32		940	
I_{SB1}	Full Standby Supply Current (CMOS)	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V, $\overline{CE} \geq V_{DD}$ -0.2V			80	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IN}			440	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA		2.4		V

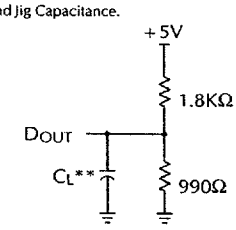
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Output Load		
Load	**C_L**	**Parameters Measured**
1	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}
2	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.

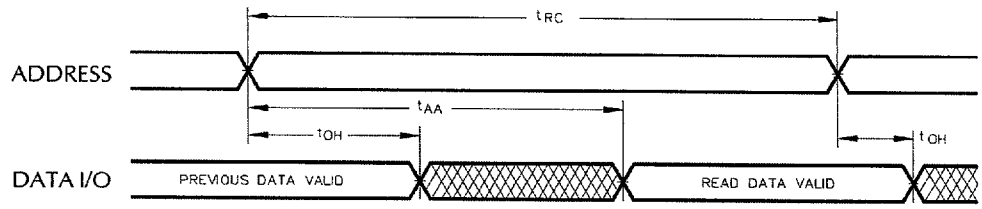


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	**Symbol**	**Parameter**	**20ns**		**25ns**		**35ns**		**45ns**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
1	t_{RC}	Read Cycle Time	20		25		35		45		ns
2	t_{AA}	Address Access Time		20		25		35		45	ns
3	t_{CO}	Chip Enable to Output Valid		20		25		35		45	ns
4	t_{OV}	Output Enable to Output Valid		8		10		25		35	ns
5	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	0		0		0		0		ns
7	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		10		12		25		25	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		8		10		15		20	ns
9	t_{OH}	Output Hold from Address Change	5		3		3		5		ns

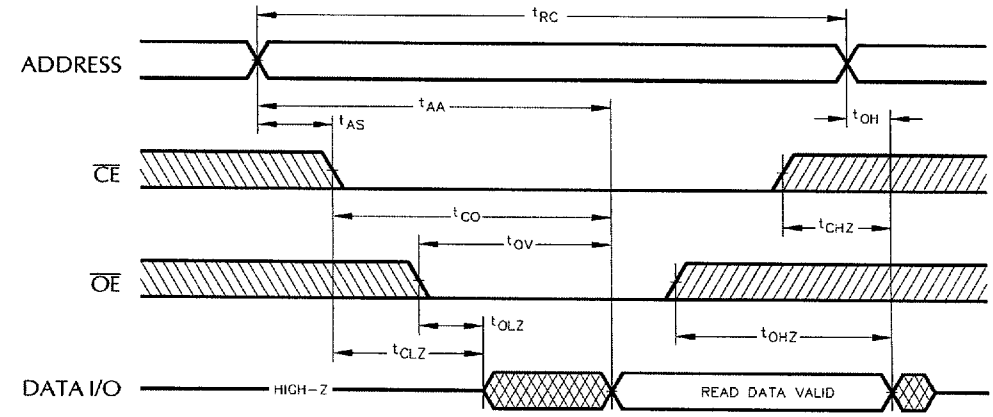
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [6, 7]											
No.	**Symbol**	**Parameter**	**20ns**		**25ns**		**35ns**		**45ns**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
10	t_{WC}	Write Cycle Time	20		25		35		45		ns
11	t_{AW}	Address Valid to End of Write	17		20		30		40		ns
12	t_{CW}	Chip Enable to End of Write	17		20		30		40		ns
16	t_{AS}	Address Set-up Time ***	0		0		0		0		ns
15	t_{WP}	Write Pulse Width	15		20		25		35		ns
17	t_{AH}	Address Hold Time	5		5		5		5		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		8		10		15		20	ns
13	t_{DW}	Data to Write Time Overlap	10		15		15		20		ns
14	t_{DH}	Data Hold Time from Write Time	0		0		0		0		ns
19	t_{OW}	Output Active from End of Write	3		3		3		5		ns

*** Valid for both Read and Write Cycles.

READ CYCLE 1: Address Controlled. WE is HIGH. CE and OE are LOW.



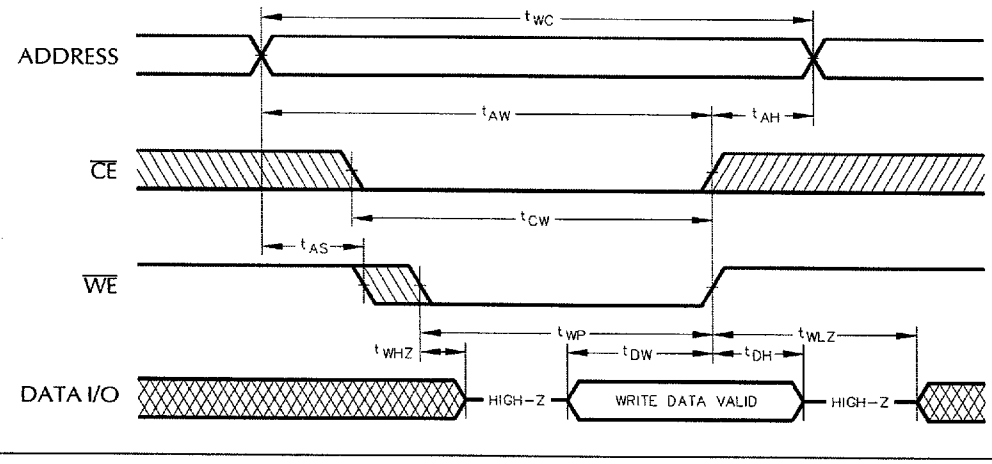
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



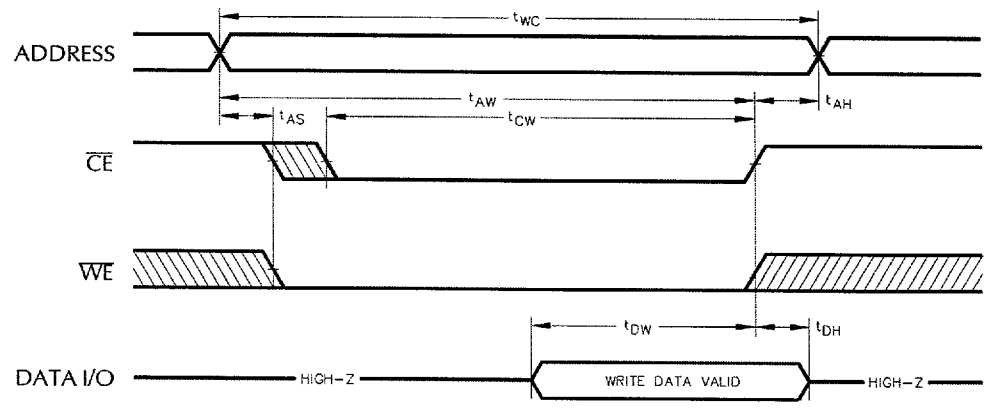
NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

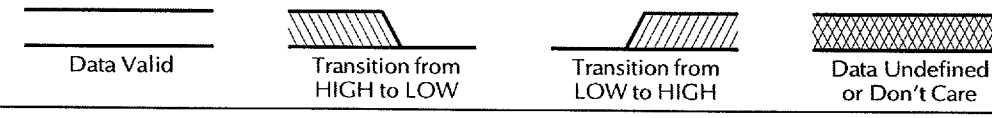
WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.

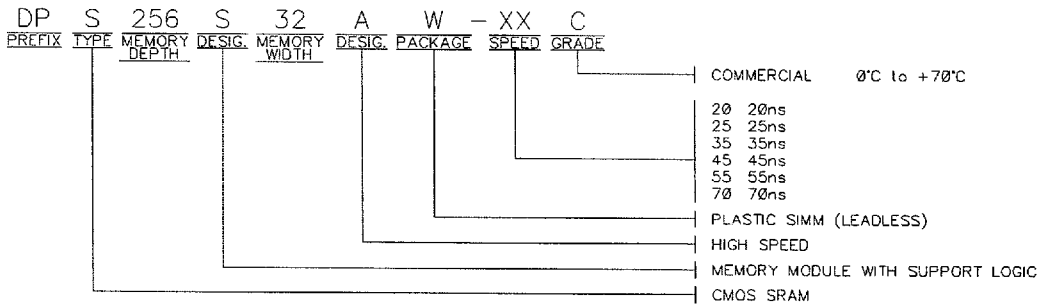


WAVEFORM KEY

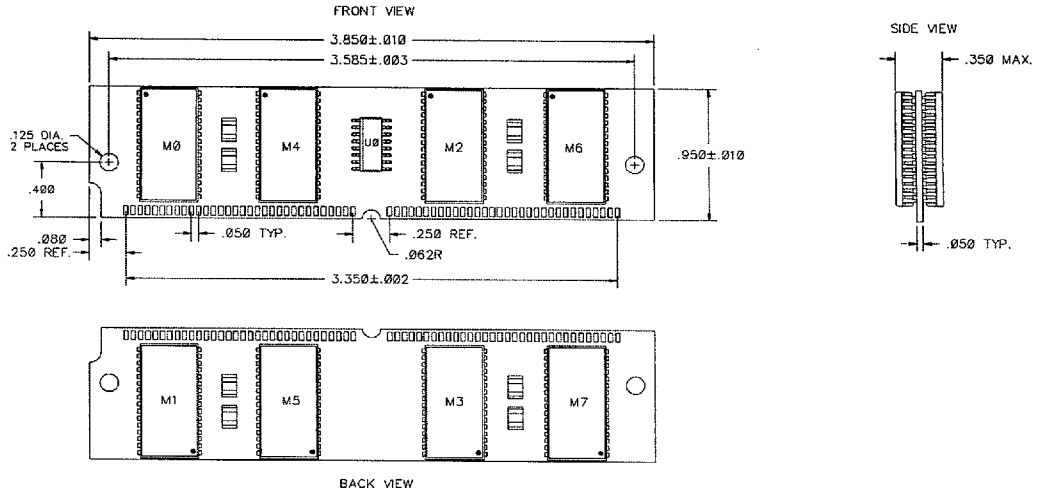


ADVANCED INFORMATION

ORDERING INFORMATION



MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove, California 92841-1428
(714) 898-0007 ◆ (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com