Features

- **0.6 µm Drawn Gate Length (0.5 µm Leff) Sea-of-Gates Architecture with Triple-level Metal**
- **5.0V, 3.3V and 2.0V Operation including Mixed Voltages**
- **On-chip Phase Locked Loop Available to Synthesize Frequencies up to 150 MHz and Manage Chip-to-Chip Clock Skew**
- **Compiled (Gate Level) and Embedded (Custom) SRAMs, ROM, and CAMs Available**
- **PCI, SCSI and High Speed (250 MHz) Buffers Available**
- **Easy Alternative Sourcing of Existing ASIC, FPGA and PLD Designs**
- **Design-for-Test Methods, Including JTAG, Serial and Boundary Scan and ATPG**
- **High Output Drive Capability: Up to 48 mA with Slew Rate Control**

Description

Atmel's next generation ATL60 Series CMOS ASICs are fabricated using a 0.6µm drawn gate, oxide isolated, triple-level metal process. Extensive cell libraries are available and support the major CAD software tools. As with all Atmel ASIC families, customer involvement and satisfaction is integral to all steps of the design flow. A variety of Design for Testability techniques are supported by the libraries, and a wide range of packaging options are available. The ATLS version utilizes a fine pitch staggered row on bond pads to achieve the smallest die size possible for a given pad count. The ATLS60 is only available in a limited number of PQFP packages.

Table 1. ATL60 Array Organization

Device Number	Raw Gates	Routable Gates	Max Pin Count	Max I/O Pins	Gate[1] Speed
ATL60/4	4,000	3,000	44	36	200 ps
ATL60/15	15,000	10,000	68	60	200 ps
ATL60/25	25,000	16,900	84	76	200 ps
ATL60/40	38,000	25,400	100	92	200 ps
ATL60/60	58,000	34,600	120	112	200 ps
ATL60/85	86,000	51,900	144	136	200 ps
ATL60/110	110,000	65,900	160	152	200 ps
ATL60/150	149,000	89,300	184	176	200 ps
ATL60/200	195,000	116,900	208	200	200 ps
ATL60/235	232,000	139,500	226	218	200 ps
ATL60/300	301,000	181,000	256	248	200 ps
ATL60/435	430,000	260,000	304	296	200 ps
ATL60/550	545,000	288,000	340	332	200 ps
ATL60/700	693,000	363,000	380	372	200 ps
ATL60/870	870,000	456,000	424	416	200 ps
ATL60/1100	1,119,000	590,000	480	472	200 ps

Note: 1. Nominal two input NAND gate with a fanout of 2 at 5.0 volts

ASIC

ATL 60 and ATLS60 Series

Rev. 0388D–ASIC–07/02

ATLS60 Array Organization

Device Number	Raw Gates	Routable Gates	Max Pin Count	Max I/O Pins	Gate[1] Speed
ATLS60/80	12,500	8,000	80	72	200 ps
ATLS60/100	20,400	13,000	100	92	200 ps
ATLS60/120	30,200	17,500	120	112	200 ps
ATLS60/144	44,600	26,000	144	136	200 ps
ATLS60/160	55,300	32,500	160	152	200 ps
ATLS60/208	96,500	57,000	208	200	200 ps
ATLS60/225	113,500	67,500	225	217	200 ps
ATLS60/256	148,200	88,000	256	248	200 ps

Note: 1. Nominal two-input NAND gate with a fanout of 2 at 5.0 volts

Design

Design Systems Supported

Atmel supports the major software systems for design with complete macro cell libraries, as well as utilities for checking the netlist and accurate pre-route delay simulations.

Table 2. Design Systems Supported

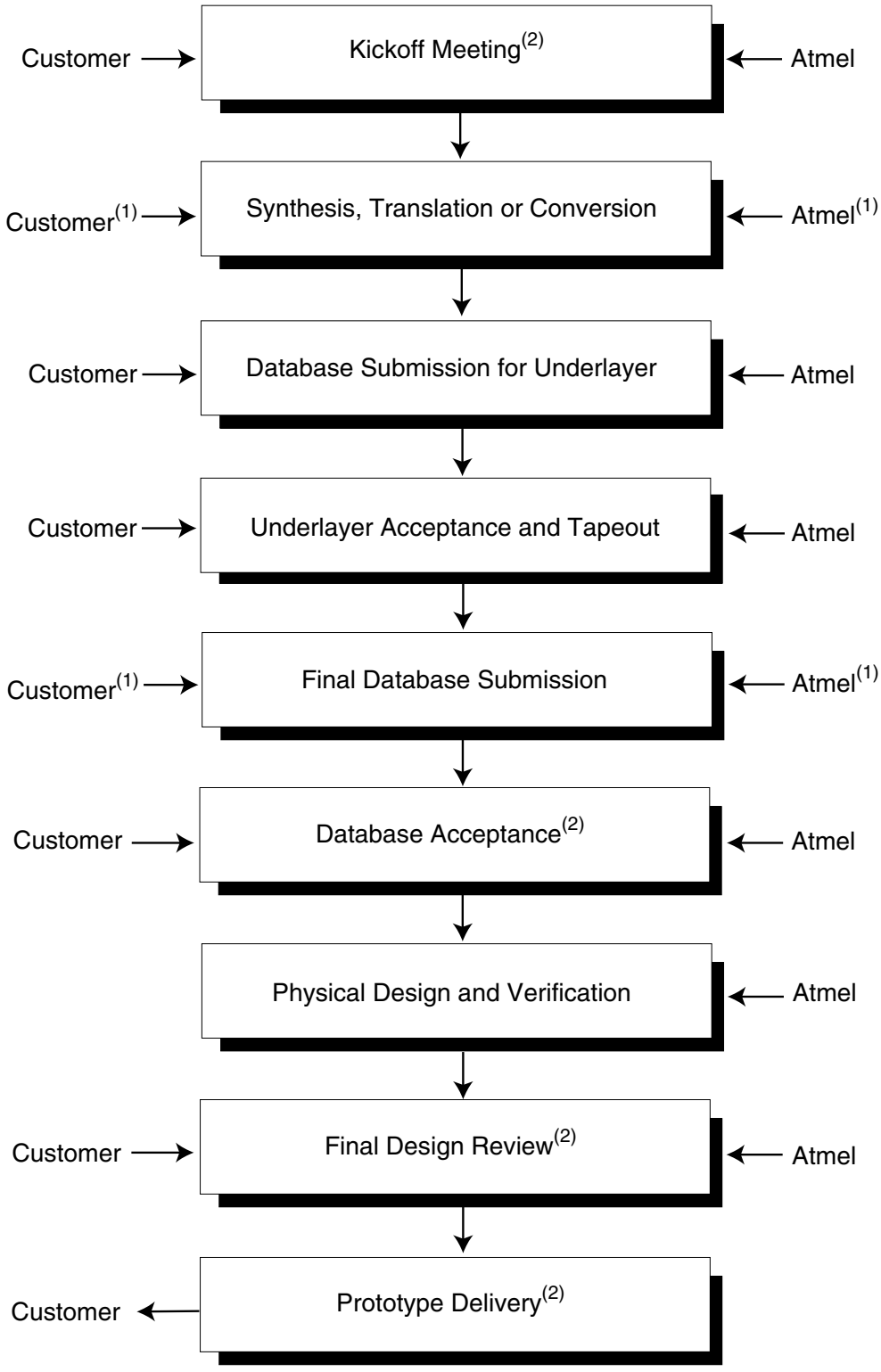
System	Tools	Version
Cadence® Design Systems, Inc.	Opus™ – Schematic and Layout NC Verilog™ – Verilog Simulator Pearl™ – Static Path Verilog-XL™ – Verilog Simulator BuildGates™ – Synthesis (Ambit)	4.46 3.3-s008 4.3-s095 3.3-s006 4.0-p003
Mentor Graphics®	ModelSim® – Verilog and VHDL (VITAL) Simulator Leonardo Spectrum™ – Logic Synthesis	5.5e 2001.1d
Synopsys™	Design Compiler™ – Synthesis DFT Compiler – 1-Pass Test Synthesis BSD Compiler – Boundary Scan Synthesis TetraMax® – Automatic Test Pattern Generation PrimeTime™ – Static Path VCS™ – Verilog Simulator Floorplan Manager™	01.01-SP1 01.08-SP1 01.08-SP1 01.08 01.08-SP1 5.2 01.08-SP1
Novas Software, Inc.	Debussy®	5.1
Silicon Perspective™	First Encounter®	v2001.2.3

Design Flow

Atmel provides three methods for implementing an ASIC design while maintaining the same basic design flow for each method. This flow involves both the customer and Atmel at all critical review and acceptance steps, as shown on the following page. Database Acceptance occurs when Atmel receives and accepts the complete design database.

Upon completion of this critical step, Atmel performs physical place-and-route. Functional and timing simulations are performed, based on the physical design, including the generation of a back annotation report to provide the customer with the most accurate timing information available. Final Design Review is the last step of the design flow prior to generation of masks. After this acceptance step is completed, masks are generated and released, and prototype parts in ceramic packages are delivered.

ASIC Design Flow



Notes: 1) Performed by the customer or optionally by Atmel
2) ISO 9001/QS9000 Milestone

Rev.2.3-04/02

Pin Definition Requirements

Within the Physical Design step (i.e., layout), certain restrictions apply during pin definition. The corner pins on each die are reserved and programmable for power and ground only. All other buffer pins are fully programmable as input, output, bidirectional, clock-into-array, power, or ground.

Design Options

Logic Synthesis

Atmel can accept Register Transfer Level (RTL) designs for VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL format. Atmel fully supports Synopsys for VHDL simulation as well as synthesis. VHDL or Verilog-HDL is Atmel's preferred method of performing an ASIC design.

ASIC Design Translation

Atmel has successfully translated dozens of existing designs from most major ASIC vendors into our ASICs. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors into our ASICs. There are four primary reasons to convert from an FPGA/PLD to an ASIC. Conversion of high-volume devices (over 10,000 units) for a single or combined design is cost effective. Performance can often be optimized for speed or power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, an ASIC may provide a lower cost answer for long-term volume production.

ATL60 Series Cell Library

Atmel's ATL60 Series ASICs make use of an extensive library of cell structures, including logic cells, buffers and inverters, multiplexers, decoders and I/O options. Soft macros are also available.

The ATL60 Series PLL operates at frequencies of up to 150 MHz with minimal phase error and jitter, making it ideal for frequency synthesis of high-speed on-chip clocks and chip-to-chip synchronization. Output buffers are programmable to meet the voltage and current requirements of both PCI and SCSI.

These cells are characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test arrays. Characterization is performed over the military temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Table 3. Cell Index

Signal Name	Description	Site Count[1]
ADD3X	One-bit full adder with buffered outputs	10
AND2	2-input AND	2
AND2H	2-input AND – High-drive	3
AND3	3-input AND	3
AND3H	3-input AND – High-drive	4
AND4	4-input AND	3
AND4H	4-input AND – High-drive	4
AND5	5-input AND	5
AOI22	2-input AND into 2-input NOR	2
AOI22H	2-input AND into 2-input NOR – High-drive	4
AOI222	Two 2-input ANDs into 2-input NOR	4
AOI222H	Two 2-input ANDs into 2-input NOR – High-drive	8
AOI2223	Three 2-input ANDs into 3-input NOR	4
AOI2223H	Three 2-input ANDs into 3-input NOR – High-drive	7
AOI23	2-input AND into 3-input NOR	2
BUF1	1x Buffer	2
BUF2	2x Buffer	2
BUF2T	2x Tristate Bus Driver with Active-high Enable	4
BUF2Z	2x Tristate Bus Driver with Active-low Enable	4
BUF3	3x Buffer	3
BUF4	4x Buffer	3
BUF8	8x Buffer	5
BUF12	12x Buffer	8
BUF16	16x Buffer	10
CLA7X	7-input Carry Lookahead	5
DEC4	2:4 Decoder	7
DEC4N	2:4 Decoder with Active-low Enable	9

Table 3. Cell Index (Continued)

Signal Name	Description	Site Count[1]
DEC8N	3:8 Decoder with Active-low Enable	24
DFF	D Flip-flop	8
DFFBCPX	D Flip-flop with Asynchronous Clear and Preset with Complementary Outputs	16
DFFBSRX	D Flip-flop with Asynchronous Set and Reset with Complementary Outputs	16
DFFC	D Flip-flop with Asynchronous Clear	9
DFFR	D Flip-flop with Asynchronous Reset	11
DFFS	D Flip-flop with Asynchronous Set	9
DFFSR	D Flip-flop with Asynchronous Set and Reset	12
DLY1500	Delay Buffer 1.5 ns	6
DLY2000	Delay Buffer 2.1 ns	10
DLY6000	Delay Buffer 6.0 ns	24
DSS	Set Scan Flip-flop	11
DSSBCPY	Set Scan Flip-flop with Clear and Preset	16
DSSBR	Set Scan Flip-flop with Reset	13
DSSBS	Set Scan Flip-flop with Set	13
DSSR	Set Scan D Flip-flop with Reset	13
DSSS	Set Scan D Flip-flop with Set	12
DSSSR	Set Scan D Flip-flop with Set and Reset	14
INV1	1x Inverter	1
INV1D	Dual 1x Inverters	2
INV1Q	Quad 1x Inverters	4
INV1TQ	Quad Tristate Inverter	7
INV2	2x Inverter	2
INV2T	2x Tristate Inverter with Active-high Enable	3
INv3h	3x Inverter	2
INV4	4x Inverter	2
INV8	8x Inverter	4
INV10	10x Inverter	8
JKF	JK Flip-flop	10
JKFBCPX	Clear Preset JK Flip-flop with Asynchronous Clear and Preset and Complementary Outputs	16
JKFC	JK Flip-flop with Asynchronous Clear	12
LAT	LATCH	4
LATBG	LATCH with Complementary Outputs and Inverted Gate Signal	6
LATBH	LATCH with High-drive Complementary Outputs	7

Table 3. Cell Index (Continued)

Signal Name	Description	Site Count[1]
LATR	LATCH with Reset	4
LATS	LATCH with Set	6
LATSR	LATCH with Set and Reset	8
LSCC	Voltage Level Shifter	4
LSISO	Voltage Level Shifter with Power Supply Isolation Function	12
MUX2	2:1 MUX	4
MUX2H	2:1 MUX – High-drive	5
MUX2I	2:1 MUX with Inverted Output	3
MUX2IH	2:1 MUX with Inverted Output – High-drive	4
MUX2N	2:1 MUX with Active-low Enable	4
MUX2NQ	Quad 2:1 MUX with Active-low Enable	18
MUX2Q	Quad 2:1 MUX	14
MUX3I	3:1 MUX with Inverted Output	6
MUX3IH	3:1 MUX with Inverted Output – High-drive	8
MUX4	4:1 MUX	9
MUX4X	4:1 MUX with Transmission Gate Data Inputs	10
MUX4XH	4:1 MUX with Transmission Gate Data Inputs – High-drive	10
MUX5H	5:1 MUX – High-drive	14
MUX8	8:1 MUX	18
MUX8N	8:1 MUX with Active-low Enable	20
MUX8XH	8:1 MUX with Transmission Gate Data Inputs – High-drive	18
NAN2	2-input NAND	2
NAN2D	Dual 2-input NAND	3
NAN2H	2-input NAND – High-drive	2
NAN3	3-input NAND	2
NAN3H	3-input NAND – High-drive	3
NAN4	4-input NAND	3
NAN4H	4-input NAND – High-drive	4
NAN5	5-input NAND	5
NAN5H	5-input NAND – High-drive	6
NAN6	6-input NAND	6
NAN6H	6-input NAND – High-drive	7
NAN8	8-input NAND	7
NAN8H	8-input NAND – High-drive	7
NOR2	2-input NOR	2
NOR2D	Dual 2-input NOR	3

Table 3. Cell Index (Continued)

Signal Name	Description	Site Count[1]
NOR2H	2-input NOR – High-drive	2
NOR3	3-input NOR	2
NOR3H	3-input NOR – High-drive	3
NOR4	4-input NOR	3
NOR4H	4-input NOR – High-drive	4
NOR5	5-input NOR	5
NOR8	8-input NOR	7
OAI22	2-input OR into 2-input NAND	2
OIA22H	2-input OR into 3-input NAND – High-drive	4
OAI222	Two 2-input ORs into 2-input NAND	2
OAI222H	Two 2-input ORs into 2-input NAND – High-drive	4
OAI22224	Four 2-input ORs into 4-input NAND	6
OAI23	2-input OR into 3-input NAND	3
ORR2	2-input OR	2
ORR2H	2-input OR – High-drive	3
ORR3	3-input OR	3
ORR3H	3-input OR – High-drive	4
ORR4	4-input OR	3
ORR4H	4-input OR – High-drive	4
ORR5	5-input OR	5
XNR2	2-input Exclusive NOR	4
XNR2H	2-input Exclusive NOR – High-drive	4
XOR2	2-input Exclusive OR	4
XOR2H	2-input Exclusive OR – High-drive	4

Note: 1. A single ATL60 routing site contains four transistors, two N-channel and two P-channel, aligned in columns. The number of sites used per gate varies according to the specific isolation and power requirements. Percent utilization varies from 50% to 70%, with more accurate utilization figures generated by DoubleCheck™, the netlist checker.

Table 4. CMOS Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5V Minimum	1.5V Maximum	V_{DD}/2 Typical
TTL	2.0V Minimum	0.8V Maximum	1.4V Typical

Table 5. Absolute Maximum Ratings[1]

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–2.0V to +7.0V[2]
Maximum Operating Voltage	6.0V

Notes: 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Minimum voltage is –0.6V DC, which may undershoot to –2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{DD} + 0.75V dc, which may overshoot to +7.0V for pulses of less than 20 ns.

Table 6. 5.0-volt DC Characteristics

Applicable over recommended operating range from T_a = –55°C to +125°C, V_{DD} = 4.5V to 5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 5.5V			10	µA
I_{IL}	Input Leakage Low (no pull-up) 40K pull-up	$V_{IN} = V_{SS}$, V_{DD} = 5.5V $V_{IN} = V_{SS}$, V_{DD} = 5.5V	–10 –100		–15	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 5.5V	–10		10	µA
I_{OS}	Output Short Circuit Current (3x buffer)[1]	V_{DD} = 5.5V, $V_{OUT} = V_{DD}$ V_{DD} = 5.5V, $V_{OUT} = V_{SS}$		66 –66		mA mA
V_{IL}	TTL Input Low Voltage				0.8	V
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	TTL Switching Threshold CMOS Switching Threshold	V_{DD} = 5.0V, 25°C V_{DD} = 5.0V, 25°C		1.4 2.4		V V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2 mA I_{OL} per stage	I_{OL} = as rated V_{DD} = 4.5V		0.2	0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with –2 mA I_{OH} per stage	I_{OH} = as rated V_{DD} = 4.5V	0.7 x V_{DD}	4.2		V

Note: 1. This is the specification for the 3x buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

Table 7. 3.3-volt DC Characteristics

Applicable over recommended operating range from T_a = –55°C to +125°C, V_{DD} = 2.7V to 3.6V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 3.6V			5	µA
I_{IL}	Input Leakage Low (no pull-up) Max R pull-up (U31)	$V_{IN} = V_{SS}$, V_{DD} = 3.6V $V_{IN} = V_{SS}$, V_{DD} = 3.6V	–5 –25		 –3	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 3.6 V	–5		5	µA
I_{OS}	Output Short Circuit Current (8 x buffer)(1)	V_{DD} = 3.6 V, $V_{OUT} = V_{DD}$ V_{DD} = 3.6 V, $V_{OUT} = V_{SS}$		88 –88		mA mA
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	CMOS Switching Threshold	V_{DD} = 3.0V, 25°C		1.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 1 mA I_{OL} per stage.	I_{OL} = as rated V_{DD} = 2.7V			0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with –1 mA I_{OH} per stage.	I_{OH} = as rated V_{DD} = 2.7V	0.7 x V_{DD}	4.2		V

Table 8. 2.0-volt DC Characteristics

Applicable over recommended operating range from T_a = 0°C to +70°C, V_{DD} = 1.8V to 2.2V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 2.2V			5	µA
I_{IL}	Input Leakage Low (no pull-up) Max R pull-up (U31)	$V_{IN} = V_{SS}$, V_{DD} = 2.2V $V_{IN} = V_{SS}$, V_{DD} = 2.2V	–5 –15		 –2	µA µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 2.2V	–5		5	µA
I_{OS}	Output Short Circuit Current (8 x buffer)(1)	V_{DD} = 2.2V, $V_{OUT} = V_{DD}$ V_{DD} = 2.2V, $V_{OUT} = V_{SS}$		40 –40		mA mA
V_{IL}	CMOS Input Low Voltage				0.2 x V_{DD}	V
V_{IH}	CMOS Input High Voltage		0.8 x V_{DD}			V
V_T	CMOS Switching Threshold			0.5xV_{DD}		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 0.5 mA I_{OL} per stage.	I_{OL} as rated V_{DD} = 1.8V			0.2 x V_{DD}	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with –0.5 mA I_{OH} per stage.	I_{OH} as rated V_{DD} = 1.8V	0.8 x V_{DD}			V

Note: This is the specification for the 8x buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

Table 9. I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance, Input Buffer (die)	5.0V, 3.3V, 2.0V		2.4		pF
C_{OUT}	Capacitance, Output Buffer (die)	5.0V, 3.3V, 2.0V		5.6		pF
$C_{I/O}$	Capacitance, Bidirectional	5.0V, 3.3V, 2.0V		6.6		pF
Schmitt Trigger						
V+	TTL Positive Threshold CMOS Positive Threshold	25°C, 5.0V 25°C, 5.0V		1.8 3.0	2.0 3.5	V V
V–	TTL Negative Threshold CMOS Negative Threshold	25°C, 5.0V 25°C, 5.0V	0.8 1.5	1.0 2.0		V V
ΔV	TTL Hysteresis CMOS Hysteresis	25°C, 5.0V 25°C, 5.0V		0.8 1.0		V V
V+	CMOS Positive Threshold	25°C, 3.3V		1.8	2.3	V
V-	CMOS Negative Threshold	25°C, 3.3V	1.0	1.3		V
ΔV	CMOS Hysteresis	25°C, 3.3V		0.5		V

I/O Buffers

- Programmable output drive
  2 to 24 mA IOL; –2 to –24 mA IOH at 5.0 volts
  1 to 12 mA IOL; –1 to –12 mA IOH at 3.3 volts
- Programmable slew rate control
- Built-in configurable test logic

Design for Testability

Atmel supports a wide range of Design for Testability techniques to improve the percentage of a design that can be fully tested. By achieving a high degree of testability, a designer can reduce design and prototype debug time, minimize production test time, and improve board- and system-level test and diagnostic capability.

Synopsys Test Compiler software is fully supported by Atmel. By using this system during design, the computer will create and add a set of scan chains to the design, and test vectors will be generated to provide greater than 95% fault coverage. This method requires only one or two added pins for Test Enable and Test Mode. This is the easiest and least expensive method of designing testability into an ASIC design.

Ad hoc means of increasing testability of an ASIC are also available. Partitioning, memory array isolation, and test point insertion are encouraged and supported by the ATL60 Series ASICs. Atmel also encourages the inclusion of Built-In Self-Test (BIST) techniques whenever possible. Each of these methods is discussed in detail in the Atmel *CMOS ASIC Design Manual.*

In addition to all of the above, the ATL60 Series ASICs also support the Joint Test Action Group (JTAG) boundary scan architecture and Test Access Port (TAP) requirements. The required soft and hard macros to implement IEEE 1149.1-compliant architecture are available in Atmel's cell library. Use of JTAG architecture requires an additional four to five pins for test mode, data, and clock signals.

Advanced Packaging

The ATL60 Series ASICs are offered in a wide variety of standard packages, including plastic and ceramic quad flatpacks, thin quad flatpacks, ceramic pin grid arrays and ball grid arrays. High-volume on-shore and off-shore contractors provide assembly and test for commercial product, with prototype capability in Colorado Springs.

Custom package designs are also available as required to meet a customer's specific needs and are supported through Atmel's package design center. When a standard package cannot meet a customer's need, a package can be designed to precisely fit the application and to maintain the performance obtained in silicon. Atmel has delivered custom-designed packages in a wide variety of configurations.

Table 10. Package Options (Partial List)

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
Power Quad	144, 160, 208, 240, 304
L/TQFP	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
PBGA	121, 169, 208, 217, 225, 240, 256, 272, 300, 304, 313, 316, 329, 352, 388, 420, 456
Super BGA	168, 204, 240, 256, 304, 352, 432, 560, 600
Low-profile Mini BGA	40, 48, 49, 56, 60, 64, 80, 81, 84, 96, 100, 108, 128, 132, 144, 160, 176, 192, 208, 224, 228
Chip-scale BGA	32, 36, 40, 48, 49, 56, 64, 81, 84, 100, 108, 121, 128, 144, 160, 169, 176, 192, 208, 224, 256, 288, 324
Flex-tape BGA	48, 49, 64, 80, 81, 84, 96, 100, 112, 132, 144, 156, 160, 180, 192, 196, 204, 208, 220, 225, 228, 256, 280
FCBGA*	416, 480, 564, 672, 788, 896, 960, 1032, 1152, 1157, 1292, 1357, 1413, 1500, 1517, 1557, 1677, 1728, 1932

Note: * These packages require a custom design substrate.

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