



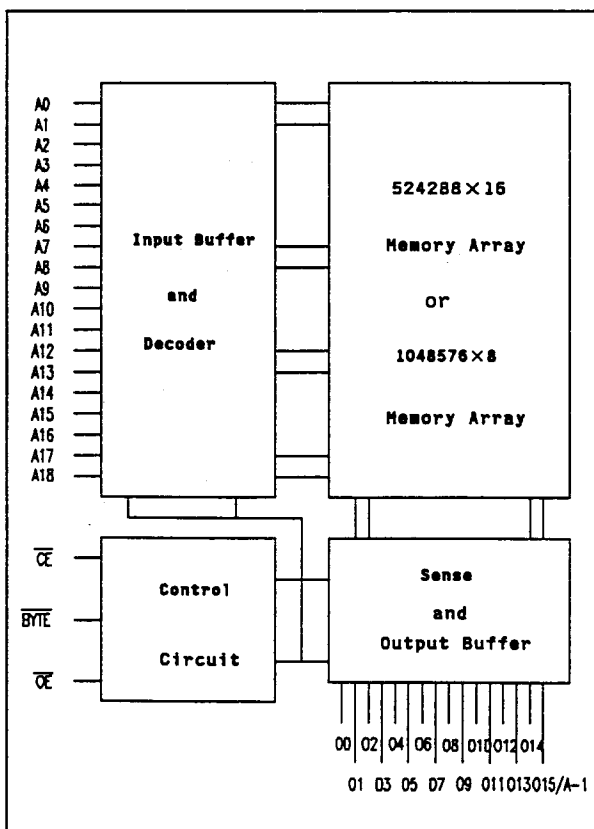
512K $\times$ 16 BITS/1024K $\times$ 8 BITS CMOS MASK ROM

W22C8192

FEATURES

- Low power consumption:
Active: 150mW (typ.)
Standby: 25 μ W (typ.)
- Access time: 120/150/200 nS (max.)
- Single +5V power supply
- Fully static operation
- Direct TTL compatible
- Programmable output enable ($\overline{OE}/\overline{OE}$) and chip enable ($\overline{CE}/\overline{CE}$)
- Automatic power-down ($\overline{CE}/\overline{CE}$)
- Three-state outputs
- Capability of battery buck up operation
- Available in 42 pin DIP

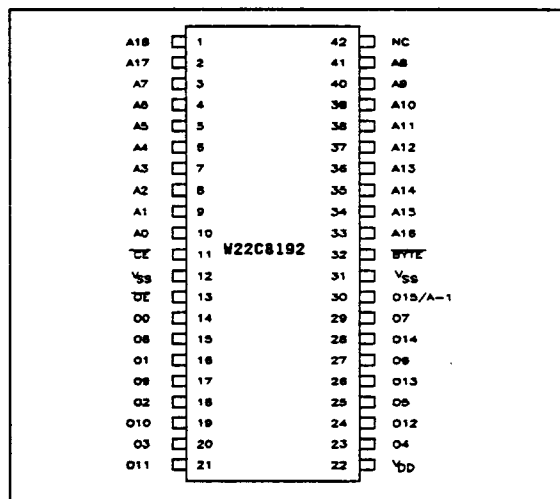
BLOCK DIAGRAM



GENERAL DESCRIPTION

The W22C8192 is a high speed, low power mask-programmable read-only memory organized as 524288 $\times$ 16 bits or 1048576 $\times$ 8 bits by typing the $\overline{BYTE}$ pin high or low and operates on a single 5-Volt power supply. The device is manufactured in WINBOND's high performance CMOS technology.

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
D0 - D15	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connection
O15/A-1	Output/LSB Address(byte)
$\overline{BYTE}$	Byte Selection

FEBRUARY 1992

DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Inputs or Outputs to V_{SS} Potential	-0.5 to $V_{DD}+0.5$	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-55 to +150	°C
Operating Temperature	0 to +70	°C

OPERATING CHARACTERISTICS

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to 70°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-	- 0.5	-	+ 0.8	V
Input High Voltage	V_{IH}	-	+ 2.2	-	$V_{DD} + 0.5$	V
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{DD}	- 10	-	+ 10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{DD} $\overline{CE} = V_{IH}$ or $CE = V_{IL}$ or $\overline{OE} = V_{IH}$ or $OE = V_{IL}$	- 10	-	+ 10	μA
Output Low Voltage	V_{OL}	$I_{OL} = +2.0\text{mA}$	-	-	+ 0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -1.0\text{mA}$	+ 2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$ or $CE = V_{IH}$, $OE = V_{IH}$ $I_{OUT} = 0\text{mA}$, CYCLE = MIN	-	-	+ 50	mA
Standby Power Supply Current	I_{SB}	$\overline{CE} = V_{IH}$ or $CE = V_{IL}$	-	-	+ 1	mA
		$\overline{CE} \geq V_{DD} - 0.2V$ $CE \leq 0.2V$	-	-	+50	μA

Note: Typical characteristics are at $V_{DD}=5V$, $T_a=25^\circ\text{C}$.



W22C8192

CAPACITANCE

($V_{DD}=5V$, $T_a=25^{\circ}C$, $f=1MHz$)

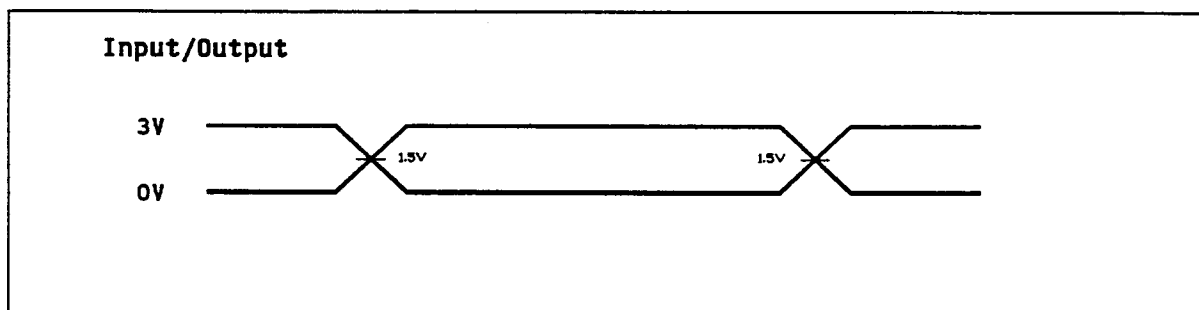
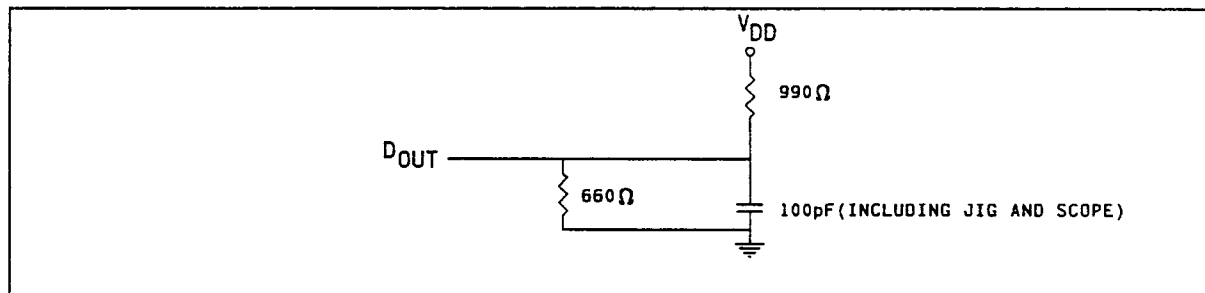
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	$V_{IN}=0V$	10	pF
Output Capacitance	C_{OUT}	$V_{OUT}=0V$	15	pF

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5nS
Input and Output Timing Reference Level	1.5V
Output Load	$C_L=100pF$, $I_{OH}/I_{OL}=-1mA/2.0mA$

AC TEST LOADS AND WAVEFORMS





W22C8192

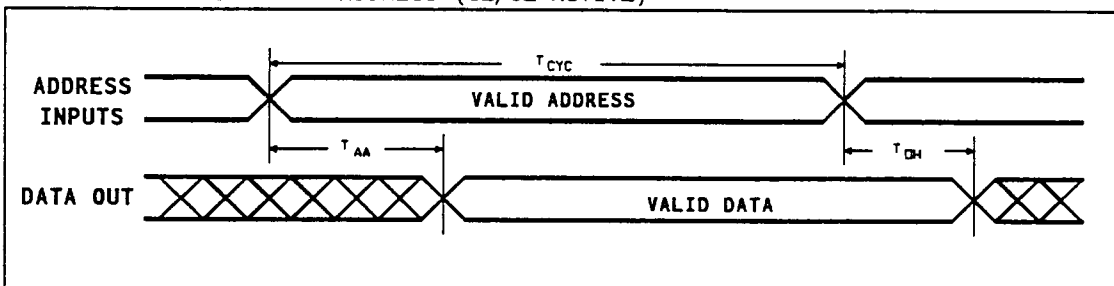
AC CHARACTERISTICS

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $70^\circ C$)

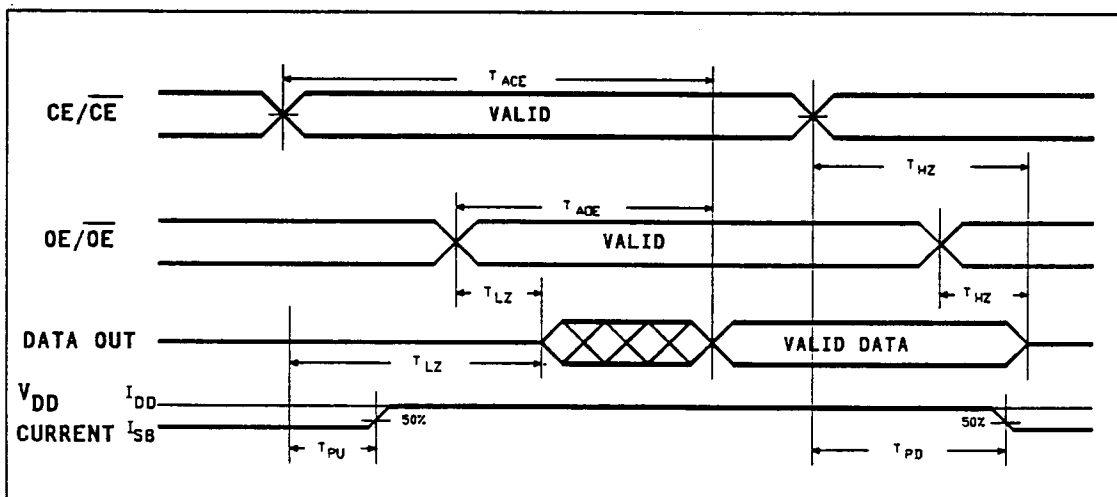
PARAMETER	SYMBOL	W22C8192-12		W22C8192-15		W22C8192-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Cycle Time	T_{CYC}	120	-	150	-	200	-	nS
Address Access Time	T_{AA}	-	120	-	150	-	200	nS
Chip Enable Access Time	T_{ACE}	-	120	-	150	-	200	nS
Output Enable Access Time	T_{AOE}	-	50	-	60	-	80	nS
Output Hold Time	T_{OH}	10	-	10	-	10	-	nS
Output Low Z Delay	T_{LZ}	10	-	10	-	10	-	nS
Output High Z Delay	T_{HZ}	-	50	-	60	-	80	nS
Power-Up Time	T_{PU}	0	-	0	-	0	-	nS
Power-Down Time	T_{PD}	-	50	-	60	-	80	nS

TIMING WAVEFORM

PROPAGATION DELAY FROM ADDRESS (CE/OE=ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE OR OUTPUT ENABLE (ADDRESS VALID)





W22C8192

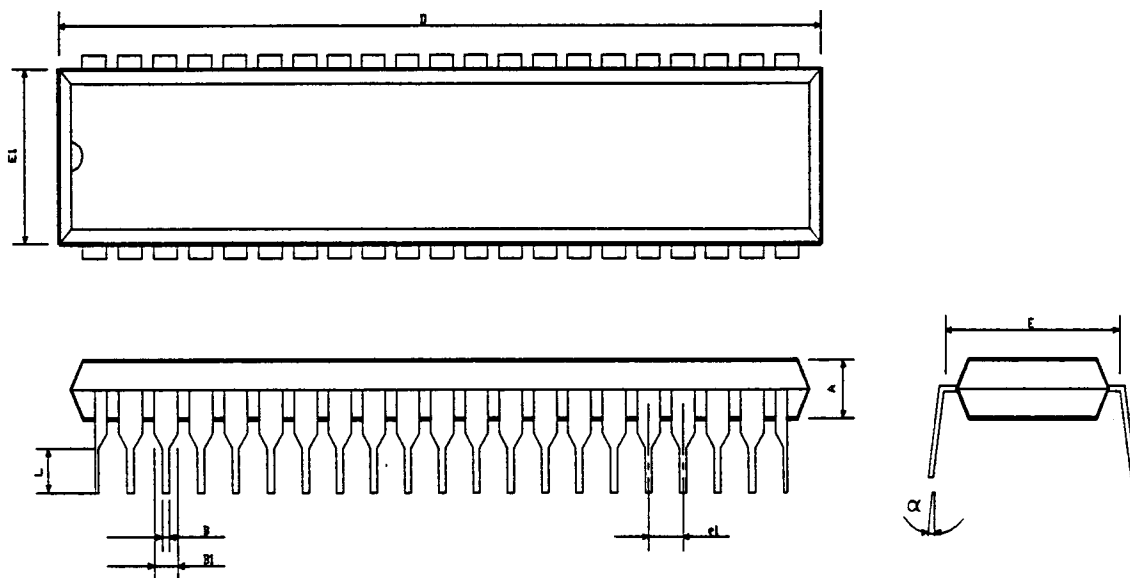
ORDERING INFORMATION

Part No.	Access Time (nS)	Operating Current Max. (mA)	Standby Current Max. (μ A)	Package	Remark
W22C8192-12	120	50	50	600mil DIP	
W22C8192-15	150	50	50	600mil DIP	
W22C8192-20	200	50	50	600mil DIP	

Notes:

1. Winbond Electronics Corp. reserves the right to make design improvements and other changes to its products without notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products used in applications where personal injury might result from device failure.

PACKAGE DIMENSION **42 LEAD P-DIP**



Symbol	Dimensions in inch	Dimensions in mm
A	0.155 ± 0.005	3.937 ± 0.127
B	0.018 ± 0.004	0.457 ± 0.102
B1	0.050 ± 0.004	1.270 ± 0.102
D	2.060 ± 0.010	52.32 ± 0.254
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.550 ± 0.010	13.970 ± 0.254
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.135 ± 0.010	3.429 ± 0.254
α	$0^\circ \sim 15^\circ$	$0^\circ \sim 15^\circ$



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Note: All data and specifications are subject to change without notice