CDI CALIFORNIA DEVICES INC.

DLM SERIES HCMOS Gate Arrays

April 1985

PRODUCT FEATURES

- High performance 3 μm silicon gate HCMOS technology.
- From 210 to 10,152 equivalent 2-input gates.
- Double layer metal used for global and intracell routing.
- Wide operating supply range (3V to 5.5V) over the full military temperature range (−55°C to 125°C).
- Channelless core architecture for enhanced performance.
- Die sizes similar to conventional standard cells.
- Typical delays of 2 ns for 2 input NAND gates with FO = 2 plus interconnect capacitance.
- Flexible I/O programmability compatible with TTL or MOS logic families.
- State-of-the-art electrostatic and latch-up protection on all pins.
- Bipolar-like output drive capabilities (8/−10 mA per driver).
- Separate power buses minimize power pin requirements and maximize noise immunity.
- Extensive macrocell library fully compatible with CDI channelless standard cells.
- Fully automated development system supporting hierarchical methodologies for electrical and physical design.
- Design automation software for workstation and mainframe based CAD systems.

DESCRIPTION

The DLM Series of gate arrays is a high performance family of HCMOS devices ranging in complexity from 210 to 10,152 equivalent 2-input gates manufactured with an advanced oxide-isolated, 3 micron silicon gate process using two layers of metallization.

As a fourth generation concept in gate array architecture, the DLM design significantly improves silicon utilization while enhancing routeability. The main feature is the absence of pre-defined core area for wiring channels. This channelless architecture allows the interconnection paths for global routing to be merged with the active transistor area, significantly reducing wiring capacitance while allowing large transistor sizes for increased performance. This technique allows high component utilization, and yields die sizes comparable to conventional standard cells.

CMOS gate arrays allow quick, low cost, and low risk integration of logic systems. The primary benefits of this integration include improved reliability, reduced system costs, and proprietary protection.

DLM SERIES FAMILY ORGANIZATION

Part Number	Available Gates	Number of Cells	Maximum Pads	Maximum Inputs*	Maximum Outputs
DLM 200	210	140	30	30	22
DLM 400	432	288	40	40	32
DLM 700	720	480	48	48	40
DLM 900	990	660	54	54	46
DLM 1200	1224	816	60	60	52
DLM 1600	1680	1120	68	68	60
DLM 2100	2112	1408	76	76	66
DLM 2800	2850	1900	86	86	76
DLM 3600	3600	2400	96	96	86
DLM 4600	4608	3072	108	108	100
DLM 7200	7200	4800	132	132	124
DLM 10000	10152	6768	156	156	148

*Power pins are included

BASIC CELL

The core logic area consists of building blocks, or basic cells, which are repeated in horizontal and vertical directions. Each basic cell contains three uncommitted transistor pairs (1.5 equivalent gates) and interconnect paths for inter and intracell routing including internal power supply buses.

An equivalent gate is defined as two pairs of transistors with which a two input NAND or NOR logic gate can be made. Array complexity is measured in equivalent gates. For example, the DLM 7200 has 7200 available equivalent gates, that is 28,800 core transistors, not including those in the periphery.

The basic cell also contains numerous interconnect paths through the cell. By programming the two metal levels and the connecting via mask, the uncommitted transistors in the array are patterned to implement logic functions, called macros. In this sea-of-gates approach, layout freedom is assured because of the flexibility allowed in the basic cell for programming either logic gates, interconnect, or both.

Extremely high cell utilization (typically over 90%) is possible on the DLM arrays due to the freedom of transistor and interconnect assignment. Cell utilization refers to the percentage ratio of programmed basic cells to those available.

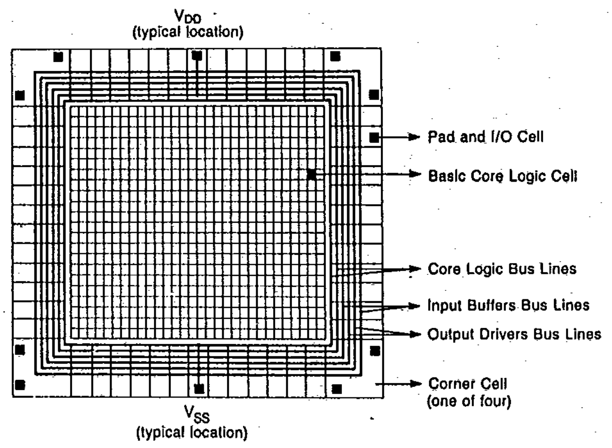

Figure 1. DLM Series Array Structure

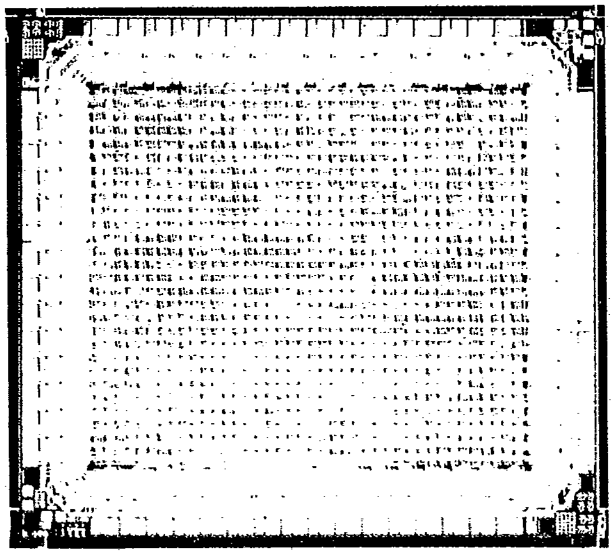

Figure 2. Personalized Channelless Gate Array

I/O CELL

Each available pad, except for eight corner pads, can be programmed to perform the following input-output functions.

Input: CMOS or TTL compatible receivers with or without pull-up or pull-down.

Output: TTL and CMOS compatible levels
- Three driver sizes per pad: D_3, D_2, D_1
- Open drain, current sink or source
- Three-state drivers with non-overlapping switching characteristics to minimize current spikes

I/O: Bidirectional buffers for CMOS or TTL system interface

Analog Switch: Two pads connected by a transmission gate (R_{ON} = 100 ohms at 85°C, 5V)

Power Supply: V_{SS} or V_{DD}

Special Functions: There are eight corner pads in each array that can be used as inputs or power supply pins. Two of these eight pads include unique testability features that facilitate testing the final devices, as described later on. Other special functions, such as oscillator pins, clock input, Schmitt trigger input, current mirror or voltage reference inputs can also be configured using special corner circuitry or core area gates.

POWER SUPPLY BUSES

Special attention is given in the periphery to the distribution of power supply buses. Wide metal bus lines are provided for high current demands of the high drive output buffers, input TTL level shifters, and core logic.

To improve noise immunity, the V_{SS} and V_{DD} power input pads each connect to three bus rings (see Figure 1). One ring pair supplies the internal array core, another pair the output buffer transistors, and the third ring powers the input TTL buffers. Noise generated from the low impedance output buffers is thus isolated from the core logic and the remaining circuitry. The core power buses are also connected through the array core to lower supply source impedance for the internal gates.

The peripheral cells are designed so that any pad may be used as a power pin. Optimum placement, if only two pads are used for V_{SS} and V_{DD}, is the center of the chip on opposing sides, as shown in Figure 1. As in most commercially available packages, this allows the lowest resistance and inductive effects because it uses the centermost package pins. As more current is required, additional power pads may be added. Each supply pad is limited to approximately 50 mA.

TESTABILITY FEATURES

Special testability circuitry is available on-chip to facilitate production testing. Two corner pads are designed as three-state inputs. They may be used as ordinary input pins, but when brought to a negative seven volts referenced to V_{SS}, they activate a third logic state. This state can be used to define test signals, such as 'Reset' and 'Test Enable'.

Reset allows the internal storage elements to be readily initialized, minimizing the need for sequencing the device through numerous logic patterns in order to establish the proper starting state for functional testing. Test Enable allows, for example, each output to be activated in sequence, so that V_{OL}, V_{OH}, leakage, noise immunity and other parametric tests can be made, without having to search the test pattern for vectors that force the output buffers to the proper state. Thus, testing time for parametric measurements is dramatically reduced.

Other in-circuit structures for improving testability and system diagnostics, such as LSSD (Level Sensitive Scan Design) and Scan testing techniques, can be implemented in the core logic with special macros.

The DLM family is fully supported by an automated design system for both workstation and mainframe based CAD systems. The basic design flow is outlined in Figure 3. This automated design system supports schematic capture, logic simulation, timing analysis, fault simulation and automatic placement and routing. This permits the user to interface at a variety of data transfer levels. CDI provides designers with the training and software tools necessary to define and analyze semicustom designs to ensure accurate implementation in silicon.

WISE I

The WISE I (Workstation Interface Software Engineering) Package allows users of commercially available engineering workstations to design and evaluate the performance characteristics of logic designs to be implemented on a DLM array. This software package provides designers with the ability to capture schematics using CDI's extensive macro library, simulate the logic based on actual device performance and statistical interconnect information, and verify the design integrity using electrical rule checking routines. This comprehensive package provides the user with a powerful tool that allows control of the design cycle and ensures that the final devices will meet the system performance requirements.

CDI-User Interface

CDI offers a variety of interface levels for customers designing with the DLM array family. Each interface level requires the user to provide a given set of information to CDI which is needed to manufacture the part to specification. The quality of the information that the customer supplies will affect the turnaround time for prototypes, and the non-recurring engineering charges.

Level I interface is a turnkey approach to application-specific integrated circuits. The customer submits a schematic diagram describing the circuit in terms of standard MSI and SSI functions along with input patterns to be used to simulate and test the device, and specifications describing the electrical characteristics of the circuit. CDI will implement the design using the DLM library set and simulate the logic using the input patterns provided. The converted schematic and simulation results are then submitted for customer approval before layout of the circuit begins.

Level II interface allows the designer to become more closely involved in the circuit design process. At this interface level the customer submits a verified design file which allows CDI to layout and manufacture the array directly from the customer's inputs. This verified design file is based upon a simulated netlist which meets CDI's design requirements as defined in the WISE I software package. These design requirements are coded into software routines to provide automated error checking for the designer. This level of interface provides the designer with faster prototype turnaround time and more control over the performance of the final design.

Level IA interface provides designers with an intermediate handoff point between full Level I and Level II designs. For designers doing schematic capture and functional simulation only, CDI's Electronic Data Book Software provides these capabilities on most commercially available engineering workstation. Level IA requires that CDI complete the simulation process by performing load dependent timing simulation to verify the design file.

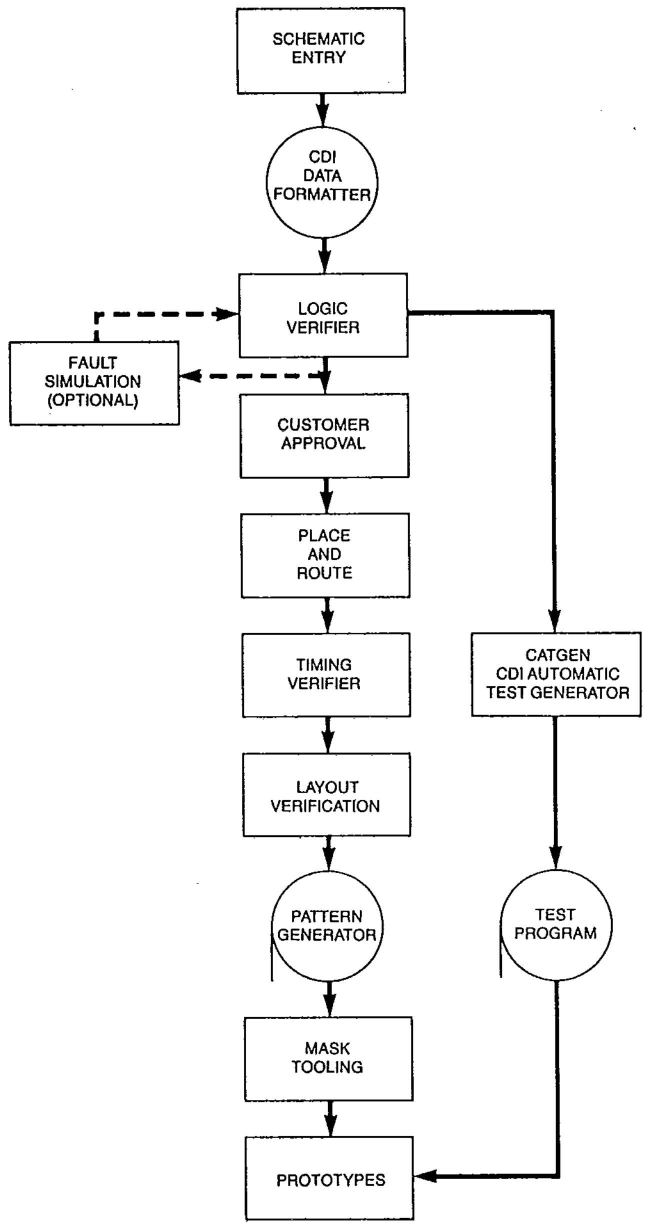

Figure 3. CDI Design Flow

MACROCELLS

The unique metallization patterns that convert uncommitted basic cells into logic functions are called macrocells. These macrocells implement the basic building blocks, shown in Table 1.

Complete characterization exists for the macrocells, including schematic symbol, netlist, logic simulation model, timing performance, and layout attributes.

Macrofunctions, also called software macros, are composed of macrocells and used to implement more complex functions like counters, registers, adders, etc. They allow the designer to describe the system logic in a hierarchical fashion, and their performance is determined by that of the macrocell components.

DLM SERIES OPERATING CHARACTERISTICS[1]

ABSOLUTE MAXIMUM RATINGS[2]

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 7	V
$V_{I/O}$	Voltage on Any Pin	− 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
	Storage Temperature Range:		
T_{STG}	Ceramic	− 65 to + 150	°C
T_{STG}	Plastic	− 40 to + 125	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply Voltage	5 ± 10%	V
	Extended Voltage Range*	+ 2 to + 6	V
	Operating Temperature Range:		
T_A	Commercial	0 to + 70	°C
T_A	Industrial	− 40 to + 85	°C
T_A	Military	− 55 to + 125	°C

*Consult factory for operation at voltage extremes.

GENERAL OPERATING CHARACTERISTICS[1, 4]

Symbol	Parameter	Condition	Limits[3] TLOW Min	TLOW Max	+25°C Min	+25°C Typ	+25°C Max	THIGH Min	THIGH Max	Unit
I_{IN}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{DD}		± 0.1		± 0.001			± 1.0	μA
I_{OZ}	Three-State Output Leakage	$V_{IN} = V_{SS}$ or V_{DD}		± 1.0		± 0.001			± 10	μA
C_{IN}	Input Capacitance	Any Input				5				pF
I_{KLU}	Latch up Protection	$V_O < V_{SS}$, $V_O > V_{DD}$				± 100				mA
V_{ESD}	Electrostatic Discharge Protection	C = 100 pF, R = 1500Ω				± 1500				V
I_{DD}	Quiescent Device Current	$V_{IN} = V_{SS}$ or V_{DD}				0.002				μA/gate

DC CHARACTERISTICS - TTL INTERFACE[1, 4]

Symbol	Parameter	Buffer[5] Type	Condition[6]	Limits Min	Limits Typ	Limits Max	Unit
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IH}	High-Level Input Voltage			2.0			V
V_{OL}	Low-Level Output Voltage	D3 D2 D1	I_{OL} = 8.0 mA I_{OL} = 6.4 mA I_{OL} = 3.2 mA			0.4 0.4 0.4	V
V_{OH}	High-Level Output Voltage	D3 D2 D1	I_{OH} = − 10.0 mA I_{OH} = − 8.0 mA I_{OH} = − 4.0 mA	2.7 2.7 2.7			V
I_{OS}	Short Circuit Output Current[7]	D3 D2 D1	$V_O = V_{DD}$ or V_{SS}	− 450 − 300 − 150		360 240 120	mA

DC CHARACTERISTICS - CMOS INTERFACE[1] EIA/JEDEC Standard for CMOS Integrated Circuit Specifications, V_{DD} = 5V

Symbol	Parameter	Condition	Limits[3] TLOW Min	TLOW Max	+25°C Min	+25°C Typ	+25°C Max	THIGH Min	THIGH Max	Unit
V_{IL}	Low-Level Input Voltage			1.5			1.5		1.5	V
V_{IH}	High-Level Input Voltage		3.5		3.5			3.5		V
V_{OL}	Low-Level Output Voltage	$\lvert I_{OL} \rvert \le 1\,\mu A$		0.05			0.05		0.05	V
V_{OH}	High-Level Output Voltage	$\lvert I_{OH} \rvert \le 1\,\mu A$	4.95		4.95			4.95		V

NOTES:

1. All voltages referenced to V_{SS}, ambient temperature + 25° C unless otherwise specified.
2. Stresses beyond the absolute maximum ratings may cause permanent damage to the device. Prolonged exposure to these ratings may affect device reliability.
3. Temperature ranges specified as follows:
   Commercial 0° C to + 70° C
   Industrial − 40° C to + 85° C
   Military − 55° C to + 125° C (ceramic package only)
4. For specified temperature range, voltage supply specified as V_{DD} = 5V ± 5%.
5. Each output pad has available 2/5, 4/5, or full drive buffer capacity, designated respectively as D_1, D_2, and D_3.
6. Above + 85° C, I_{OL} for D_3, D_2, D_1 is respectively 6.4 mA, 4.8 mA, 1.6 mA. I_{OH} for D_3, D_2, D_1 is respectively 8.0 mA, 6.0 mA, 2.0 mA.
7. Current limiting not available on-chip. Limitations on total maximum current and duration may be required to prevent irreversible damage.

DLM SERIES AC CHARACTERISTICS Conditions: $V_{DD} = 5V$, $T_A = 25°C$, Nominal Process with Statistical Interconnect[1]

CORE MACROCELLS

Logic Description	Parameter[3]	Number of Unit Loads[2]					Units
		1	2	3	4	8	
Single Inverter	t_{PLH} t_{PHL}	1.1 1.1	1.4 1.4	1.8 1.7	2.2 2.1	3.7 3.4	ns
2 Input NAND	t_{PLH} t_{PHL}	1.2 1.9	1.5 2.4	1.8 3.0	2.0 3.5	3.1 5.6	ns
2 Input NOR	t_{PLH} t_{PHL}	2.5 1.4	3.3 1.7	4.0 2.0	4.8 2.4	7.8 3.6	ns
4 Input NAND	t_{PLH} t_{PHL}	2.1 4.5	2.5 5.5	2.9 6.5	3.4 7.4	5.1 11.3	ns
6 Input NAND	t_{PLH} t_{PHL}	4.4 6.5	4.7 6.9	5.1 7.2	5.5 7.5	7.0 8.8	ns
Exclusive NOR	t_{PLH} t_{PHL}	4.2 4.1	4.6 4.5	4.9 4.9	5.3 5.4	6.9 7.1	ns
3 Input Majority Gate (AB + BC + AC)	t_{PLH} t_{PHL}	4.0 2.4	4.9 2.9	5.9 3.3	6.9 3.8	10.7 5.7	ns
Inverting 2:1 Mux Data to Output	t_{PLH} t_{PHL}	2.3 2.1	2.5 2.4	2.8 2.6	3.1 2.8	4.1 3.6	ns
Select to Output	t_{PLH} t_{PHL}	3.6 4.0	3.9 4.2	4.2 4.4	4.4 4.6	5.5 5.5	
D Flip-Flop CLK to QB	t_{PLH} t_{PHL}	3.8 5.4	4.1 5.6	4.4 5.8	4.6 6.0	5.7 6.9	ns
Setup Time Hold Time	t_{SU} t_h	3.4 0.0	3.4 0.0	3.4 0.0	3.4 0.0	3.4 0.0	
JK Flip-Flop CLK to QB	t_{PLH} t_{PHL}	3.9 5.6	4.1 5.8	4.4 6.0	4.7 6.2	5.7 7.1	ns
Setup Time Hold Time	t_{SU} t_h	7.9 0.0	7.9 0.0	7.9 0.0	7.9 0.0	7.9 0.0	
Internal 3-State Propagation Delay	t_{PLH} t_{PHL}	3.5 3.8	4.3 4.1	5.0 4.5	5.8 4.8	8.8 6.1	ns
Enable Time Disable Time	t_{EN} t_{DS}	4.5 3.0	5.0 3.0	5.5 3.0	6.0 3.0	8.2 3.0	
TTL Input Buffer	t_{PLH} t_{PHL}	1.9 1.1	2.2 1.3	2.6 1.4	3.0 1.6	4.5 2.1	ns
CMOS Input Buffer	t_{PLH} t_{PHL}	0.1 0.1	0.2 0.2	0.3 0.3	0.4 0.3	0.8 0.7	ns
Inverting Schmitt Trigger with 1 Volt Hysteresis	t_{PLH} t_{PHL}	3.6 3.9	4.3 4.5	5.1 5.1	5.9 5.6	9.0 7.9	ns

PERIPHERY MACROCELLS

Logic Description	Parameter	Output Load Capacitance					Units
		15 pF	50 pF	85 pF	100 pF	160 pF	
Non-Inverting TTL/CMOS Output Driver Size 3 ($I_{OL} = 8$ mA)	t_{PLH} t_{PHL}	4.7 4.9	6.4 6.2	8.2 7.4	8.9 7.9	11.9 10.1	ns
Non-Inverting TTL/CMOS Output Driver Size 1 ($I_{OL} = 3.2$ mA)	t_{PLH} t_{PHL}	4.4 4.4	7.2 6.4	9.9 8.4	11.1 9.3	15.8 12.7	ns
Inverting TTL Bi-Directional Buffer with 3-State Driver ($I_{OL} = 8$ mA)	t_{PLH} t_{PHL}	2.4 1.7	4.1 3.0	5.9 4.2	6.6 4.8	9.6 6.9	ns
Inverting TTL Bi-Birectional Buffer with 3-State Driver ($I_{OL} = 3.2$ mA)	t_{PLH} t_{PHL}	2.5 2.1	5.3 4.1	8.0 6.1	9.2 6.9	13.9 11.4	ns

NOTES:

1. To calculate worst case performance multiply nominal values by 1.4, and derate over temperature and voltage ranges with $K_T = +0.45\%/°C$ and $K_V = -30\%/V$.
2. A Unit Load is defined as the equivalent capacitance of a one logic input, using statistical interconnection capacitance. Actual propagation delays are a function of both fanout (additional loads) and layout (interconnection) loading.
3. Propagation delay times are specified from input 50% waveform point to output 50% waveform point.

TABLE 1. DLM SERIES MACROCELLS

MACRO NAME	DESCRIPTION	GATE COUNT	CELL COUNT
DMIN	Inverter	0.5	1
DM2XIN	Inverter (2X)	1	1
DM3XIN	Inverter (3X)	0.5	1
DM4XIN	Inverter (4X)	2	2
DMDIN	Inverter (Delayed)	1.5	1
DM2CIN	True/Complement (2X) Buffer	1.5	1
DM3CIN	True/Complement (3X) Buffer	2	2
DM2ND	2-Input NAND	1	1
DM3ND	3-Input NAND	1.5	1
DM4ND	4-Input NAND	2	2
DM6ND	6-Input NAND	4.5	3
DM8ND	8-Input NAND	5.5	4
DM2NDI	2-Input NAND/AND	1.5	1
DMI2ND	2-Input NAND with Inverting Input	1.5	1
DM2NR	2-Input NOR	1	1
DM3NR	3-Input NOR	1.5	1
DM4NR	4-Input NOR	2	2
DM6NR	6-Input NOR	4.5	3
DM8NR	8-Input NOR	5.5	4
DM2NRI	2-Input NOR/OR	1.5	1
DMI2NR	2-Input NOR with Inverting Input	1.5	1
DMON1	2-Input OR, 2-Input NAND into 2-Input NAND	2.5	2
DMON2	2-Input AND, 2-Input NOR into 2-Input NOR	2.5	2
DM2ANR	2-Input AND into 3-Input NOR	1.5	1
DM3ANR	2-Input AND into 3-Input NOR	2	2
DM4ANR	Two 2-Input ANDs into 2-Input NOR	2	2
DM2OND	2-Input OR into 2-Input NAND	1.5	1
DM3OND	2-Input OR into 3-Input NAND	2	2
DM4OND	Two 2-Input ORs into 2-Input NAND	2	2
DM5ANR	Majority Gate (AB + BC + AC)	3	2
DMEX	Exclusive OR/NOR	3	2
DMGMUX	2:1 Multiplexer	3.5	3
DMTGI	Inverting 2:1 Multiplexer	4	3
DMCAP	Capacitor	1.5	1
DMDF	D F/F (Two Phase Clock)	6	4
DMDFC	D F/F (Single Phase Clock)	6	4
DMRF	D F/F (Reset, Two Phase Clock)	6	4
DMRFC	D F/F (Reset, Single Phase Clock)	6	4
DMSF	D F/F (Set, Two Phase Clock)	5	4
DMSRF	D F/F (Set, Two Phase Clock)	6	6
DMSRFC	D F/F (Set, Reset, Single Phase Clock)	6.5	6
DMSL	D Latch (Set)	3	2
DMRL	D Latch (Reset)	3	2
DMJK	JK F/F	9	6
DMJKR	JK F/F (Reset)	8.5	6
DMJKS	JK F/F (Set)	8	6
DMJKSR	JK F/F (Set, Reset)	9	8
DMTRF	T F/F (Reset)	8	6
DMTSF	T F/F (Set)	7	6
DMTSRF	T F/F (Set, Reset)	8	8
DMITS	Non-Inverting, Active HIGH, 3-State Logic for Internal Logic	3.5	3
DMTRI	Non-Inverting, Active HIGH, 3-State Logic for Prescaled or CMOS Bidirectional I/O	3	2
DMTRIE	Non-Inverting, Active LOW, 3-State Logic for Prescaled or CMOS Bidirectional I/O	3	2

MACRO NAME	DESCRIPTION	GATE COUNT	CELL COUNT
DMITRI	Inverting, Active HIGH, 3-State Logic for Prescaled or CMOS Bidirectional I/O	2.5	2
DMITRIE	Inverting, Active LOW, 3-State Logic for Prescaled or CMOS Bidirectional I/O	2.5	2
DMPTRI	Non-Inverting, Active HIGH, 3-State Logic for TTL Bidirectional I/O	6	4
DMPTRIE	Non-Inverting, Active LOW, 3-State Logic for TTL Bidirectional I/O	6	4
DMPITRI	Inverting, Active HIGH, 3-State Logic for TTL Bidirectional I/O	5.5	4
DMPITRIE	Inverting, Active LOW, 3-State Logic for TTL Bidirectional I/O	5.5	4
DMAI	Input Protection	0	0
DMAP1	Input Protection with 30K Pull-Up	0	0
DMAP3	Input Protection with 100K Pull-Up	0	0
DMAN1	Input Protection with 30K Pull-Down	0	0
DMAN3	Input Protection with 100K Pull-Down	0	0
DMLSTI	TTL Level Shifter	0	0
DMLSTP1	TTL Level Shifter with 30K Pull-Up	0	0
DMLSTP3	TTL Level Shifter with 100K Pull-Up	0	0
DMLSTN1	TTL Level Shifter with 30K Pull-Down	0	0
DMLSTN3	TTL Level Shifter with 100K Pull-Down	0	0
DMSMIT	Inverting Schmitt Trigger	2	2
DMSMIT1	Non-Inverting Schmitt Trigger	2.5	3
DMD1	Non-Inverting Output Driver Size 1 (3.2 mA)	0	0
DMD2	Non-Inverting Output Driver Size 2 (6.4 mA)	0	0
DMD3	Non-Inverting Output Driver Size 3 (8.0 mA)	0	0
DMTR1	Non-Inverting Three-State, Output Driver Size 1	0	0
DMTR2	Non-Inverting Three-State, Output Driver Size 2	0	0
DMTR3	Non-Inverting Three-State, Output Driver Size 3	0	0
DMTR1ZI	CMOS I/O (Driver 1)	0	0
DMTR1ZP1	CMOS I/O (Driver 1, 30K PU)	0	0
DMTR1ZP3	CMOS I/O (Driver 1, 100K PU)	0	0
DMTR1ZN1	CMOS I/O (Driver 1, 30K PD)	0	0
DMTR1ZN3	CMOS I/O (Driver 1, 30K PD)	0	0
DMTR2ZI	CMOS I/O (Driver 2)	0	0
DMTR2ZP1	CMOS I/O (Driver 2, 30K PU)	0	0
DMTR2ZP3	CMOS I/O (Driver 2, 100K PU)	0	0
DMTR2ZN1	CMOS I/O (Driver 2, 30K PD)	0	0
DMTR2ZN3	CMOS I/O (Driver 2, 100K PD)	0	0
DMTR3ZI	CMOS I/O (Driver 3)	0	0
DMTR3ZP1	CMOS I/O (Driver 3, 30K PU)	0	0
DMTR3ZP3	CMOS I/O (Driver 3, 100K PU)	0	0
DMTR3ZN1	CMOS I/O (Driver 3, 30K PD)	0	0
DMTR3ZN3	CMOS I/O (Driver 3, 100K PD)	0	0
DMST1ZI	TTL I/O (Driver 1, TTL Receiver)	0	0
DMST1ZP1	TTL I/O (Driver 1, 30K PU, TTL Receiver)	0	0
DMST1ZP3	TTL I/O (Driver 1, 100K PU, TTL Receiver)	0	0
DMST1ZN1	TTL I/O (Driver 1, 30K PD, TTL Receiver)	0	0
DMST1ZN3	TTL I/O (Driver 1, 100K PD, TTL Receiver)	0	0
DMST2ZI	TTL I/O (Driver 2, TTL Receiver)	0	0
DMST2ZP1	TTL I/O (Driver 2, 30K PU, TTL Receiver)	0	0
DMST2ZP3	TTL I/O (Driver 2, 100K PU, TTL Receiver)	0	0
DMST2ZN1	TTL I/O (Driver 2, 30K PD, TTL Receiver)	0	0
DMST2ZN3	TTL I/O (Driver 2, 100K PD, TTL Receiver)	0	0
DMST3ZI	TTL I/O (Driver 3, TTL Receiver)	0	0
DMST3ZP1	TTL I/O (Driver 3, 30K PU, TTL Receiver)	0	0
DMST3ZP3	TTL I/O (Driver 3, 100K PU, TTL Receiver)	0	0
DMST3ZN1	TTL I/O (Driver 3, 30K PD, TTL Receiver)	0	0
DMST3ZN3	TTL I/O (Driver 3, 100K PD, TTL Receiver)	0	0

CDI **DLM SERIES HCMOS Gate Arrays**

PACKAGING CONSIDERATIONS

Present packaging options are divided into three main categories:

Dual In Line Package (DIP)
Chip Carriers (LCC/PLCC)
Pin Grid Arrays (PGA)

The following table shows the packaging options available for California Devices DLM gate array family.

Available Lead Counts:

plastic DIP	8,14,16,18,20,22,24,28,40,48,64
ceramic DIP	8,14,16,18,20,22,24,28,40,48,64
CERDIP	8,14,16,18,20,22,24,28,40
LCC	16,18,20,22,24,28,30,32,34,36,40, 44,48,52,54,56,58,64,68,76,80,84,100
PLCC	28,44,68,84
PGA	64,68,72,84,100,104,120,132,139, 144,180

DLM SERIES OF GATE ARRAYS

Package Type	200	400	700	900	1200	1600	2100	2800	3600	4600	7200	10000
plastic DIP	8+	8+	8+	8+	14+	22+	22+	22+	24+	48+	64+	
ceramic side-brazed DIP	8+	8+	8+	8+	8+	14+	14+	14+	16+	16+	24+	24+
CERDIP	8+	8+	8+	8+	8+	16+	22+	22+	22+	28+		
ceramic LLCC	16+	16+	16+	16+	16+	16+	16+	18+	24+	24+	28+	28+
plastic LCC	28+	28+	28+	28+	28+	28+	28+	28+	22+	44+	68+	68+
PGA	64+	64+	64+	64+	64+	64+	64+	64+	64+	64+	64+	64+

LLCC = Leadless Chip Carrier, LCC = Leaded Chip Carrier, PGA = Pin Grid Array

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JBA 5M85/Printed in U.S.A.