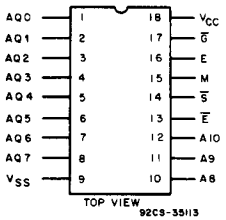
CDP65516 997368 16K (4K) **Product Preview**

CMOS 2048-Word x 8-Bit Static Read-Only Memory



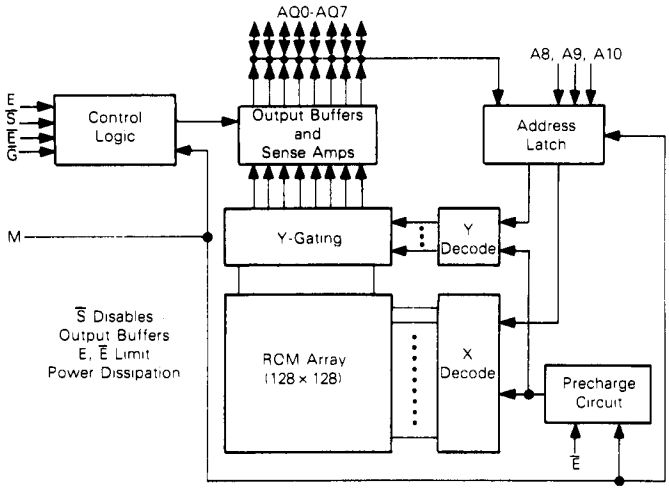
TERMINAL ASSIGNMENT

Features

- *3 to 6 volt supply*
- *Access time*
  430 ns (5 V) CDP65516-43
  550 ns (5 V) CDP65516-55
- *Low power dissipation*
  15 mA maximum(active)
  30 μA maximum (standby)
- *Directly compatible with muxed bus CMOS microprocessors*
- *Pins 13, 14, 16, and 17 are mask programmable*
- *MOTEL mask option also insures direct compatibility with many NMOS microprocessors*
- *Standard 18-pin package*

The CDP65516 is a complementary MOS mask programmable byte organized read-only memory (ROM). The CDP65516 is organized as 2048 bytes of 8 bits, designed for use in multiplex bus systems. It is fabricated using silicon gate CMOS technology, which offers low-power operation from a single 5-volt supply.

The memory is compatible with CMOS microprocessors that share address and data lines. Compatibility is enhanced by pins 13, 14, 16, and 17 which give the user the versatility of selecting the active levels of each. Pin 17 allows the user to choose active high, active low or a third option of programming which is termed the "MOTEL" mode. If this mode is selected by the user, it provides direct compatibility with the CDP6805E2 type microprocessor series. In the MOTEL operation the ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This unique operational feature makes the ROM an extremely versatile part.



PIN NAMES	
AQ0-AQ7	Address/Data Output
A8-A10	Address
M	Multiplex Address Strobe
E	Chip Enable
S	Chip Select
G	Data Strobe (Output Enable)

Fig. 1 - Block diagram.

File Number **1376**

CDP65516

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7	V
Input Voltage	V_{in}	−0.3 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5	5.5	V
Input High Voltage	V_{IH}	$V_{CC}-2$	–	5.5	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	CDP65516-43		CDP65516-55		Unit	Test Condition
		Min	Max	Min	Max		
Output High Voltage Source Current −1.6 mA	V_{OH}	$V_{CC}-0.4$ V	–	$V_{CC}-0.4$ V	–	V	
Output Low Voltage Sink Current +1.6 mA	V_{OL}	–	0.4	–	0.4	V	
Supply Current (Operating)	I_{CC1}	–	15	–	15	mA	$C_L = 130$ pF, $V_{in} = V_{IH}$ to V_{IL} $t_{cyc} = 1$ μs
Supply Current (DC Active)	I_{CC2}	–	100	–	100	μA	$V_{in} = V_{CC}$ to GND
Standby Current	I_{SB}	–	30	–	50	μA	$V_{in} = V_{CC}$ to GND
Input Leakage	I_{in}	−10	+10	−10	+10	μA	
Output Leakage	I_{OL}	−10	+10	−10	+10	μA	

CAPACITANCE ($f = 1$ MHz, $T_A = 25°C$, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	5	pF
Output Capacitance	C_{out}	12.5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

READ CYCLE

$C_L = 130$ pF

Parameter	Symbol	CDP65516-43		CDP65516-55		Unit
		Min	Max	Min	Max	
Address Strobe Access Time	t_{MLDV}	–	430	–	550	ns
Read Cycle Time	t_{MHMH}	–	750	–	1000	ns
Multiplex Address Strobe High to Multiplex Address Strobe Low (Pulse Width)	t_{MHML}	150	–	175	–	ns
Data Strobe Low to Multiplex Address Strobe Low	t_{GLML}	50	–	50	–	ns
Multiplex Address Strobe Low to Data Strobe High	t_{MLGH}	100	–	160	–	ns
Address Valid to Multiplex Address Strobe Low	t_{AVML}	50	–	50	–	ns
Chip Select Low to Multiplex Address Strobe Low	t_{SLML}	50	–	50	–	ns
Multiplex Address Strobe Low to Chip Select High	t_{MLSH}	50	–	80	–	ns
Chip Enable Low/High to Multiplex Address Strobe Low	t_{ELML} t_{EHML}	50 50	– –	50 50	– –	ns
Multiplex Address Strobe Low to Address Don't Care	t_{MLAX}	50	–	80	–	ns
Data Strobe High to Data Valid	t_{GHDV}	175	–	200	–	ns
Data Strobe Low to High-Z	t_{GLDZ}	–	160	–	160	ns

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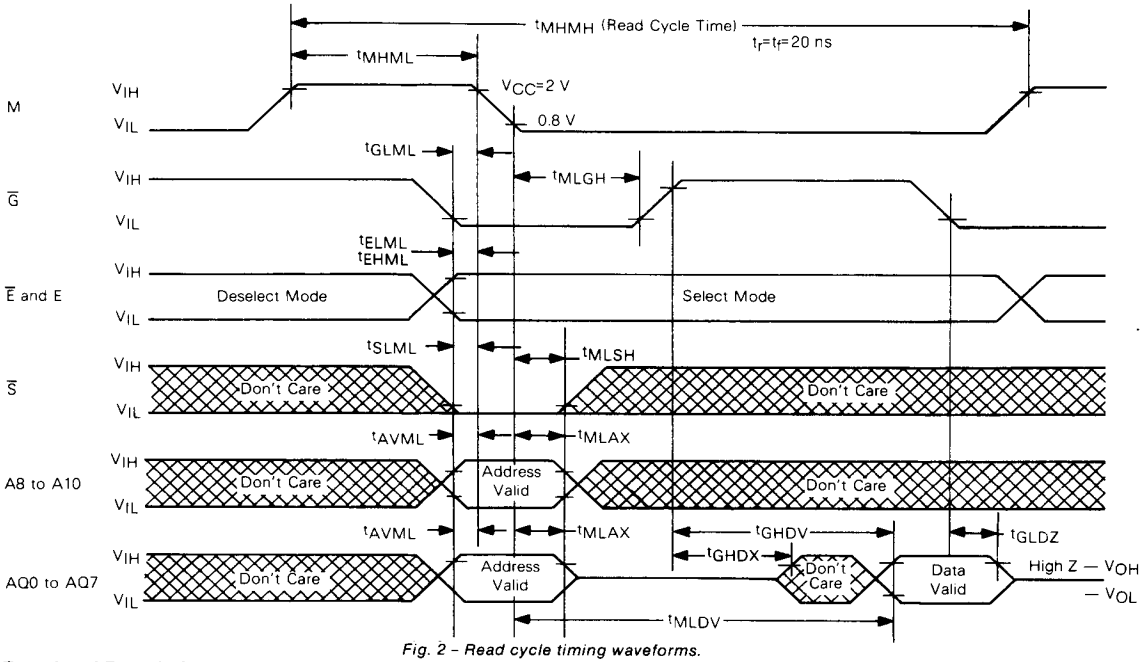

Fig. 2 - Read cycle timing waveforms.

Functional Description

The 2K x 8 bit CMOS ROM (CDP65516) shares address and data lines and, therefore, is compatible with the majority of CMOS microprocessors in the industry. The package size is reduced from 24 pins for standard NMOS ROMs to 18 pins because of the multiplexed bus approach. The savings in package size and external bus lines adds up to tighter board packing density which is handy for battery-powered hand-carried CMOS Systems. This ROM is designed with the intention of having very low active as well as standby currents. The active power dissipation of 75 mW (at V_{CC}=5 V, freq.=1 MHz) and standby power of 150 μW (at V_{CC}=5 V) add up to low power for battery operation. The typical access time of the ROM is 280 ns making it acceptable for operation with today's existing CMOS microprocessors.

An example of this operation is shown in Fig. 3. Shown is a typical connection with the CDP6805E2 CMOS microprocessor. The main difference between this system and competitive process is that the data strobe (DS) on the CDP6805E2 and the read bar ($\overline{RD}$) on the competitive process both control the output of data from the ROM but are of opposite polarity. The 2K x 8 ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This is termed the MOTEL mode of operation. This unique operational feature makes the ROM an extremely versatile part. Further operational features are explained in the following section.

Operational Features

In order to operate in a multiplexed bus system the ROM latches, for one cycle, the address and chip-select input information on the trailing edge of address strobe (M) so the address signals can be taken off the bus.

Since they are latched, the address and chip-select signals have a setup and hold time referenced to the negative edge of address strobe. Address strobe has a minimum pulse width requirement since the circuit is internally precharged during this time and is set up for the next cycle on the trailing edge of address strobe. Access time is measured from the negative edge of address strobe.

The part is equipped with a data strobe input (G) which controls the output of data onto the bus lines after the addresses are off the bus. The data strobe has three potential modes of operation which are programmable with the ROM array. The first mode is termed the MOTEL mode of operation. In this mode, the circuit can work with either the 6805 or 8085 type microprocessor series. The difference between the two series for a ROM peripheral is only the polarity of the data-strobe signal. Therefore, in the MOTEL mode the ROM recognizes the state of the data-strobe signal at the trailing edge of address strobe (requires a setup and hold time), latches the state into the circuit after address strobe, and turns on the data outputs when an opposite polarity signal appears on the data-strobe input. In this manner the data-strobe input can work with either polarity signal but that signal must toggle during a cycle to output data on the bus lines. If the data strobe remains at a dc level the outputs will remain off. The data-strobe input has two other programmable modes of operation and those are the standard static select modes (high or low) where a dc input not synchronous with the address strobe will turn the output on or off.

The chip-enable and chip-select inputs are all programmable with the ROM array to either a high or low select. The chip select acts as an additional address and is latched on the address-strobe trailing edge. On deselect the chip select merely turns off the output drivers acting as an output disable. It does not power down the chip. The chip-enable inputs, however, do put the chip in a power down standby mode but they are not latched with address strobe and must be maintained in a dc state for a full cycle.

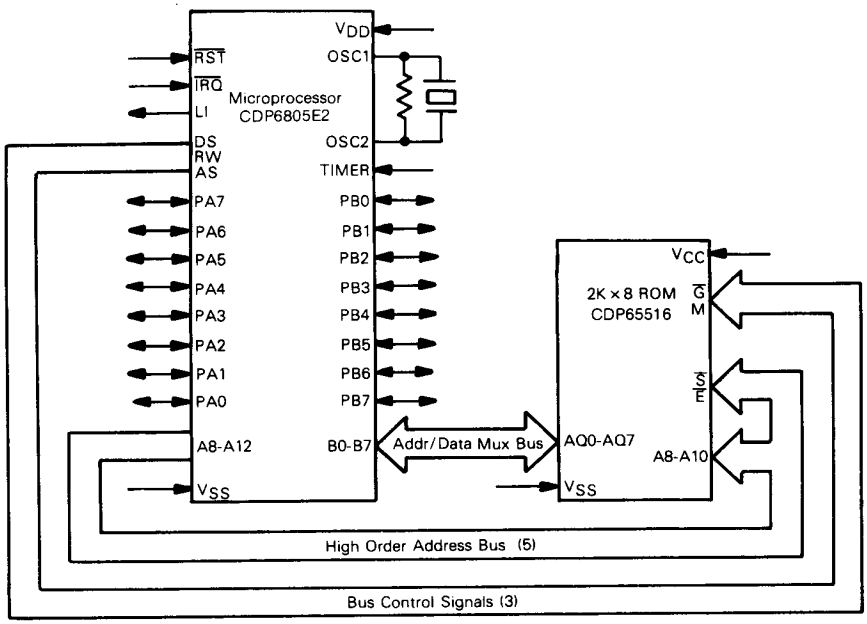

Fig. 3 - Typical minimum system.

Introduction

CBUG05 is a debug monitor program written for the CDP6805E2 Microprocessor Unit and contained in the CDP65516 2K x 8 CMOS ROM. CBUG05 allows for rapid development and evaluation of hardware and 6805 Family type software, using memory and register examine/change commands as well as breakpoint and single instruction trace commands. CBUG05 also includes software to set and display time, using an optional CDP6818 Real-Time Clock (RTC), and routines to punch and load an optional cassette interface. Fig. 2 shows a minimum system which only requires the MPU, ROM, keypad inputs and display output interfaces. Port A of the CDP6805E2 MPU is required for the I/O; however, Port B and all other CDP6805E2 MPU features remain available to the user. A possible expanded system is shown in Fig. 3.

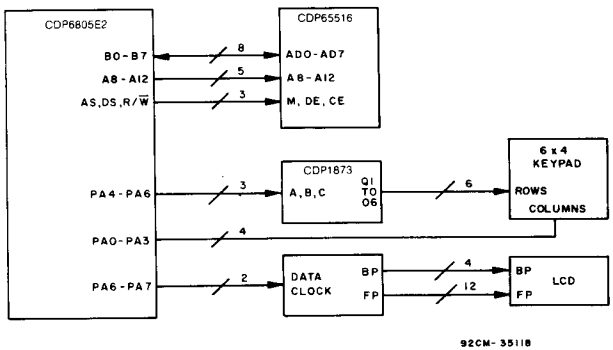

Fig. 4 - Minimum CBUG05 system.

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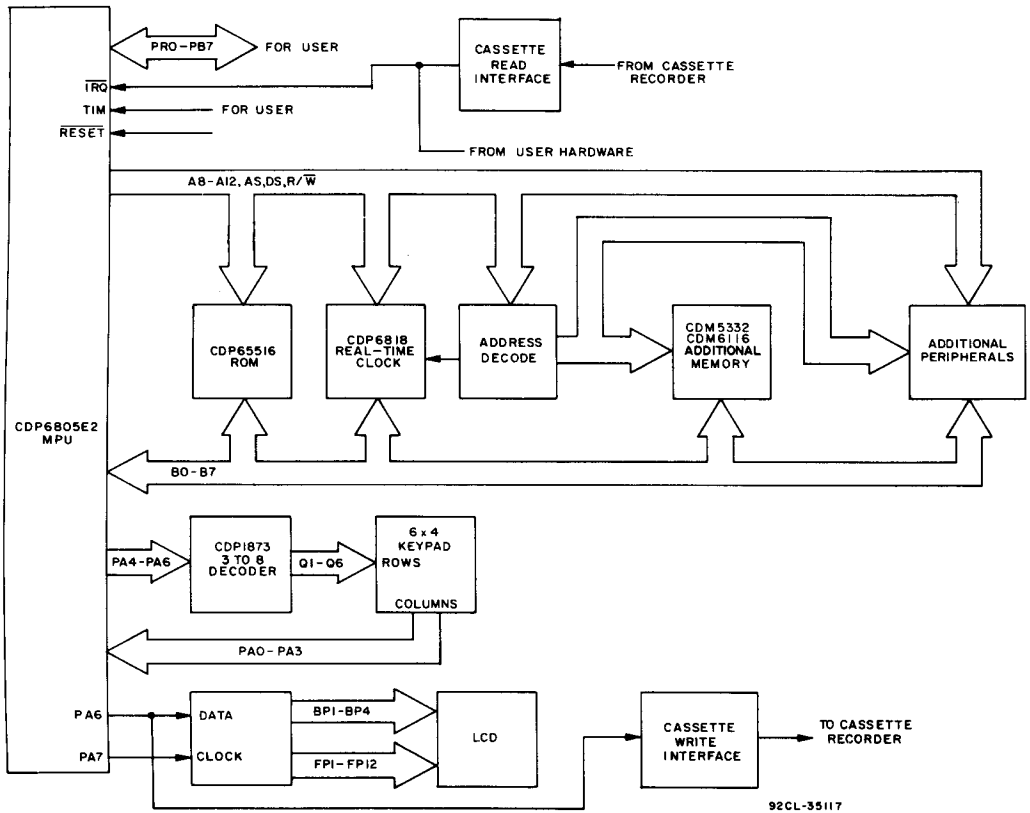

Fig. 5 - Expanded CBUG05 system.

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DATA PROGRAMMING INSTRUCTIONS

When a customer submits instructions for programming RCA custom ROM s, the customer must also complete the relevant parts of the ROM information sheet and submit this sheet together with the programming instructions. Programming instructions may be submitted in any one of three ways, as follows:

1. **Computer-Card Deck**—use standard 80-column computer punch cards.
2. **Floppy Diskette**—diskette information must be generated on an RCA CDP1800-series microprocessor development system.
3. **Master Device** — a ROM, PROM, or EPROM that contains the required programming information.

The requirements for each method are explained in detail in the following paragraphs:

COMPUTER-CARD METHOD

Use standard 80-column computer cards. Each card deck must contain, in order, a title card, an option card, a data-format card, and data cards. Punch the cards as specified in the following charts:

TITLE CARD

Column No.	Data
1	Punch T
2-5	leave blank
6-30	Customer Name (start at 6)
31-34	leave blank
35-54	Customer Address or Division (start at 35)
55-58	leave blank
59-63	RCA custom selection number (5 digits) (Obtained from RCA Sales Office)
64	leave blank
65-71	RCA device type, without CDP6 prefix, e.g., 5516
72	Punch an opening parenthesis (
73	Punch 8
74	Punch a closing parenthesis)
75-78	leave blank
79-80	Punch a 2-digit decimal number to indicate the deck number; the first deck should be numbered 01

OPTION CARD

Use the ROM Information Sheet to select the polarity options, P, N, or X, for the desired ROM type.

Column No.	Data
1-6	Punch the word OPTION
7	leave blank
8-17	RCA device type, including CDP6 prefix, e.g., CDP65516
18-27	leave blank
28-31	Punch P or N per ROM Information Sheet
32-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

DATA-FORMAT CARD

The data-format card specifies the form in which the data is to be entered into ROM.

Column No.	Data
1-11	Punch the words DATA FORMAT
12	leave blank
13-15	Punch the letters HEX
16	leave blank
17-19	Punch POS
20-78	leave blank
79-80	Punch the deck number (the 2-digit number in columns 79-80 of the title card)

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DATA PROGRAMMING INSTRUCTIONS (Cont'd)

DATA CARDS

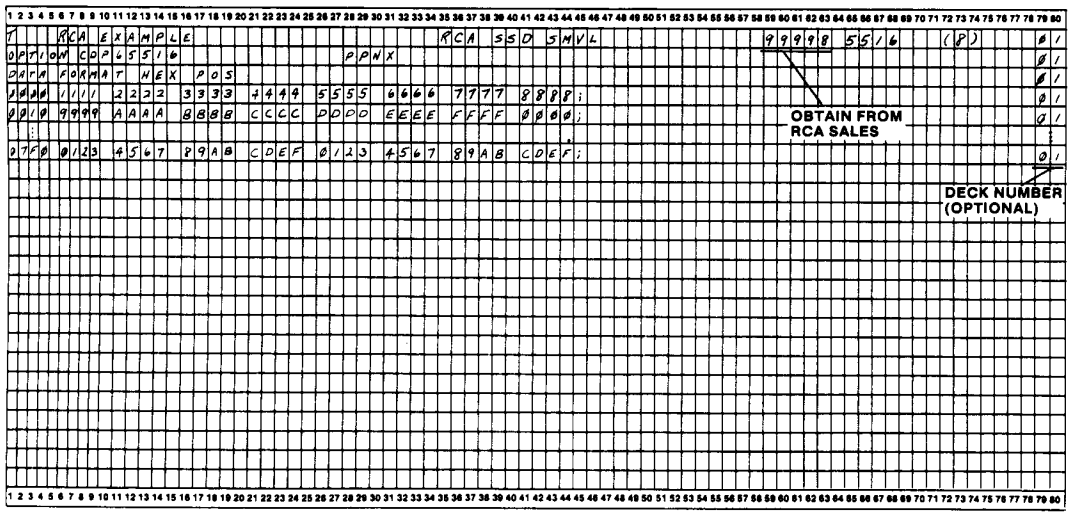
The data cards contain the hexadecimal data to be programmed into the ROM device.
Each card must contain the starting address plus sixteen words of data in clusters of four Hex Bytes.

Column No.	Data
1-4	Punch the starting address in hexadecimal for the following data.*
5	Blank
6-7	2 hex digits of 1st WORD
8-9	2 hex digits of 2nd WORD
10	Blank
11-12	2 hex digits of 3rd WORD
13-14	2 hex digits of 4th WORD
15	Blank
16-17	2 hex digits of 5th WORD
18-19	2 hex digits of 6th WORD
20	Blank
21-22	2 hex digits of 7th WORD
23-24	2 hex digits of 8th WORD
25	Blank

Column No.	Data
26-27	2 hex digits of 9th WORD
28-29	2 hex digits of 10th WORD
30	Blank
31-32	2 hex digits of 11th WORD
33-34	2 hex digits of 12th WORD
35	Blank
36-37	2 hex digits of 13th WORD
38-39	2 hex digits of 14th WORD
40	Blank
41-42	2 hex digits of 15th WORD
43-44	2 hex digits of 16th WORD
45	Semicolon, blank if last card
46-78	Blank
79-80	Punch 2 decimal digits as in title card

*The address block must be contiguous starting at an even-numbered address. Column 4 must be zero.

OPTION DATA CARD



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ROM INFORMATION SHEET

OPTION LIST

Select the options for your ROM from the following list. A manufacturing mask will be generated from this information. Select one in each section..

PROGRAMMABLE PIN OPTIONS

	Pin Number			
	13 ($\overline{E}$)	14 ($\overline{S}$)	16 (E)	17 ($\overline{G}$)
Active High (1 or P)	☐	☐	☐	☐
Active Low (1 or P)	☐	☐	☐	☐
MOTEL (X)	—	—	—	☐
	28	29	30	31

Column Number
(On Option Card)

CUSTOMER INFORMATION

Customer Name _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____ Extension _____

Contact Ms./Mr. _____

Customer Part No. _____

PATTERN MEDIA

☐ EPROM

☐ Card Deck

☐ Other*

*Other media require factory approval.

Signature _____

Title _____