NEC
NEC Electronics Inc.

μPD46258L
32,768 x 8-Bit
Static BiCMOS RAM

Preliminary Information

November 1993

Description

The μPD46258L is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses BiCMOS peripheral circuits and N-channel memory cells that make the μPD46258L suitable as cache and buffer memory in applications requiring high speed, low voltage, and high density. The μPD46258L is available in standard 32-pin plastic SOJ packaging.

Features

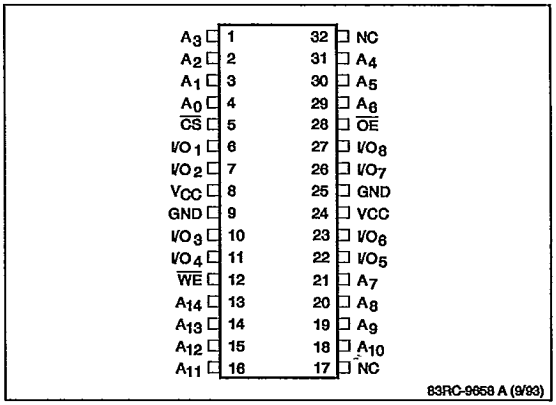
- Single +3.3-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Standard 32-pin plastic SOJ packaging
- Fast access times of 8, 9, and 10 ns (max)

Ordering Information

Part Number	Access Time (max)	Package
μPD46258LLA-8	8 ns	32-pin plastic SOJ
LA-9	9 ns	
LA-10	10 ns	

Pin Configuration

32-Pin Plastic SOJ



83RC-9658 A (9/93)

Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+3.3-volt power supply

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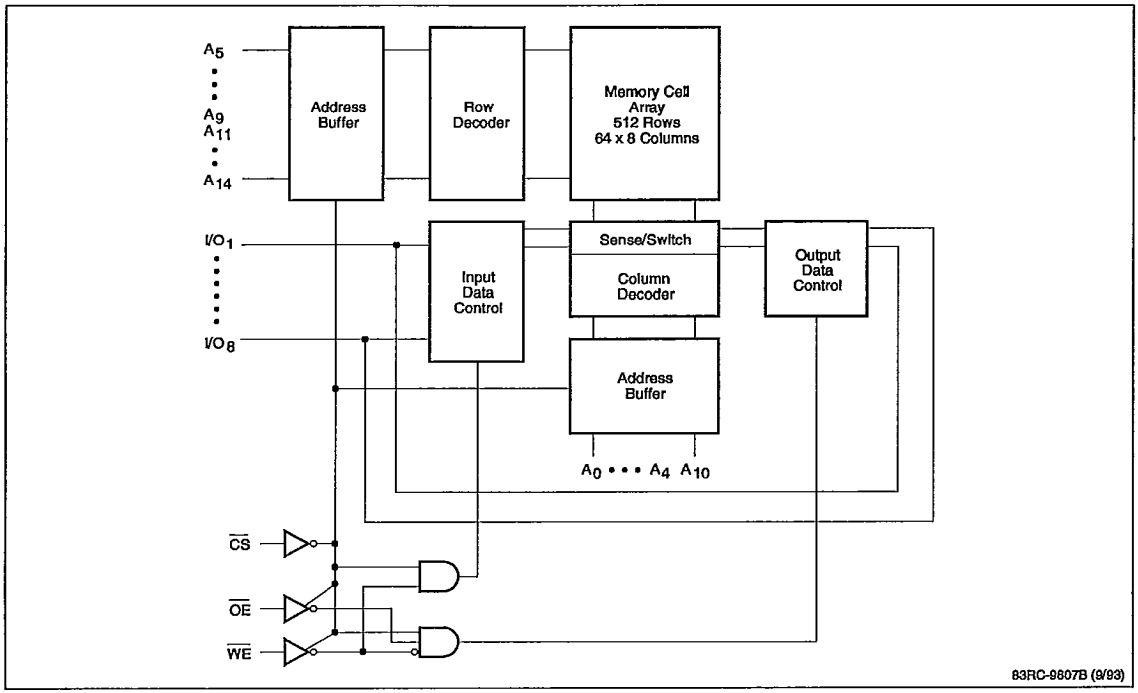
Block Diagram



Truth Table

Function	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	High-Z	Standby
Outputs disabled	L	H	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input voltage, low *	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

* −2.5 V minimum (pulse width = 3 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +3.3 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−10		10	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	I_{CC}			TBD	mA	$\overline{CS} \geq V_{IL}$; $V_{I/O}$ = 0 mA; 100 MHz
	I_{CC1}			TBD	mA	$\overline{CS} \geq V_{IL}$; $V_{I/O}$ = 0 mA; 0 MHz
Standby supply current	I_{SB}			TBD	mA	$\overline{CS} \geq V_{IH}$; $V_{IN} = V_{IH}$ or V_{IL}
	I_{SB1}			TBD	mA	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \leq 0.2$ V or $\geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −2.0 mA

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Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +5.5 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) −2.5 V minimum (pulse width = 3 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Input/output capacitance	$C_{I/O}$		8	pF

Note:

(1) This parameter is sampled and not 100% tested.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +3.3 V ± 10%

		μPD46258L-8		μPD46258L-9		μPD46258L-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	8		9		10		ns	(Note 2)
Address access time	t_{AA}		8		9		10	ns	(Note 2)
Chip select access time	t_{ACS}		8		9		10	ns	(Note 2)
Output enable to output valid	t_{OE}		5		5		6	ns	(Note 2)
Output hold from address change	t_{OH}	2		2		2		ns	(Note 2)
Chip select to output in low-Z	t_{CLZ}	2		2		2		ns	(Note 2)
Output enable to output in low-Z	t_{OLZ}	1		1		1		ns	(Note 2)
Chip select to output in high-Z	t_{CHZ}		4		4		5	ns	(Note 2)
Output enable to output in high-Z	t_{OHZ}		4		4		5	ns	(Note 2)
Write Operation									
Write cycle time	t_{WC}	8		9		10		ns	
Chip select to end of write	t_{CW}	6		6		7		ns	
Address valid to end of write	t_{AW}	6		6		7		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	6		6		7		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	5		5		6		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		4		4		5	ns	(Note 2)
Output active from end of write	t_{OW}	1		1		1		ns	(Note 2)

Notes:

(1) Input pulse levels = GND to 3 V; input pulse rise and fall times = 2 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

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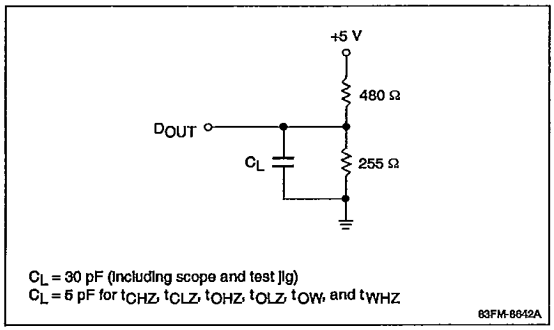
Figure 1. Test Conditions



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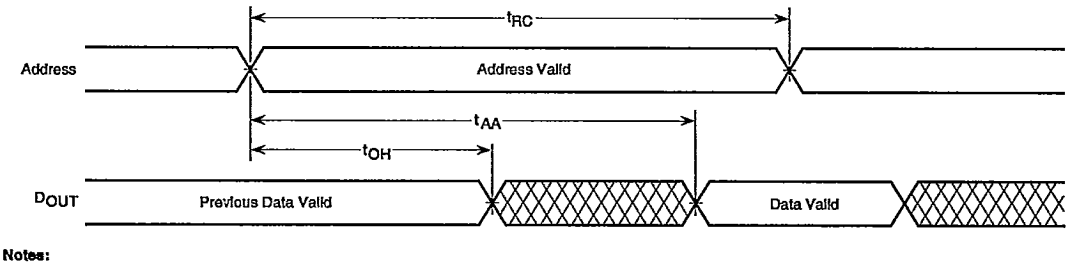
Timing Waveforms

Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

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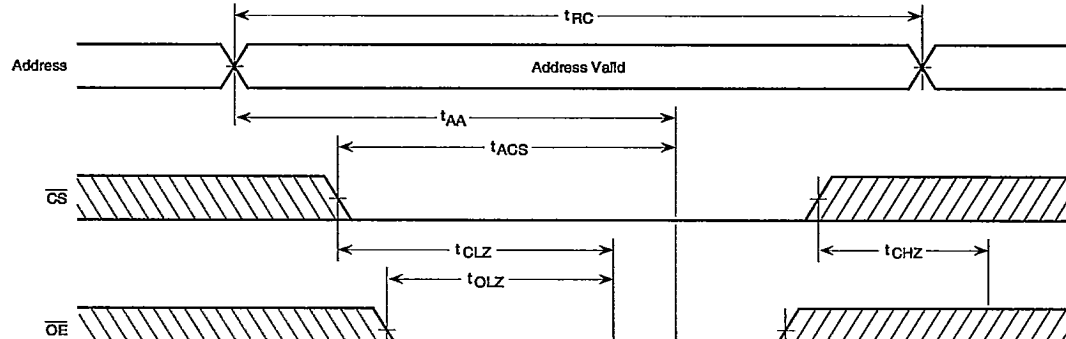
Chip Select Access Cycle



Notes:
1) $\overline{WE}$ is high for a read cycle.
2) Address valid prior to or coincident with the low transition of $\overline{CS}$.

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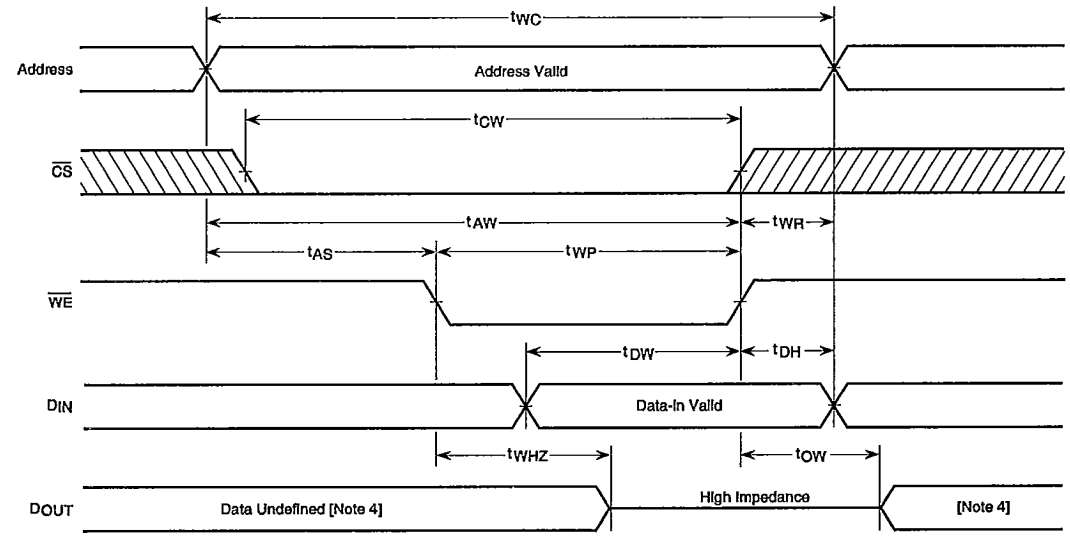
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

83IH-8438B (7/93)

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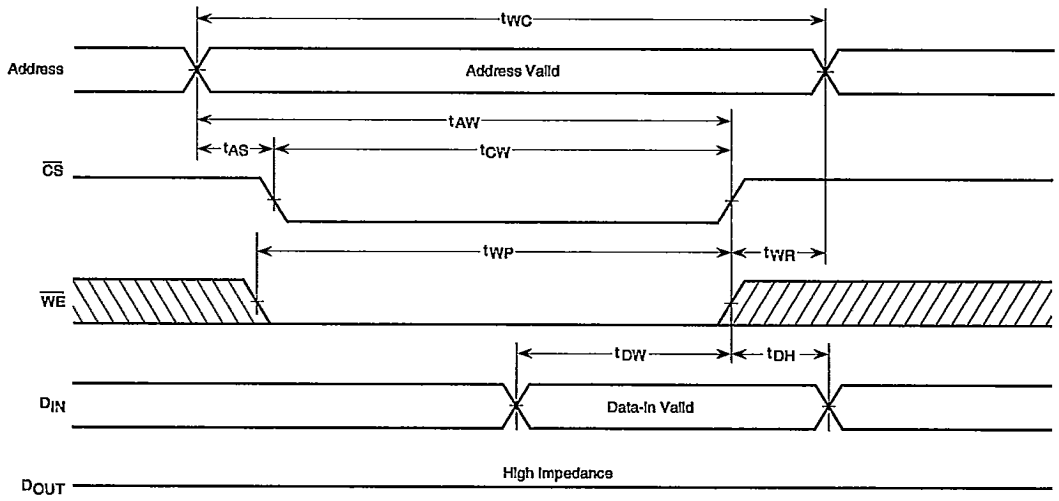
Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

831H-6439B (7/83)

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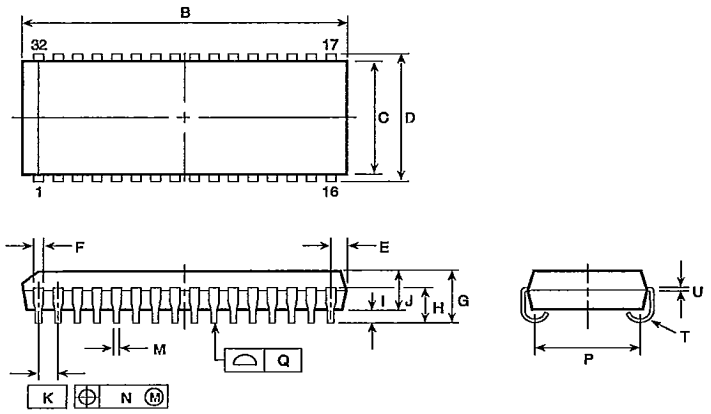
μPD46258L

Package Drawing

32-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	21.21 $^{+0.3}_{-0.35}$	.835 $^{+.009}_{-.014}$
C	7.57	.298
D	8.47 ± 0.2	.333 $^{+.009}_{-.008}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.74	.029
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.55	.100
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	6.73 ± 0.20	.265 ± .008
Q	0.1	.004
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



P32LA-300A

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NEC
NEC Electronics Inc.
CORPORATE HEADQUARTERS
475 Ellis Street
P.O. Box 7241
Mountain View, CA 94039
TEL 415-960-6000

For literature, call toll-free 7 a.m. to 6 p.m. Pacific time:
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