



STY60NM60

N-CHANNEL 600V - 0.050Ω - 60A Max247 Zener-Protected MDmesh™ Power MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STY60NM60	600V	< 0.06Ω	60 A

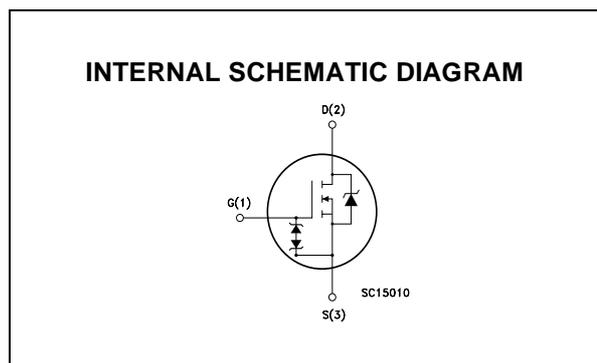
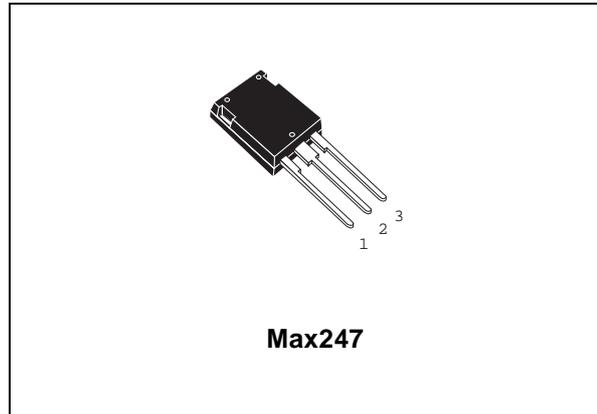
- TYPICAL R_{DS(on)} = 0.050Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL
- INDUSTRY'S LOWEST ON-RESISTANCE

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600	V
V _{GS}	Gate- source Voltage	±30	V
I _D	Drain Current (continuous) at T _C = 25°C	60	A
I _D	Drain Current (continuous) at T _C = 100°C	37.8	A
I _{DM} (●)	Drain Current (pulsed)	240	A
P _{TOT}	Total Dissipation at T _C = 25°C	450	W
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=15KΩ)	4	KV
	Derating Factor	3.6	W/°C
dv/dt	Peak Diode Recovery voltage slope	6	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(●)Pulse width limited by safe operating area

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.277	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	30	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 35 V)	1350	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			10 100	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 30A		0.050	0.06	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = I _{D(on)} × R _{DS(on)max} , I _D = 30A		20		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		4430		pF
C _{oss}	Output Capacitance			733		pF
C _{rss}	Reverse Transfer Capacitance			54		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.5		Ω

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

ELECTRICAL CHARACTERISTICS (CONTINUED)
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V, I_D = 30A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		TBD		ns
t_r	Rise Time			TBD		ns
Q_g	Total Gate Charge	$V_{DD} = 400V, I_D = 60A,$ $V_{GS} = 10V$		104	145	nC
Q_{gs}	Gate-Source Charge			TBD		nC
Q_{gd}	Gate-Drain Charge			TBD		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400V, I_D = 60A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		TBD		ns
t_f	Fall Time			TBD		ns
t_c	Cross-over Time			TBD		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				60	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				240	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 60A, V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 60A, di/dt = 100A/\mu s,$ $V_{DD} = 60V, T_j = 150^\circ C$ (see test circuit, Figure 5)		TBD		ns
Q_{rr}	Reverse Recovery Charge			TBD		μC
I_{RRM}	Reverse Recovery Current			TBD		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

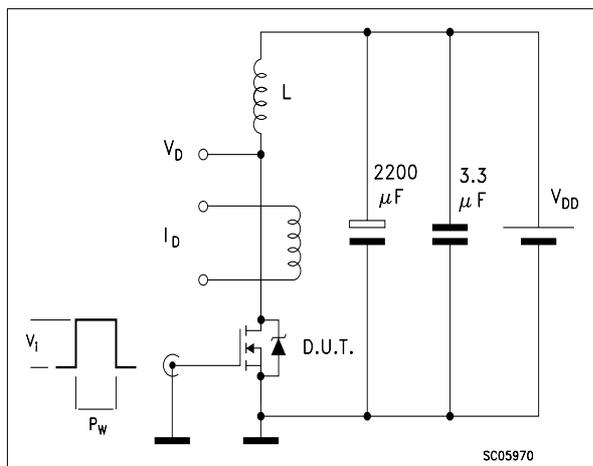


Fig. 2: Unclamped Inductive Waveform

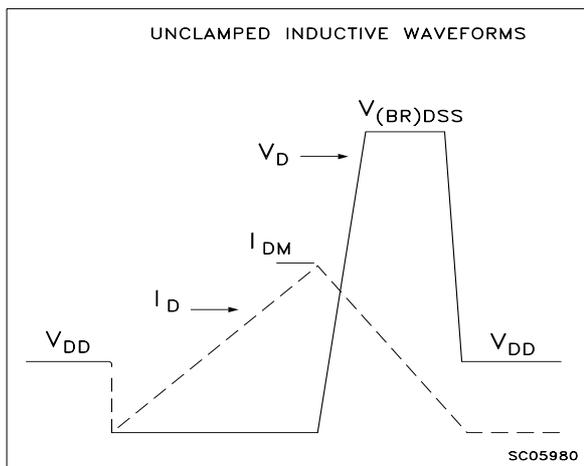


Fig. 3: Switching Times Test Circuit For Resistive Load

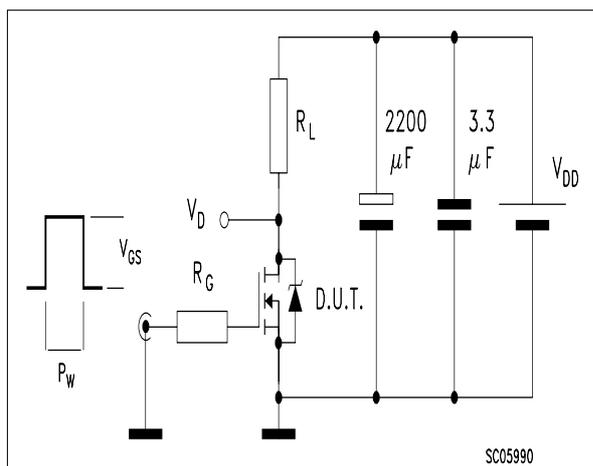


Fig. 4: Gate Charge test Circuit

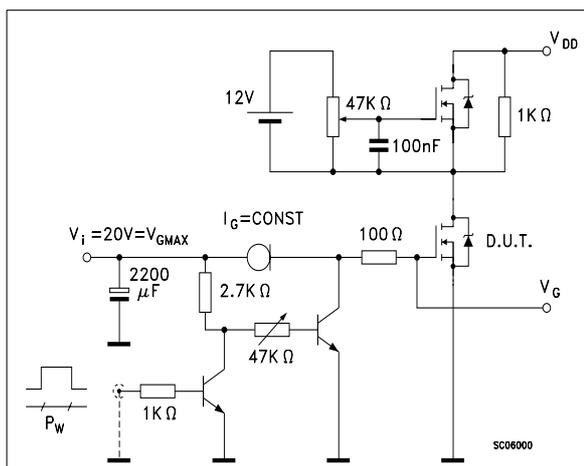
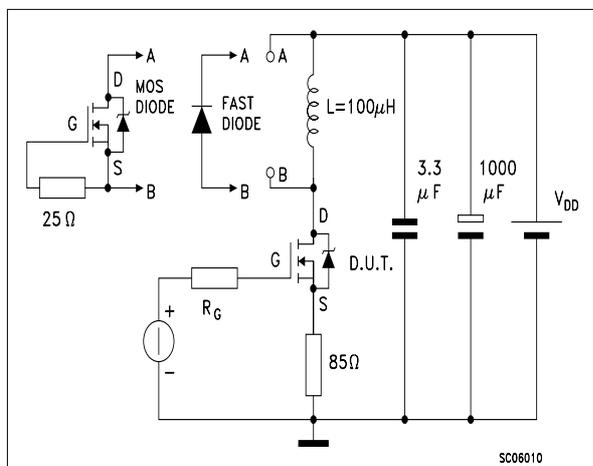
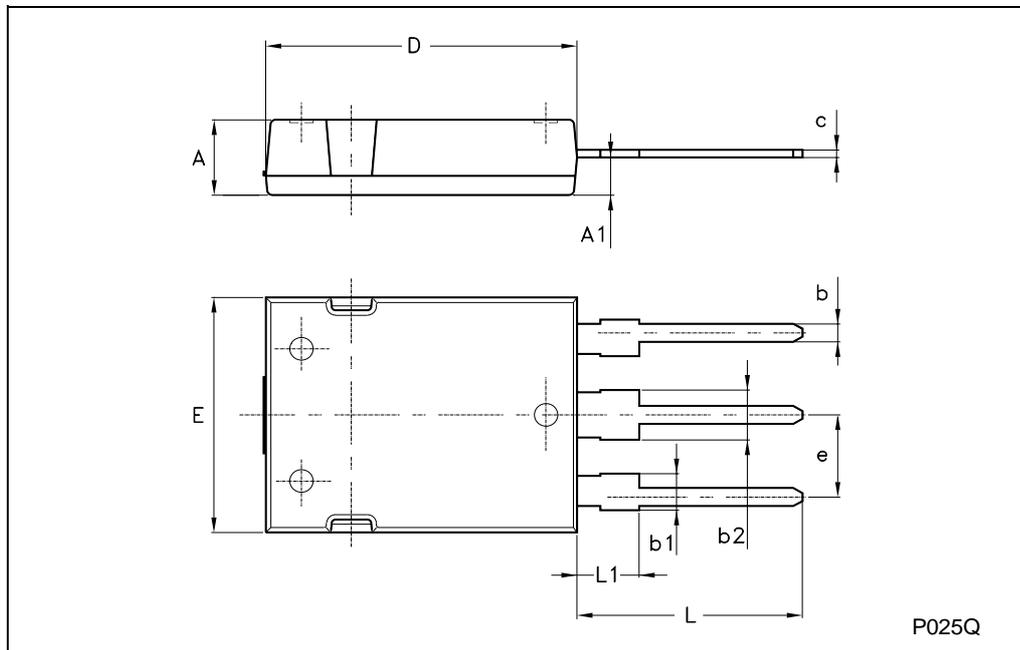


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



Max247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.70		5.30			
A1	2.20		2.60			
b	1.00		1.40			
b1	2.00		2.40			
b2	3.00		3.40			
c	0.40		0.80			
D	19.70		20.30			
e	5.35		5.55			
E	15.30		15.90			
L	14.20		15.20			
L1	3.70		4.30			



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