SSI 32H6827/6828
Servo and Spindle Predriver

January 1995

DESCRIPTION

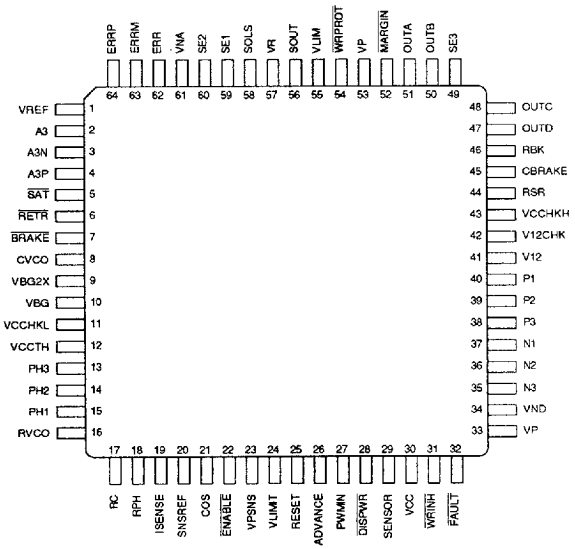
The SSI 32H6827 Servo and Spindle Predriver, a Bipolar monolithic integrated circuit housed in a 64-Lead TQFP package, operates from +5V and +12V supplies. It is designed to drive a voice coil actuator and a 3-phase, sensorless motor with external power MOSFETs. The device is intended for use in 12V disk drive applications. The SSI 32H6828 is a reduced pin count version of the 32H6827 and is housed in a 48-Lead TQFP package. The 32H6828 is a functional subset of the 32H6827 and is a pin-for-pin drop replacement for the SSI 32H6825A.

Improvements to the actuator driver shared by both the 32H6827 and 32H6828 include: a current-sensed window comparator to detect high currents, an uncommitted op-amp for use as a PWM filter, and reduced power dissipation. The 32H6827 also includes a saturation detector to monitor the loop compensation amplifier for saturation and a voltage doubler to provide a precise voltage level for external PWM buffers. (continued)

FEATURES

- **SSI 32H6827 - 64-Lead TQFP package**
- **SSI 32H6828 - small 48-Lead TQFP package**
- **PWM spindle driver during run and start**
- **Commutator is driven by a phase lock loop for high jitter immunity**
- **Adjustable slew rate to minimize stress in the power MOSFETs**
- **Microprocessor controlled spindle startup**
- **Window comparator to detect high actuator currents**
- **Saturation detector to monitor loop compensation amplifier saturation**
- **Significantly reduced power dissipation**
- **Precision low voltage circuitry to monitor both +5V and +12V supplies in 32H6827 only**

PIN DIAGRAM

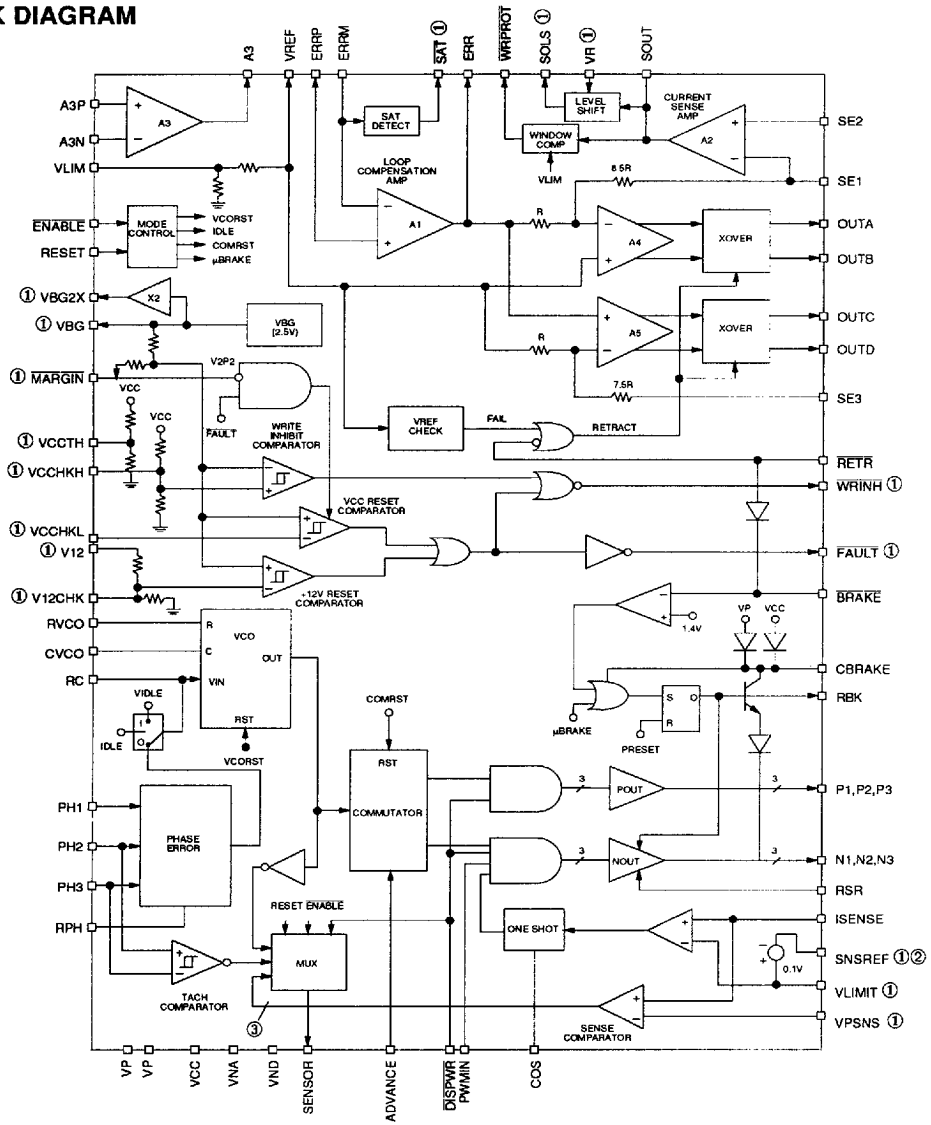


SSI 32H6827
64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

0195 -rev. 2

BLOCK DIAGRAM



NOTES:

① These pins available only in 32H6827.

② SNSREF is internally grounded in the 32H6828.

③ Sensor input PSNS is undefined for the 32H6828.

DESCRIPTION (continued)

Improvements to the spindle driver include significantly reduced power dissipation, a µP controlled startup ramp, an external PWM input to allow PWM frequencies above the audible range, active pullup on the P driver, adjustable N-channel slew rate, and improved spindle brake performance.

In the 32H6827 only, a precision low voltage monitor circuit is provided to monitor +5V and +12V supplies and initiate servo head retracts on voltage fault.

FUNCTIONAL DESCRIPTION

The SSI 32H6827 functional block diagram contains an actuator predriver with PWM interface, a spindle predriver with PLL commutator, and low voltage monitor circuitry. The 32H6828 is a functional subset of the 32H6827 as noted on the Block Diagram and pin definitions.

ACTUATOR PREDRIVER

The actuator predriver serves as a transconductance amplifier by driving four external MOSFETs in an H-bridge configuration. It has two modes of operation which are normal or linear and retract. The retract mode is activated by a power supply failure or upon an external command at $\overline{\text{RETR}}$. Otherwise, the device operates in linear mode. The predriver consists of a voltage doubler, an uncommitted opamp, A1 through A5, a saturation detector, and crossover protection blocks shown as XOVER. It is functionally similar to the SSI 32H6825.

Positioner PWM Interface

The voltage doubler provides a precision voltage source for two off-chip PWM buffers and therefore eliminates logic swing uncertainty of PWM signals. The PWM buffer outputs are then filtered by an external RC network in conjunction with the on-chip uncommitted opamp to generate an acceleration signal.

Loop Compensation Amplifier

During linear operation, the acceleration signal is applied through amplifier A1 with three connections all available externally. RC components may be used to provide loop compensation at this stage. The saturation detector monitors amplifier A1 for saturation. Whenever amplifier A1 is in saturation, the current flowing through the summing node at ERRM will be detected and $\overline{\text{SAT}}$ will be asserted.

MOSFET Drivers

ERR is the output signal of A1 and it drives two precision amplifiers each with a gain of 8.5. The first of these two amplifiers is inverting and it is formed from opamp A4, an on-chip resistor divider, and an off-chip complementary MOSFET pair. The second amplifier is non-inverting and it is formed in a similar manner in opamp A5. Feedback from the MOSFET drains on sense inputs SE1 and SE3 allows the amplifier gains to be established precisely. The voice coil motor and a current sense resistor is connected in series between SE1 and SE3.

Crossover Protection Blocks

Crossover protection circuitry between the outputs of A4 and A5 and the external MOSFETs ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold VTH, illustrated in Figure 1, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also apply a constant voltage across the motor to retract the heads at a constant velocity.

Current Sense Amplifier

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 is fixed gain with internal resistors) through inputs SE1 and SE2. SOUT is referenced to VREF and it is also connected to an internal level-shifter to generate SOLS which is referenced to VR.

Window Comparator

SOUT is connected to a window comparator which is used to detect excessive motor current. When excessive current is detected, $\overline{\text{WRPROT}}$ is pulled low. The VLIM pin may be used to program the voltage limit for the window comparator. The maximum voltage excursion allowed relative to VREF is the difference VREF-VLIM. An on-chip resistor divider sets a default value for VLIM and if VLIM is connected to ground, the windowing is effectively disabled.

FUNCTIONAL DESCRIPTION (continued)

SPINDLE PREDRIVER

The spindle driver section monitors spindle motor back EMF and generates drive signals to three MOSFET power bridges. The predriver includes current limit, a back EMF monitoring circuit to determine optimal commutation points, a phase locked loop to remove jitter from the commutation points, and a delayed spindle brake circuit.

Commutator

The commutator drives the spindle motor windings in proper sequence to commutate a three phase brushless DC spindle motor. In Run mode, the commutator is clocked by the VCO output. In Start mode, the commutator is clocked by external pulses applied at the ADVANCE pin. Table 1 shows the commutation sequence and identifies the external power MOSFETs turned on.

Phase Error Amplifier

The Phase Error circuit compares the undriven winding voltage with the average of the other two winding voltages. Depending on the result of the comparison and the state of the commutator, a positive or negative current is applied to the RC pin. Table 2 shows which winding is undriven and the polarity of the output current when that winding is positive with respect to the average of the other two.

The Phase Error circuit is only used during Run mode. In all other modes, RC is forced to V_{IDLE}, which is an internally generated voltage that will cause the VCO to idle at approximately 1/20 of the run frequency.

The magnitude of the current at RC is the sum of a constant current and a current proportional to the VCO frequency. The constant current value is set by RPH which is biased to 1.2V nominally. The proportional current is set by RVCO which is the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

VCO

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on CVCO is nominally 2.2V. The frequency formula is:

$$F_{VCO} = \frac{V_{RC}}{8.8\ R_{VCO}\ C_{VCO}}$$

The VCO will be reset whenever $\overline{\text{ENABLE}}$ = High and RESET = Low. During VCO reset, the VCO output is forced low. The first VCO clock will occur immediately after the VCO exits reset. This timing relationship is shown in Figure 2.

One Shot

The one shot is triggered whenever ISENSE exceeds VLIMIT (nominally 0.1V). When the one shot times out, it will remain high if ISENSE is still above VLIMIT. During the time the one shot output is high, the N drivers are turned off. This behavior implements the PWM over-current limit where the peak current is found from VLIMIT/R_{MS}

NOUT and POUT

The NOUT predrivers drive the gates of the external N channel power MOSFETs. They have an adjustable source current set by an external resistor at RSR. The POUT predrivers drive the external P channel power MOSFETs. During Brake mode, the POUT predrivers are disabled and all N channel power MOSFETs are turned on effectively shorting the motor windings to implement dynamic braking. During PWM, only the NOUT drivers are modulated.

Spindle Modes of Operation

The spindle driver modes are governed by the RESET, $\overline{\text{ENABLE}}$, and $\overline{\text{DISPWR}}$ inputs according to Table 3. As shown in the table, spindle braking is activated in Brake mode. Brake mode, whether activated by $\overline{\text{ENABLE}}$ and RESET or by a power failure, is internally latched and can only be turned off by asserting Preset mode.

TABLE 1: Commutator Sequence

STATE	N1	N2	N3	P1	P2	P3
Reset	Off	On	Off	On	Off	On
A	Off	Off	On	On	Off	Off
B	Off	Off	On	Off	On	Off
C	On	Off	Off	Off	On	Off
D	On	Off	Off	Off	Off	On
E	Off	On	Off	Off	Off	On
F	Off	On	Off	On	Off	Off

TABLE 2: Undriven Winding and Polarity

COMMUTATOR	UNDRIVEN WINDING	POLARITY
A	PH2	Source
B	PH1	Sink
C	PH3	Source
D	PH2	Sink
E	PH1	Source
F	PH3	Sink

TABLE 3: Spindle Modes of Operation

RESET	$\overline{\text{ENABLE}}$	$\overline{\text{DISPWR}}$	MODE	Sensor	RC	VCO	Commutator
1	1	x	Preset	VCO	V_{IDLE}	Idle	Reset
0	1	x	Start	PSNS[1]	V_{IDLE}	Reset	Run
0	0	1	Run	VCO	Run	Run	Run
0	0	0	Coast	TACH	Run	Run	Run
1	0	x	Brake	VCO	V_{IDLE}	Idle	Reset

NOTE 1: PSNS is undefined in the 32H6828.

FUNCTIONAL DESCRIPTION (continued)

LOW VOLTAGE MONITOR

A precision low voltage monitor circuit is included in the 32H6827 to monitor VREF and both the+5V and +12V supplies. The monitor includes a precision voltage reference generator, VCC reset comparator, +12V reset comparator, write inhibit comparator, and associated logic.

LOW VOLTAGE MONITOR

The voltage reference circuit generates a precision voltage reference VBG at 2.493V. From VBG, it also generates V2P2 (nominally 2.175V), $V_{RETRACT}$ (nominally 0.82V), V_{IDLE} (nominally 0.1V), VLIMIT (nominally 0.1V with respect to SNSREF), and several other internal voltage and current references.

Both supply voltages are individually monitored by internal resistor dividers and then compared to V2P2. To monitor the +5V supply, the internal resistor divider output VCCTH may be connected to VCCHKL or an external resistor divider can be used for a different threshold voltage. To monitor the +12V supply, connect V12 which is the upper side of the on-chip resistor to the system +12V supply. Power supply pin VP should be isolated from the +12V supply by a blocking diode so that the spindle motor stored rotational energy may be used to hold up VP briefly during power failure. When low voltage is detected on either of supplies, $\overline{\text{FAULT}}$ is pulled low. The threshold voltage of the VCC reset comparator will be pulled to a lower value if $\overline{\text{MARGIN}}$ is asserted while $\overline{\text{FAULT}}$ is high. $\overline{\text{MARGIN}}$ allows the VCC reset comparator to be effectively disabled once power is applied.

$\overline{\text{RETR}}$ is an active low input which is gated with FAIL to force the actuator predriver into retract mode. In this retract mode, the constant voltage $V_{RETRACT}$ is applied across the motor thereby implementing velocity limiting. An external RC delay may be used between $\overline{\text{FAULT}}$ and $\overline{\text{BRAKE}}$ to defer dynamic braking until the heads are retracted. To implement deferred braking, connect a resistor from $\overline{\text{FAULT}}$ to $\overline{\text{BRAKE}}$ and a capacitor from $\overline{\text{BRAKE}}$ to ground.

A write inhibit function is provided by the low voltage monitor circuitry. When the +5V supply is out of its specified limits or +12V supply falls below its threshold, $\overline{\text{WRINH}}$ is pulled low.

Digital Inputs

To ensure a known state during system power failure, the digital inputs at $\overline{\text{DISPWR}}$, PWMIN, ADVANCE, RESET, $\overline{\text{ENABLE}}$, $\overline{\text{RETR}}$ are pulled to ground with a 20 kΩ (minimum) resistor, while the digital input at $\overline{\text{MARGIN}}$ is pulled to VCC with a 20 kΩ (minimum) resistor.

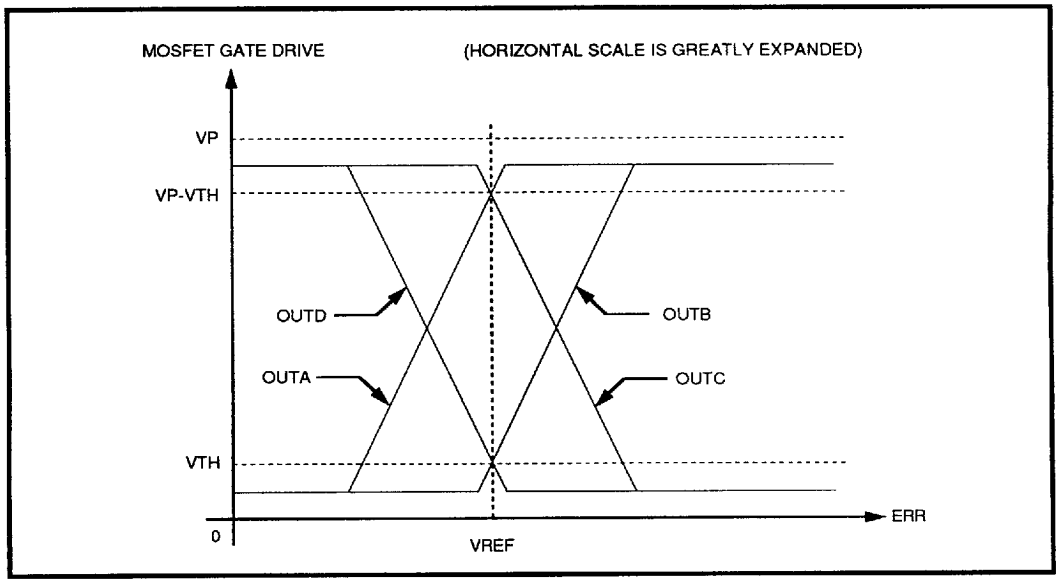


FIGURE 1: Crossover Protection

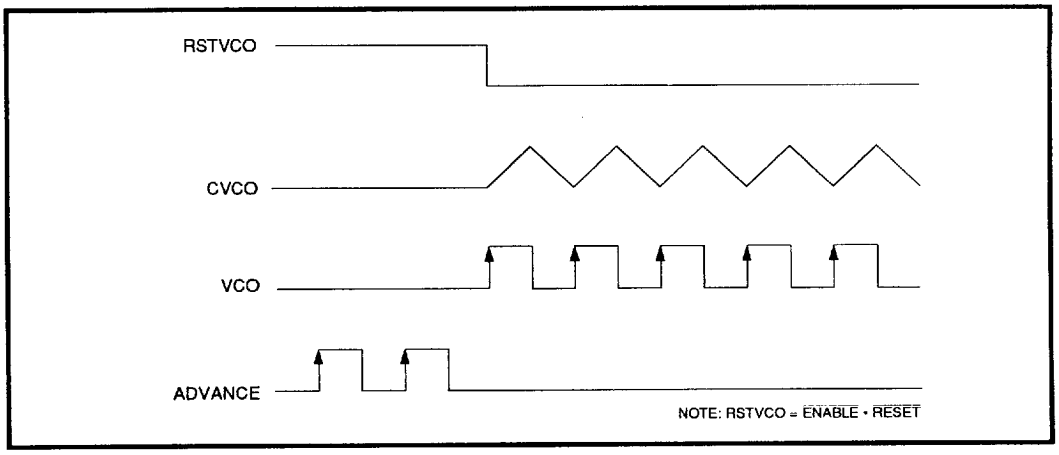


FIGURE 2: SSI 32H6827/6828 VCO Spindle Driver

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PIN DESCRIPTION

The 32H6828 is a reduced pin count version of the 32H6827. The following pins do not appear in the 6828: VBG2X, VBG, $\overline{\text{MARGIN}}$, VCCTH, VCCHKH, VCCHKL, V12, V12CHK, VPSNS, VLIMIT, SNSREF, $\overline{\text{WRINH}}$, and $\overline{\text{FAULT}}$.

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VND VNA	Ground	DIGITAL AND ANALOG GROUNDS: They are to be connected externally.
VCC	Supply	SYSTEM 5V POWER SUPPLY: Used by digital I/O circuits.
VP	Supply	THE 12V SUPPLY, DIODE BLOCKED FROM SYSTEM 12V. This is also the bridge supply for the spindle and actuator MOSFETs.

ACTUATOR PREDRIVER

VREF	I (A)	ACTUATOR VOLTAGE REFERENCE: All actuator analog signals are referenced to this voltage, except SOLS.
VLIM	I (A)	LIMITING VOLTAGE: The voltage at this pin sets the $\overline{\text{WRPROT}}$ window comparator limits. Limiting occurs when: $\lvert\text{SOUT-VREF}\rvert > (\text{VREF-VLIM})$ An internal resistor divider establishes a default value that may be externally adjusted.
ERRP	I (A)	POSITION ERROR NON-INVERTING INPUT: Non-inverting input to the loop compensation amplifier.
ERRM	I (A)	POSITION ERROR INVERTING INPUT: Inverting input to the loop compensation amplifier.
ERR	O (A)	POSITION ERROR: The loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge as follows: SE3-SE1 = 17 (ERR-VREF)
SOUT	O (A)	MOTOR CURRENT SENSE OUTPUT: This output provides a voltage proportional to the voltage drop across the external current sense resistor as follows: SOUT-VREF = 4 (SE2-SE1)
SOLS	O (A)	MOTOR CURRENT SENSE OUTPUT: This output provides a voltage equal to one half of SOUT and is referenced to VR. SOLS-VR = 0.5 (SOUT-VREF)
VR	I (A)	VOLTAGE REFERENCE: The reference for SOLS.
$\overline{\text{WRPROT}}$	O (D)	WRITE PROTECT: Active low with an on-chip 10 kΩ pullup resistor. It is asserted when SOUT exceeds the window comparator limits.
$\overline{\text{SAT}}$	O (D)	SATURATION DETECT OUTPUT: Active low with an on-chip 10 kΩ pullup resistor. It is asserted when the current flowing through the summing node at ERRM exceeds the saturation detector limits.

ACTUATOR PREDRIVER (continued)

NAME	TYPE	DESCRIPTION
SE2	I (A)	MOTOR CURRENT SENSE INPUT: Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the actuator. The inverting input of the differential amplifier is connected internally to SE1.
SE1	I (A)	MOTOR VOLTAGE SENSE INPUT: This input provides feedback to the inverting MOSFET driver amplifier and to the current sense amplifier. It is connected to the current sensing resistor that is in series with the motor. The gain to this point from ERR is: SE1-VREF = -8.5(ERR-VREF)
SE3	I (A)	MOTOR VOLTAGE SENSE INPUT: This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point from ERR is: SE3-VREF = 8.5(ERR-VREF)
OUTA OUTC	O (A)	P-FET DRIVE: Drive signal for a P-channel MOSFET connected between one side of the motor and VP.
OUTB OUTD	O (A)	N-FET DRIVE: Drive signal for an N-channel MOSFET connected between one side of the motor and ground. Crossover protection circuitry ensures that the P and N channel devices connected to the same side of the motor are never enabled simultaneously.
VBG2X	O (A)	VOLTAGE DOUBLER OUTPUT: The output of the voltage doubler.
A3P	I (A)	NON-INVERTING A3 INPUT: Positive input to A3, the uncommitted opamp.
A3N	I (A)	INVERTING A3 INPUT: Negative input to A3, the uncommitted opamp.
A3	O (A)	A3 OUTPUT: The output of A3, the uncommitted opamp.

SPINDLE PREDRIVER

P1, P2, P3	O (A)	P-CHANNEL SPINDLE FET DRIVERS: These pins are connected to the three P-channel power MOSFETs in the spindle motor power bridge.
N1, N2, N3	O (A)	N-CHANNEL SPINDLE FET DRIVERS: These pins are connected to the three N-channel power MOSFETs in the spindle motor power bridge.
RSR	Comp	SOURCE CURRENT LIMIT: An external resistor is connected between this pin and VP to set 1/20 of the peak gate current at N1, N2, N3.
ISENSE	I (A)	SPINDLE CURRENT SENSE: Connects to the high side of the spindle current sense resistor RMS.
SNSREF	I (A)	SPINDLE CURRENT SENSE REFERENCE: Connects to the low side of the spindle current sense resistor. It is normally the ground for spindle power MOSFETs.

SPINDLE PREDRIVER (continued)

NAME	TYPE	DESCRIPTION
VLIMIT	Comp	ONE SHOT THRESHOLD: Sets the threshold of the one shot. The default value of 0.1V (w.r.t. SNSREF) can be adjusted with an external resistor across VLIMIT and SNSREF.
VPSNS	I (A)	SENSE COMPARATOR INPUT: The input to the Sense comparator. The comparator output is asserted when ISENSE exceeds VPSNS.
COS	Comp	ONE SHOT CAPACITOR: Sets the time delay in the one shot. The one shot is clocked whenever the current in the spindle exceeds a limit controlled by R_{MS}.
PWMIN	I (D)	PULSE WIDTH MODULATION INPUT: Modulates the N-channel power MOSFETs to control spindle motor current.
$\overline{\text{DISPWR}}$	I (D)	DISABLE POWER: Active low, this input turns off the high and low sides of the spindle drivers. A brake command will over-ride $\overline{\text{DISPWR}}$. An internal pulldown resistor guarantees a logic low when $\overline{\text{DISPWR}}$ floats.
ADVANCE	I (D)	COMMUTATION ADVANCE: A rising edge on this pin will cause the commutator to advance whenever RESET is low. While high, ADVANCE prevents other commutation clocks from occurring.
SENSOR	O (D)	DIGITAL MUX OUTPUT: A totem pole output which is multiplexed from the VCO output, the TACH comparator output and the sense comparator output according to Table 3.
RVCO	Comp	VCO RESISTOR: Sets the frequency range of the VCO. The voltage at RVCO is forced to track RC.
CVCO	Comp	VCO CAPACITOR: Sets the frequency range of the VCO.
RC	Comp	PLL LOOP FILTER: Sets the time constant for the PLL in Run mode. In all other modes, it is connected to a DC voltage, V_{IDLE}. V_{IDLE} determines the VCO frequency at which crossover from Start to Run should occur (by lowering $\overline{\text{ENABLE}}$).
RPH	Comp	PHASE ERROR CURRENT SET: The pump current in the phase error amplifier is the sum of the VCO current (through RVCO) and the current through RPH.
PH1, PH2, PH3	I (A)	SPINDLE MOTOR TERMINALS: These pins are used to detect the phase error in the PLL. Place 1 kΩ resistors in series with each phase pin to corresponding motor winding.

LOW VOLTAGE MONITOR

NAME	TYPE	DESCRIPTION
$\overline{\text{ENABLE}}$ RESET	I (D)	MODE CONTROLS: These inputs control the spindle modes according to Table 3.
VBG	O (A)	BANDGAP VOLTAGE OUTPUT: A voltage reference output at 2.493V. It is used internally as a reference voltage in the low voltage monitor circuitry.
VCCHKH	I (A)	WRITE INHIBIT COMPARATOR INPUT: The input to the write inhibit comparator and connection to a bypass capacitor. VCC is divided down at this pin by an internal resistor divider and then compared to VBG. If VCCHKH exceeds VBG, then $\overline{\text{WRINH}}$ will be pulled low.
V12	I (A)	SYSTEM +12V SUPPLY: The upper side connection of the resistor divider for +12V reset comparator.
V12CHK	I (A)	+12V RESET COMPARATOR INPUT: The input to the +12V reset comparator and connection to a bypass capacitor. V12 is divided down at this pin by an internal resistor divider and then compared to VBG. If V12CHK falls below VBG, then a forced retract occurs.
VCCTH	Comp	VCC RESISTOR DIVIDER OUTPUT: VCC is divided down at this pin by an internal resistor divider. Typically, it is connected to VCCHKL.
VCCHKL	I (A)	VCC RESET COMPARATOR INPUT: The input to the VCC reset comparator and connection to a bypass capacitor. If VCCHKL falls below VBG, then a forced retract occurs.
$\overline{\text{MARGIN}}$	I (D)	MARGIN CONTROL INPUT: Sets the threshold voltage of VCC reset comparator. It is set high by an internal pull up resister under normal operation. If it is asserted low while $\overline{\text{FAULT}}$ is high, then the threshold voltage of the comparator will be lowered.
$\overline{\text{FAULT}}$	O (D)	POWER FAULT: Active low with an on-chip 10 kΩ pullup resistor. It is asserted when a low voltage condition is detected on either +5V or +12V supply.
$\overline{\text{WRINH}}$	O (D)	WRITE INHIBIT: Active low with an on-chip 10 kΩ pullup resistor. It is asserted when a low voltage condition is detected on either +5V or +12V supply or an excessive voltage condition is detected on +5V supply.
$\overline{\text{RETR}}$	I (D)	RETRACT: Digital active low input which must be asserted by an external circuit to force an actuator retract.
$\overline{\text{BRAKE}}$	I (A)	BRAKE: Active low input which must be pulled low by external circuitry to perform a delayed brake.
CBRAKE	Comp	BRAKE CAPACITOR: A large capacitor is connected from CBRAKE to ground to provide source voltage to the N-channel spindle MOSFETs during power fault brake.
RBK	Comp	BRAKE RESISTOR: A high value (10 Meg) resistor is connected between CBRAKE and RBK to pull up the base of the brake transistor. This pin is pulled low when $\overline{\text{BRAKE}}$ is not asserted.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING
VP	0 to 14V
VCC	0 to 7V
VREF	0 to 10V
SE1, SE2, SE3, N1, N2, N3, $\overline{\text{BRAKE}}$, CBRAKE, RBK, OUTD	0 to 15V
PH1, PH2, PH3	-2 to 15V
$\overline{\text{ENABLE}}$, RESET, PWMIN, $\overline{\text{DISPWR}}$, ADVANCE, SENSOR, $\overline{\text{SAT}}$, $\overline{\text{RETR}}$, $\overline{\text{MARGIN}}$, $\overline{\text{WRPROT}}$, $\overline{\text{FAULT}}$, $\overline{\text{WRINH}}$	0 to VCC
All other pins	0 to VP
Storage temperature	-45 to 165°C
Solder temperature: 10 sec duration	260°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VP	Normal Mode	9	12	13.2	V
	Retract/Brake Mode	3.5		14	V
VCC		4.5	5	5.5	V
VREF		4.5		7	V
VR		2	2.493	3	V
Ambient temperature		0		70	°C

DC CHARACTERISTICS

VP current				50	mA
VCC current				20	mA
V12 current				2	mA
VREF current	SE2 = VREF			2	mA
VR current	VR = 2.493V, SOUT = 2.5V w.r.t. VREF			0.5	mA

ACTUATOR PREDRIVER

A1, Loop Compensation Amplifier

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current				500	nA
Input offset voltage				±3	mV
Voltage swing	about VREF = 5V	±2			V
Common mode range V_{IL}				2	V
V_{IH}, wrt VP		-1.3			V
Load resistance	to VREF	4			kΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB

A2, Current Sense Amplifier

Input Impedance	SE1	SE1 = VREF	1.8	3.3		kΩ
	SE2	SE2 = VREF	4.8	9.6		kΩ
Input offset voltage		SE1 = SE2 = VREF			±2	mV
Output voltage swing	V_{OL}				1.4	V
V_{OH}, wrt VP			-1.3			V
Common mode range	V_{IL}				0	V
V_{IH}, wrt VP		VP ≥ 10V, VREF = 5V	-0.2			V
Load resistance		to VREF	20			kΩ
Load capacitance					100	pF
Output impedance					20	Ω
Gain (SOUT-VREF)/(SE2-SE1)			3.9	4	4.1	V/V
Unity gain bandwidth			0.5			MHz
CMRR			52			dB
PSRR			60			dB

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ACTUATOR PREDRIVER (continued)

A3 Amplifier

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current				250	nA
Input offset voltage				±2	mV
Output voltage swing V_{OL}				1.4	V
V_{OH}, wrt VP		-1.2			V
Common mode range V_{IL}				2.5	V
V_{IH}, wrt VP		-3			V
Load resistance	to VREF	10			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		150			kHz
CMRR		60			dB
PSRR		60			dB

Window Comparator

Window comparator threshold	|SOUT-VREF| rising	VREF-VLIM			V
Threshold hysteresis			50		mV
VLIM voltage	No external parts	92	94	96	%VREF
VLIM input resistance		8	15		kΩ
$\overline{\text{WRPROT}}$ delay	SOUT = VREF to VREF + 0.6V			10	µs

SOLS Output

Output voltage swing V_{OL}				1.2	V
V_{OH}, wrt VP		-2			V
Input offset voltage	SOUT = VREF			±5	mV
Load resistance	to VREF	20			kΩ
Load capacitance				100	pF
Output impedance				200	Ω
Gain (SOLS-VR)/(SOUT - VREF)		0.4875	0.5	0.5125	V/V

Voltage Doubler

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current				500	nA
Output impedance				15	Ω
Gain VBG2X/VBG	$\|I_{OUT}\| < 6$ mA, VP ≥ 10V	1.95	2	2.05	V/V
Load capacitance				0.1	µF

Saturation Detector

Threshold current	$\overline{SAT}$ falling	5	10	20	µA
Hysteresis			2		µA

Actuator MOSFET Drivers

SE3 Input impedance	to VREF	10	25		kΩ
OUTA, OUTC voltage swing	$\|I_{OUT}\| < 1$ mA	0.7		VP -1	V
OUTB, OUTD voltage swing	$\|I_{OUT}\| < 1$ mA	1		VP -1	V
VTH, crossover threshold				2	V
Slew rate, OUTA..D	CL < 1000 pF	0.5			V/µs
Crossover time	±300 mV step at ERR			7	µs
Output impedance, OUTA..D			50		kΩ
Transconductance I(OUTA..D)/(ERR-VREF)			8		mA/V
Gain (SE1-VREF)/(ERR-VREF) (SE3-VREF)/(ERR-VREF)		8	8.5	9	V/V
Retract voltage,VRETRACT	VP > 5V	0.7	0.82	1	V

VREF Monitor

VREF fail threshold	VREF falling	2.6	3.3	4	V
Hysteresis			85		mV

SPINDLE PREDRIVER

VCO (Unless otherwise specified, C_{VCO} = .01 µF, R_{VCO} = 12 kΩ)

Typical frequency		$\frac{V_{RC}}{8.8\ R_{VCO}\ C_{VCO}}$			Hz
Run Frequency	V_{RC} = 2V	1705	1950	2150	Hz
Idle Frequency	Mode = Reset	90	108	125	Hz
Reset Phase Error	$V_{RC} = V_{IDLE}$			36	deg.

SPINDLE PREDRIVER (continued)

Phase Error Amplifier (Unless otherwise specified, R_{VCO} = 12 kΩ, R_{RPH} = ∞)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VRC(V_{IDLE})	Mode = Reset		100		mV
Pump Current at RC start mode	V_{RC} = V_{IDLE}, R_{RPH} = ∞		4		µA
run mode, at speed	V_{RC} = 2V		40		µA
Source/Sink Current Mismatch	V_{RC} = 2V			5	%
PH1 Input Offset, State B	PH2 = VP, PH3 = 0	-60		60	mV
PH1 Input Offset, State E	PH2 = 0, PH3 = VP	-60		60	mV
PH2 Input Offset, State A	PH1 = VP, PH3 = 0	-60		60	mV
PH2 Input Offset, State D	PH1 = 0, PH3 = VP	-60		60	mV
PH3 Input Offset, State F	PH1 = VP, PH2 = 0	-60		60	mV
PH3 Input Offset, State C	PH1 = 0, PH2 = VP	-60		60	mV
RPH Voltage	R_{RPH} = 120 kΩ		1.2		V

Motor Current Control

ISENSE threshold (VLIMIT)		90	100	110	mV
Input impedance at VLIMIT			2.27		kΩ
One shot off time	C_{OS} = .002 µF	15	25	35	µs

Braking Circuit

$\overline{\text{BRAKE}}$ threshold	T_A = 25°C, VP = 4V	0.8	1.2	1.6	V
$\overline{\text{BRAKE}}$ VP threshold	T_A = 25°C, $\overline{\text{BRAKE}}$ = 1.6V			3.8	V
$\overline{\text{BRAKE}}$ VP threshold TCO			-7.2		mV/C°
Bias current at $\overline{\text{BRAKE}}$, RBK, CBRAKE				0.1	µA

NMOS Motor Driver Outputs (N1, N2, N3)

Source current	V_{OUT} = 4V, R_{RSR} = 50 kΩ	3		6	mA
	V_{OUT} = 4V, R_{RSR} = 100 kΩ	2		4	mA
Sink current	V_{OUT} = 4V	9		25	mA
Output Low voltage	I_{SINK} = 5 mA			1	V
Output High voltage, wrt VP	I_{SOURCE} = 0.1 mA	-2.5			V

PMOS Motor Driver Outputs (P1, P2, P3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Source current	V_{OUT} = VP-4	20			mA
Sink current	V_{OUT} = VP-4	9		25	mA
Output Low voltage	I_{SINK} = 1 mA			1.5	V
Output High voltage, wrt VP	I_{SOURCE} = 5 mA, VN = 6V	-1			V

TACH Comparator

SENSOR rising edge threshold	PH3-PH2	60	140	200	mV
SENSOR falling edge threshold	PH2-PH3	60	140	200	mV

Sense Comparator

Input voltage offset				±10	mV

LOW VOLTAGE MONITOR

VBG Output

Output voltage	VBG shorted to VR No other resistive loads	2.453	2.493	2.533	V
Load capacitance				0.1	µF

VCC Reset Comparator ($\overline{\text{MARGIN}}$ = High)

Input bias current				200	nA
Threshold voltage	VCCHKL falling	2.13	2.175	2.22	V
Hysteresis		15	20	25	mV

VCC Reset Comparator ($\overline{\text{MARGIN}}$ = Low)

Threshold voltage	VCCHKL falling	1.70	1.85	2	V

VCC Reset Comparator (VCCTH shorted to VCCHKL, $\overline{\text{MARGIN}}$ = High)

Threshold voltage	VCC falling	4.26	4.35	4.44	V
Hysteresis		30	40	50	mV
Input resistance at VCCHKL			3.45		kΩ

ELECTRICAL SPECIFICATIONS (continued)

VCC Reset Comparator (VCCTH shorted to VCCHKL, $\overline{\text{FAULT}}$ = High, $\overline{\text{MARGIN}}$ = Low)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Threshold voltage	VCC falling	3.40	3.70	4	V

VCC Write Inhibit Comparator ($\overline{\text{MARGIN}}$ = High)

Threshold voltage	VCC rising	5.64	5.82	6	V
Hysteresis		60	80	100	mV
Input resistance at VCCHKH			3.45		kΩ

+12V Reset Comparator ($\overline{\text{MARGIN}}$ = High)

Threshold voltage	V12 falling	9.20	9.50	9.80	V
Hysteresis		60	80	100	mV
Input resistance at V12CHK			3.45		kΩ

DIGITAL I/O

Digital Input ($\overline{\text{ENABLE}}$, RESET, PWMIN, $\overline{\text{DISPWR}}$, ADVANCE, $\overline{\text{RETR}}$)

Input voltage	V_{IL}		0.8			V
	V_{IH}				2	V
Input bias current, I_{IH}		V_{IN} = 4V			200	µA
Open circuit voltage					0.4	V

Digital Input ($\overline{\text{MARGIN}}$)

Input voltage	V_{IL}		0.8			V
	V_{IH}				2	V
Input bias current, I_{IH}		V_{IN} = 0.5V, VCC = 4.5V			200	µA
Open circuit voltage			2.4			V

Digital Output (SENSOR)

Output voltage	V_{OL}	I_{SINK} = 1 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 1 mA	-1			V

Digital Output ($\overline{FAULT}$)

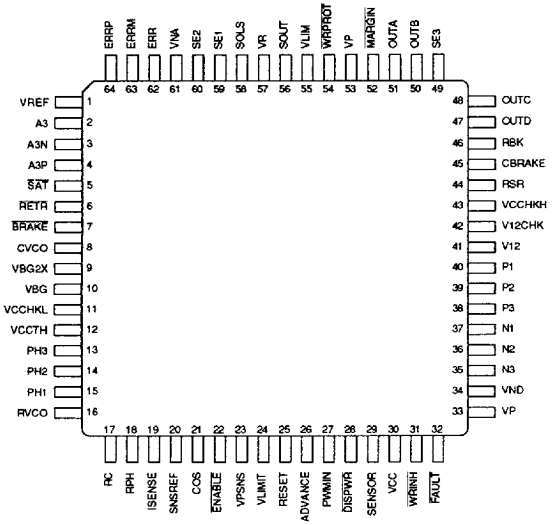
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	V_{OL}	I_{SINK} = 8 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-1.4	-1	-0.6	V

Digital Output ($\overline{WRIHN}$, $\overline{SAT}$, $\overline{WRPROT}$)

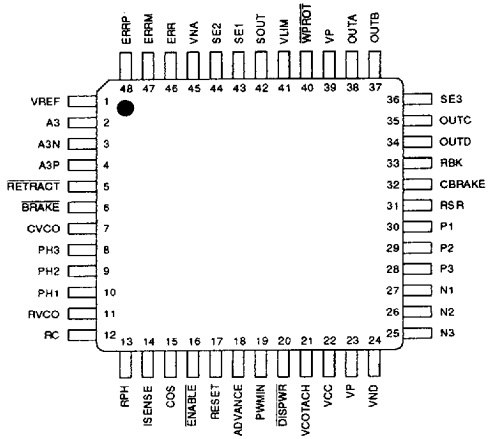
Output voltage	V_{OL}	I_{SINK} = 1 mA			0.4	V
	V_{OH}, wrt VCC	I_{SOURCE} = 0.1 mA	-1.4	-1	-0.6	V

SSI 32H6827/6828
Servo and Spindle Predriver

PACKAGE PIN DESIGNATIONS
(Top View)



SSI 32H6827
64-Lead TQFP



SSI 32H6828
48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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