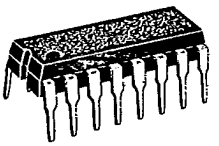
MN4044B/MN4044BS

Quad R/S Latches

■ Description

The MN4044B/S have built-in quad independent R/S flip-flops. They are suitable for 4-bit data processing due to the combination of NAND gates.
Four outputs can be high impedance by common input (EO) = L regardless of the latch contents.
These are equivalent to MOTOROLA MC14044 and RCA CD4044B.

P-3



16-Pin • Plastic DIL Package

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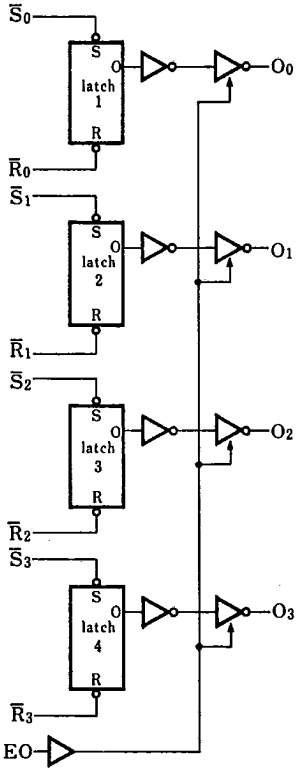
16-Pin • Panaflat Package (SO-16D)

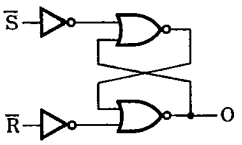
■ Truth Table

Input			Output
EO	S	R	O
L	×	×	Z
H	L	H	H
H	×	L	L
H	H	H	latch

Note) X : don't care
Z : high impedance

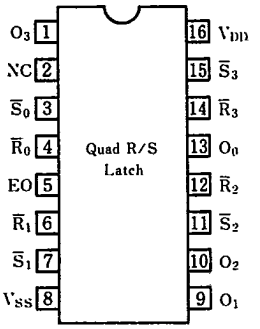
■ Logic Diagram





(One latch)

Pin Configuration



Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

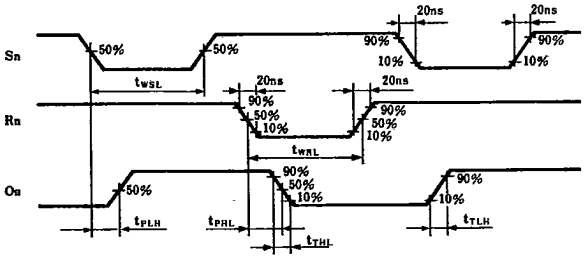
DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5 V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or15V		—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}		—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}		—	1.6	—	1.6	—	12	

■ Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{Rn}$→On (H→L)	5	t_{PHL}	—	90	270	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time $\overline{Sn}$→On (L→H)	5	t_{PLH}	—	90	270	ns
	10		—	40	120	
	15		—	30	90	
High Level Output Disable Time EO→On (H)	5	t_{PHZ}	—	50	150	ns
	10		—	30	90	
	15		—	25	75	
Low Level Output Disable Time EO→On (L)	5	t_{PLZ}	—	30	90	ns
	10		—	25	75	
	15		—	20	60	
High Level Output Enable Time EO→On (H)	5	t_{PZH}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Low Level Output Enable Time EO→On (L)	5	t_{PZL}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Low Level Minimum Sn Pulse Width	5	t_{WSL}	45	15	—	ns
	10		30	10	—	
	15		24	8	—	
Low Level Minimum Rn Pulse Width	5	t_{WRL}	45	15	—	ns
	10		30	10	—	
	15		24	8	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



Item	S	R	S.W.	O
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}	A
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}	B
t_{PZH}	V_{DD}	V_{SS}	V_{SS}	A
t_{PZL}	V_{SS}	V_{DD}	V_{DD}	B