L63500
ARINC 629
Terminal Device (DATAC)
Preliminary

Introduction

The L63500 data bus terminal controller is specified in ARINC 629. Primarily developed to function as a bus interface terminal in a multiple transmitter data bus, the L63500 simplifies I/O design and allows flexibility in the physical layout of user systems. In addition, it minimizes problems associated with centralized data communication systems – loss of all communication, application complexity, etc. The L63500 is an ideal device for application in aircraft avionic "fly by wire" systems, factory automation systems, and other control systems requiring high reliability and performance. The L63500 is currently available in a 180-pin ceramic pin grid array. A surface mountable leaded chip carrier version is under development. Both package options are available processed to the requirements of Mil-Std-883 with operation guaranteed over the military 125°C/ -55°C temperature range.

During operation, bus access control is distributed among all terminals and decisions concerning transmission go-ahead are determined autonomously. The data bus access protocol is Carrier Sense Multiple Access-Clash Avoidance (CSMA-CA) which enables equal priority access for all terminals even during overload conditions. Under normal operating conditions the terminals transmit at a fixed update rate (periodic). When overload conditions exist the terminal transmits continuously (aperiodic) utilizing 100% of the bus.

Transmitted information (messages) is (are) formatted by the scheduler. Each message consists of a set of wordstrings which are stored in the transmit personality PROM. In addition, the wordstrings contain labels which provide subsystem identification. Once the transmitted information is received by another terminal, the serial data is decoded and tested for proper format. The label of each wordstring is compared to the information stored in the receive personality PROM. If correlation between the personality and transmitted data exists, then the subsystem will initiate the proper I/O activity. If no correlation exists the system will remain idle.

During transmission the receiver acts as a data monitor. Erroneous transmissions are terminated and after seven consecutive errors the transmitter is disabled.

Features

- ARINC 629 compliant
- Boeing certified
- Autonomous bus control
- Manchester II biphase coded serial data
- 2 megabit data rate
- Direct memory access capability
- Periodic and aperiodic protocol modes
- Provides transmit and receive interrupt vectors
- Automatic shutdown on error of transmitted data
- Data validation based on format and parity
- Voltage, current and fiber optic transmission media supported
- CMOS 0.9-micron channel length (1.5-micron gate length) technology
- Low power dissipation
- +5 V supply voltage

September 1990

Order Number L63500

Block Diagram

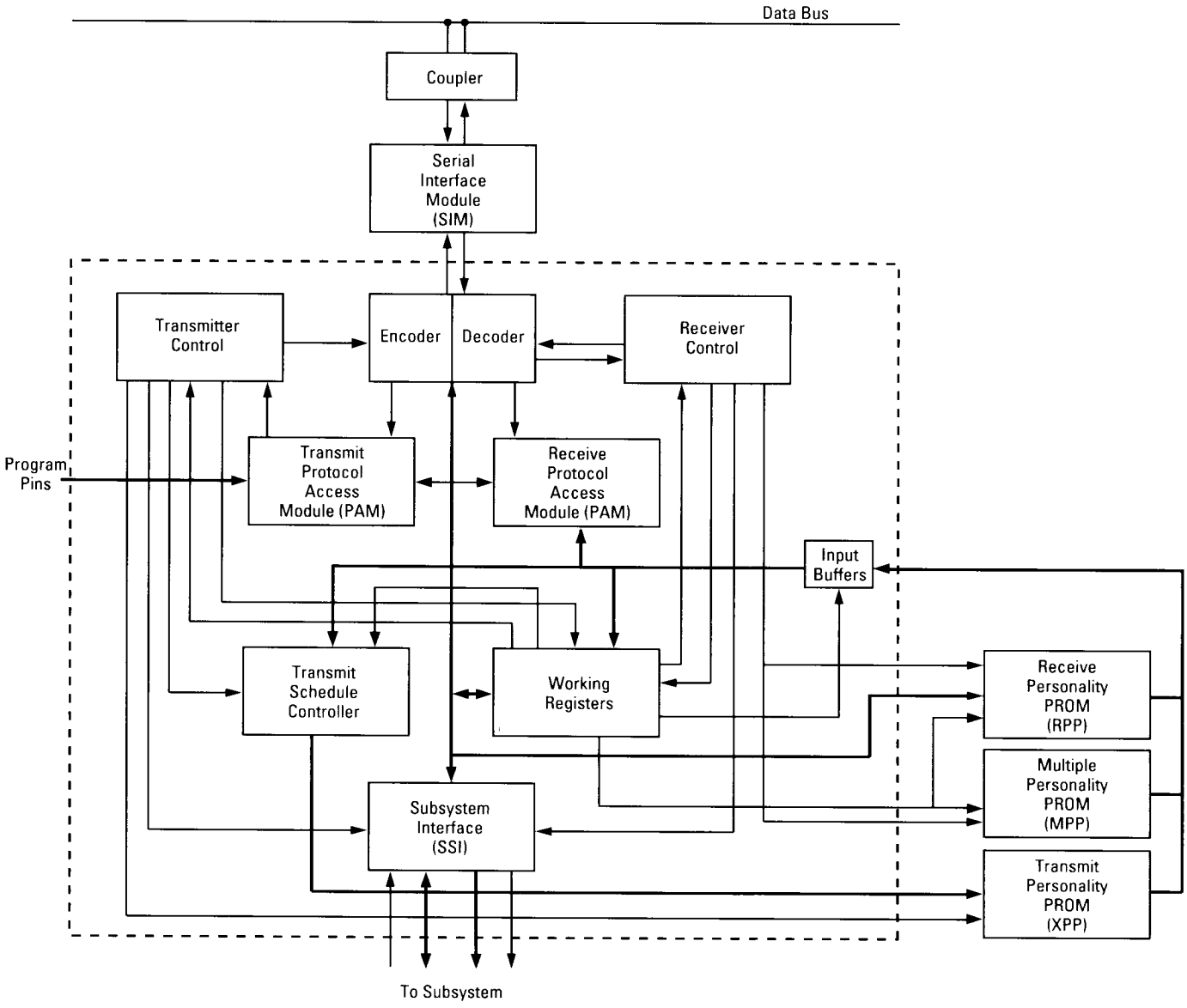


Figure 1. DATAC Functional Block Diagram

General Specifications

Parameter	Value
Bus capacity	2 MHz or 100,000 words per second
Message length	31 word strings per message
String length	256 words per word string
Word length	16 bits
Label word base label label extension	16 bits 12 bits 4 bits
Address word Interrupt vector	16 bits 15 bits
Maximum bit rate (using 32 MHz clk)	2 M bits per second
Maximum number of terminals on bus (current mode)	120 terminals

Pin Listing and Description

AD0 – ADF
Address/Data Lines
Multiplexed address/bidirectional data bus with 3-state inputs/outputs. ADF is the most significant bit.

AE
Address Enable
Enables address/data lines when input is low.

ALT
Alternate
Enables alternate transmission schedule when low. Pin is tied high for normal application. Mandatory input.

A00 – A0F
Steady Address Lines
These lines provide interrupt vectors and allow direct control of local latches. A0F is the most significant bit.

ASO
Address Strobe
Active low when address is valid on lines A00 – A0F.

B00 – B11
Bus One
Personality PROM address lines. Mandatory output. B11 is the most significant bit.

B200 – B207
Bus Two
Personality PROM data lines. Mandatory input. B207 is the most significant bit.

BI
Block/Independent
Selects transmit schedule format. BI is tied high for block schedule format and low for independent module format. Mandatory input.

BSAO
Bus Acknowledge Output
Provides handshake to subsystem upon completion of memory access through bus request (BUSR) and bus acknowledge (BUSA).

BSL
Byte Select
Addresses the multiple personality PROM when direct system programming is used.

BUSA
Bus Acknowledge
Allows the terminal to commence a read or write cycle when input is low. Mandatory input.

BUSR
Bus Request
Active low when the terminal is ready to utilize the bidirectional address/data bus.

BUSQ
Bus Quiet
Indicates bus quiet state (Inter-string gaps included). Active high.

CIDB0 – CIDB3
Channel Identification Buffered
Multiple personality PROM address lines. CIDB3 is the most significant bit.

CID0 – CID3
Channel Identification
Hardwired inputs used as channel identification codes when multiple versions of the terminal exist on the bus.

CLRX
Clear X-Counter
Indicates when x-counter of the transmit scheduler is cleared. Active low.

Pin Listing and Description (Continued)

CMD
C-Mode
When the output is low, this indicates that the chip is operating in C-mode (i.e., all terminals synchronized to a common clock, resulting in a fully synchronous operation).

CMDP
C-Mode Pulse
Maintains C-mode operation when input is pulsed low (CMDP < 2TI). For normal applications CMDP is high. Mandatory input.

CS
Chip Select
Enables access to internal registers. Active low.

DSO
Data Strobe Output
Output used to strobe data in and out of the subsystem. An active data strobe indicates stable data on lines AD0 – ADF. Mandatory output. Active low.

ENC0 – ENC4
Test Inputs
Used as test inputs with all inputs normally high. Mandatory inputs.

EX0 – EX3
Label Extension
A portion of the address to the multiple personality PROM used to provide channel identification. EX3 is the most significant bit.

EXST
Extension Strobe
Strobe used to clock label extension into external latch. Active low.

GA
Go Ahead
Grants permission to transmitter to begin transmission of new message. Active high.

GND
Ground

IOCK
I/O Clock
Convenience clock for signal synchronization of subsystem interface handshake operations (square wave).

IXTR
I Transmit
Test output indicating that the transmitter is active. Active low.

LDST
Load Strap
Indicates the loading of TI, TG and SG parameters. Active low.

MAFS
Major Frame Sync
Timing initialization input during C-mode operation. During normal operation input is high. Mandatory input.

MCS
Multiple personality PROM Chip Select
Active low.

MFG0 – MFG3
Manufacturer Identification for LSI Logic is 1010.
MFG3 is the most significant bit.

MIFS
Minor Frame Sync
Initiates minor message frame in C-mode operation. MIFS is high during normal operation. Mandatory input.

OP0 – OP6
Offset Pointer
Multiple personality PROM address lines.

PWRS
Power-Up Reset
Initializes essential circuits on power-up. Normally high. Active low. Mandatory input. See figure 2.

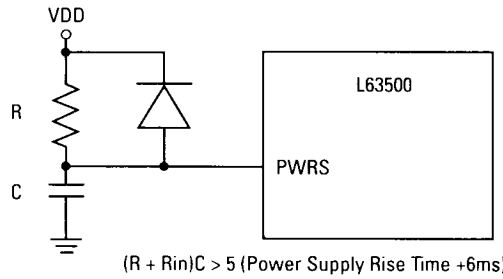


Figure 2. Reset Circuit

RCS
Receive Personality PROM Chip Select
Mandatory output. Active low.

RCT0 – RCT7
Receiver Program Counter
Outputs indicating the state of the internal receive counter (built-in self test).

Pin Listing and Description (Continued)

RERF
Receive Error Flag
Indicates that a receive error has occurred and the wordstring was truncated. A low output indicates an error has occurred.

RICK
Receive Input Clock
Receiver oscillator input (32 MHz). Mandatory input.

RIVS
Receive Interupt Vector Strobe
Interrupt vectors presented on address lines A00 – A0F. Active low.

ROCK
Receive Output Clock
This is the buffered output of RICK (not inverted).

RPH1
Receive Output Clock
Clocks the receiver controlled state machine. Normally not needed in system design and development.

RW0
Read/Write Output
Determines direction of data flow to and from the subsystem. Essential input/output.

RXCK
Receive Clock
Decoder clock used to shift the manchester bit system. Adjustable in phase depending on incoming data.

RXI
Receiver Differential Serial Data Input (POS)
Mandatory input.

RXN
Receiver Differential Serial Data Input (NEG)
Mandatory input.

RZ0 – RZ2
Receive Z-Vector
Receive personality PROM lines. Mandatory output. RZ2 is the most significant bit.

SG0 – SG1
Sync Gap
This is a 2-bit strap for the SG parameter in the access protocol. The time duration of the selected SG can be computed from the TG equation (see TG0 – TG6). SG must be greater than any TG on the bus. Mandatory input. SG1 is the most significant bit.

Equivalent TG Length	SG	
	SG1	SG0
16	0	0
32	0	1
64	1	0
127	1	1

STAC
String Active
Indicates that the device is actively transferring a string to or from the subsystem. Active low.

TG0 – TG6
Terminal Gap
Seven-bit terminal gap input for transmission. Mandatory input. TG6 is the most significant bit.

$$TG = [3.375 + (2)(\text{binary value})][\frac{16}{f_{clk}\ (MHz)}]\mu sec$$

TI0 – TI6
Transmit Interval
Seven-bit transmit interval input for transmission. Mandatory input. TI6 is the most significant bit.

$$TI = (\text{binary value} + 1.001125)(\frac{16}{f_{clk}\ (MHz)})\ msec$$

TXE
Transmitter Enable
Stops transmission when the transmit counter receives seven consecutive transmit error flags (XERF). Active high.

TXHB
Transmitter High Impedance Bus
When output is low the data is on the bus. May be used to enable drivers.

TXN
Transmitter Differential Serial Output (POS)
Mandatory output.

TX0
Transmitter Differential Serial Output (NEG)
Mandatory output.

Pin Information and Description (Continued)

VDD
Power Supply
VDD = + 5 V

WAIT
Extends the duration of the read and write cycles when the input is low. For normal applications wait is set high. Mandatory input.

1WAT
One Wait
Extends the duration of the read and write cycles by one wait cycle when input is tied low. Mandatory input.

XCS
Transmit Personality PROM Chip Select
Mandatory output. Active low.

XERF
Transmit Error Flags
Indicates that an error has occurred during transmission. The monitor truncates the message when transmission error is detected. Active low.

XICK
Transmit Clock Input
Transmitter oscillator input. Mandatory input.

XIVS
Transmit Interrupt Vector Strobe
Indicates that a valid transmit interrupt vector is present on the address lines (A00 – A0F). Active low.

XPH1
Transmit Phase 1 Clock Output

XX0 – XX4
Transmit Y-Vector
Transmit personality PROM address lines. Mandatory output. XX4 is the most significant bit.

XY0 – XY4
Transmit Y-Vector
Transmit personality PROM address lines. Mandatory output. XY4 is the most significant bit.

XZ0 – XZ4
Transmit Z-Vector
Transmit personality PROM address lines. Mandatory output. XZ4 is the most significant bit.

Power Dissipation

Parameter	Value
Number of gates	26,508
Number of gates switching each cycle	4,639
Dissipation/gate/MHz (μW)	12
Total core dissipation/MHz (mW)	56
Number of available I/O buffers	256
Percentage of I/O buffers utilized (%) as outputs	46.1
Number of I/O buffers utilized as outputs	118
Number of I/O buffers switching each cycle (20%)	12
Dissipation/output buffer/MHz/pF (μW)	25
Output capacitive load (pF)	50
Dissipation/output buffer/MHz (mW)	1.25
Total output buffer dissipation/MHz (mW)	32.5
Total dissipation/MHz (mW)	68
Total dissipation at 16 MHz clock speed (mW)	1,088
Total dissipation at 32 MHz clock speed (mW)	2,176

Operating Characteristics

Absolute Maximum Rating (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VI	-0.3 to VDD ± 0.3	V
DC input current	II	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range Military	TA	-55 to +125	°C
Industrial	TA	-40 to +85	°C
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V ± 5% ambient temperature over the specified temperature range(1)

Symbol	Parameter	Condition			Min	Typ	Max	Unit
VIL	Voltage input LOW TTL Inputs						0.8	V
VIH	Voltage input HIGH TTL inputs, commercial temperature range				2.0			V
	TTL inputs, military and industrial temperature range				2.25			V
VT+	Schmitt trigger, positive-going threshold					3.0	4.0	V
VT-	Schmitt trigger, negative-going threshold				1.0	1.5		V
	Hysteresis, Schmitt trigger	VIL to VIH VIH to VIL			1.0	1.5		V
IIN	Inputs with pullup resistors(5)	VIN = VSS			-130	-45	-15	µA
VOH (TTL)	Voltage output HIGH Type B4		Commercial	Military				
		IOH =	-4 mA	-4 mA				
VOL (TTL)	Voltage output LOW Type B4		Commercial	Military				
		IOL =	4 mA	4 mA				
IOZ	3-State output leakage current	VOH = VSS or VDD			-10	±1	10	µA
IOS	Output short circuit current(1)	VDD = Max, VO = VDD VDD = Max, VO = 0 V			20 -10	65 -45	130 -130	mA mA
IDD	Quiescent supply current	VIN = VDD or VSS						
CIN	Input capacitance	Any input(3)				2		pF
COUT	Output capacitance	Any output(4)				4		pF

Notes:
1. Military temperature range is -55°C to +125°C, ±10% power supply. Commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Not applicable to assigned bidirectional buffer (excluding package).
4. Excluding package.
5. All L63500 inputs have internal pullup resistors.

Pinout and Package Information

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	XX2	XY1	XY2	B207	B204	B201	B00	B02	B03	B05	B08	B11	XZ1	XZ2	TXHB
P	XX1	GND	XX3	XY3	B206	B203	ENC1	B01	B04	B07	B10	XZ0	TXN	GND	IOCK
N	TI0	XX0	GND	XX4	XY4	B205	B200	GND	ENC2	B09	XPH1	TXO	GND	BSAO	XICK
M	TI3	TI1	GA	VDD	XY0	ENC0	B202	VDD	B06	IXTR	XIVS	VDD	DSO	RWO	BUSQ
L	SG1	TI5	TI2	CS				MFG3				ASO	BUSR	EX0	EX2
K	TG6	ENC4	TI6	TI4								RXCK	EX1	EX3	MAFS
J	TG2	TG3	TG4	TG5								ALT	BI	PWRS	RXI
H	TG1	CMDP	TG0	SG0	MFG2			Bottom View			MFG0	BUSA	WAIT	RXN	1WAT
G	RPH1	CMD	STAC	RCT7								AOC	AOD	AOE	AOF
F	CLRX	RCT6	RCT4	RCT1								AO6	AO8	AOA	AOB
E	RCT5	RCT3	RCT0	XCS				MFGI				AOO	AO4	AO7	AO9
D	RCT2	RICK	MCS	VDD	TXE	CID0	CIDB2	VDD	OP6	AD5	ADA	VDD	AO1	AO3	AO5
C	RCS	ROCK	GND	RERF	RZ2	CID3	MIFS	GND	AE	AD2	AD6	ADB	GND	ADF	AO2
B	EXST	GND	RIVS	RZ1	CID2	CIDB3	CIDB0	OP2	OP4	AD0	AD3	AD7	ADC	GND	ADE
A	XERF	LDST	RZO	CID1	BSL	CIDB1	OP0	OP1	OP3	OP5	AD1	AD4	AD8	AD9	ADD

Locating Pin

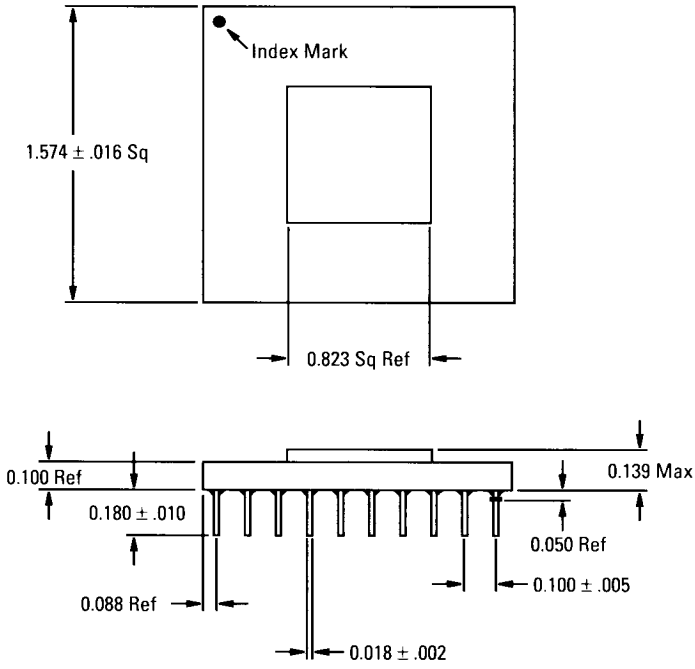
Figure 3. 180-Pin Ceramic Pin Grid Array (CPGA) Pin Diagram

Pinout and Package Information
(Continued)

Table 1. 180-Pin Ceramic Pin Grid Array (CPGA) Pin List

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B10	AD0	P11	B10	N8	GND	G3	STAC
A11	AD1	R12	B11	N13	GND	H3	TG0
C10	AD2	N7	B200	P2	GND	H1	TG1
B11	AD3	R6	B201	P14	GND	J1	TG2
A12	AD4	M7	B202	P15	IOCK	J2	TG3
D10	AD5	P6	B203	M10	IXTR	J3	TG4
C11	AD6	R5	B204	A2	LDST	J4	TG5
B12	AD7	N6	B205	K15	MAFS	K1	TG6
A13	AD8	P5	B206	D3	MCS	N1	TI0
A14	AD9	R4	B207	H11	MFG0	M2	TI1
D11	ADA	J13	BI	E8	MFG1	L3	TI2
C12	ADB	N14	BSA0	H5	MFG2	M1	TI3
B13	ADC	A5	BSL	L8	MFG3	K4	TI4
A15	ADD	H12	BUSA	C7	MIFS	L2	TI5
B15	ADE	M15	BUSQ	A7	OP0	K3	TI6
C14	ADF	L13	BUSR	A8	OP1	D5	TXE
C9	AE	B7	CIDB0	B8	OP2	R15	TXHB
J12	ALT	A6	CIDB1	A9	OP3	P13	TXN
E12	A00	D7	CIDB2	B9	OP4	N12	TXO
D13	A01	B6	CIDB3	A10	OP5	D4	VDD
C15	A02	D6	CID0	D9	OP6	D8	VDD
D14	A03	A4	CID1	J14	PWRS	D12	VDD
E13	A04	B5	CID2	C1	RCS	M4	VDD
D15	A05	C6	CID3	E3	RCT0	M8	VDD
F12	A06	F1	CLRX	F4	RCT1	M12	VDD
E14	A07	G2	CMD	D1	RCT2	H13	WAIT
F13	A08	H2	CMDP	E2	RCT3	E4	XCS
E15	A09	L4	CS	F3	RCT4	A1	XERF
F14	A0A	M13	DSO	E1	RCT5	N15	XICK
F15	A0B	M6	ENC0	F2	RCT6	M11	XIVS
G12	A0C	P7	ENC1	G4	RCT7	N11	XPH1
G13	A0D	N9	ENC2	C4	RERF	N2	XX0
G14	A0E	K2	ENC4	D2	RICK	P1	XX1
G15	A0F	L14	EX0	B3	RIVS	R1	XX2
L12	AS0	K13	EX1	C2	ROCK	P3	XX3
R7	B00	L15	EX2	G1	RPH1	N4	XX4
P8	B01	K14	EX3	M14	RWO	M5	XY0
R8	B02	B1	EXST	K12	RXCK	R2	XY1
R9	B03	M3	GA	J15	RXI	R3	XY2
P9	B04	B2	GND	H14	RXN	P4	XY3
R10	B05	B14	GND	A3	RZ0	N5	XY4
M9	B06	C3	GND	B4	RZ1	P12	XZ0
P10	B07	C8	GND	C5	RZ2	R13	XZ1
R11	B08	C13	GND	H4	SG0	R14	XZ2
N10	B09	N3	GND	L1	SG1	H15	1WAT

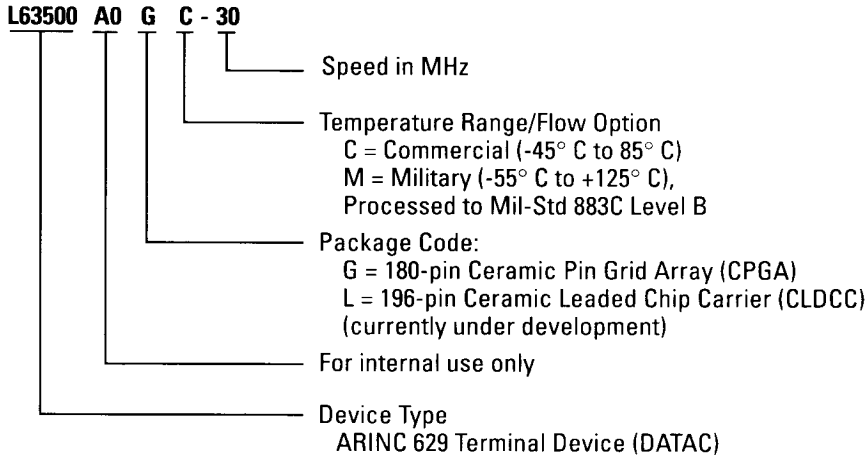
Pinout and Package Information
(Continued)



Notes:
1. Ceramic packages meet Mil-Std-38510, Revision H.
2. Controlling dimension — inch.

Figure 4. 180-Pin Ceramic Pin Grid Array (CPGA) Mechanical Drawing

Ordering Information



LSI LOGIC

L63500 Preliminary Data Sheet Errata

Page 6: $XZ0\text{-}XZ_4$ should read XZ0-XZ2
with XZ2 being the most significant bit instead of XZ4

Power Dissipation:

Add Note 1: LSI Logic power analysis and simulation tools show a typical power-dissipation of 450 milliwatts.

Page 8: Add Note 1: Pin E4(XCS)VIS internally connected to Pin E5 (the locating pin). Do not electrically connect or ground the locating pin.

Page 11: C=Commercial (-45°C to 85°C) should read
C=Commercial (0°C to 70°C)