8BIT 30MSPS ADC BW1237X

GENERAL DESCRIPTION

The BW1237X is a CMOS 8-bit A/D converter for video applications. It is a three-stage pipelined A/D converter which consists of sample-and-hold circuit, two multiplying DACs, and three flash ADCs.
The maximum conversion rate of BW1237X is 30MSPS and supply voltage is 2.0V single.

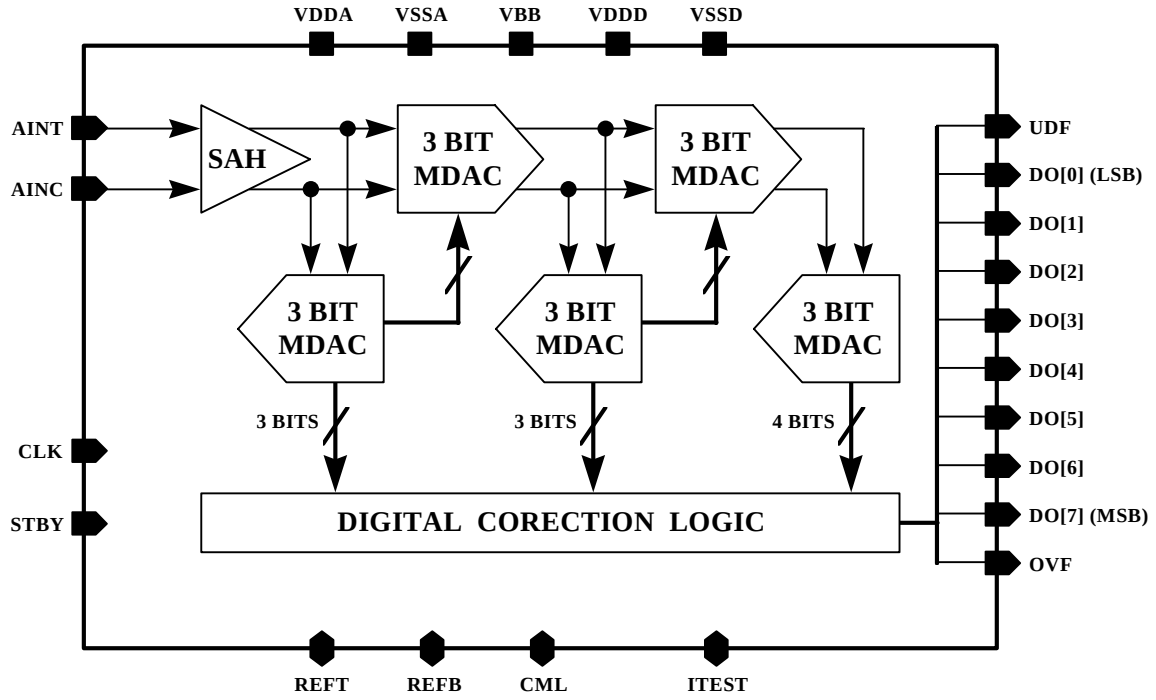
FEATURES

- **Process : CMOS**
- **Resolution : 8Bit**
- **Maximum Conversion Rate : 30MSPS**
- **Power Supply : 2.0V Single**
- **Power Consumption : 40mW**
- **Differential Linearity Error : ±0.3 LSB (Typ)**
- **Integral Linearity Error : ±0.5 LSB (Typ)**
- **Sample and Hold Function Implemented**

TYPICAL APPLICATIONS

- Multi-media Applications
- Frame-grabber Scanner
- Camcorder
- Digital Video (TV/VCR)
- Broadcasting and Studio Equipments.
- Medical Electronics (ultra-sound and imaging)
- High Speed Instruments (digital scope, radar)

FUNCTIONAL BLOCK DIAGRAM



CORE PIN DESCRIPTION

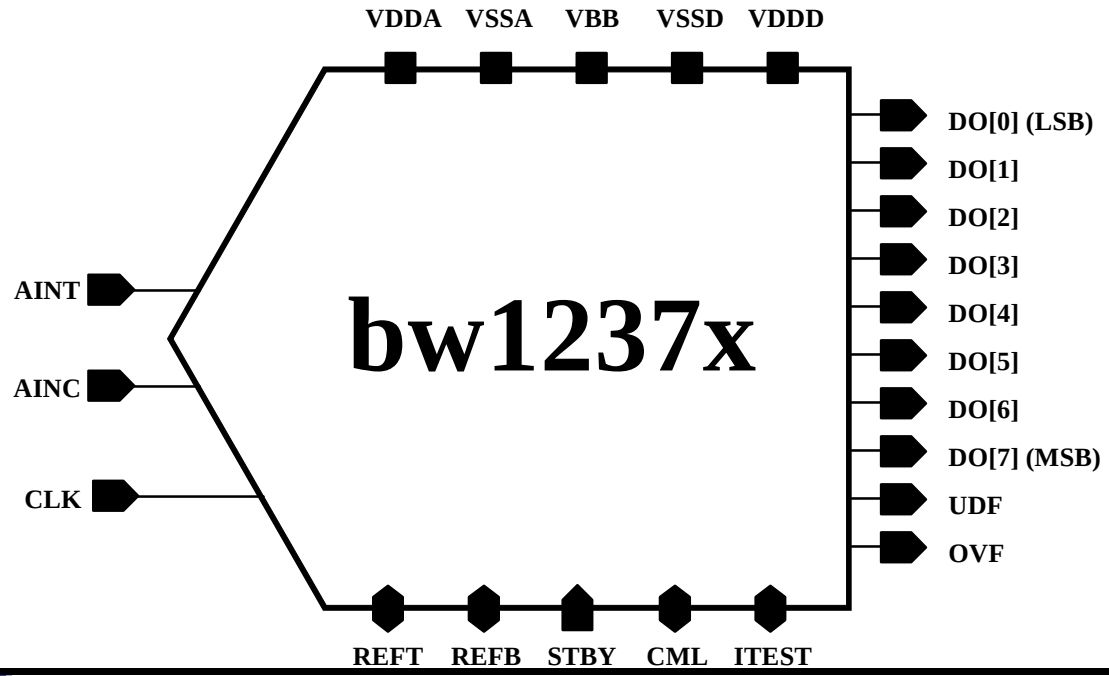
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
REFT	AB	poa_bb	+1.1V Reference Top Bias.
REFB	AB	poa_bb	+0.5V Reference Bottom Bias.
CML	AB	poa_bb	Internal Bias (Test Pin).
VDDA	AP	vdda	+2.0V Analog Power.
VBB	AG	vbba	Sub Bias.
VSSA	AG	vssa	Analog Ground.
AINT	AI	piar10_bb	Analog Input. Input Span : 0.0V ~ 1.2V
AINC	AI	piar10_bb	Analog Input. Input : Analog Ground
ITEST	AB	poa_bb	Open (Use Internal Bias)
STBY	DI	picc_bb	High (Power Saving Standby Mode) Low (Normal Operation)
CLK	DI	picc_bb	Clock Input.
DO[7:0]	DO	pot2_bb	Digital Output.
UDF	DO	pot2_bb	UnderFlow Indication.
OVF	DO	pot2_bb	OverFlow Indication.
VSSD	DG	vssd	Digital Ground.
VDDD	DP	vddd	+2.0V Digital Power.

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to 4.5	V
Analog Input Voltage	AINT	-0.3 to VDD+0.3	V
Digital Input Voltage	CLK	-0.3 to VDD+0.3	V
Digital Output Voltage	V_{OH}, V_{OL}	-0.3 to VDD+0.3	V
Reference Voltage	REFT, REFB	-0.3 to VDD+0.3	V
Storage Temperature Range	T_{stg}	-45 to 125	°C

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDA - VSSA VDDD - VSSD	1.95	2.0	2.4	V
Supply Voltage Difference	VDDA - VDDD	-0.1	0.0	0.1	V
Reference Input Voltage	REFT REFB	- -	1.1 0.5	- -	V
Analog Input Voltage Positive Port	AINT	0.0	-	1.2	V
Analog Input Voltage Negative Port	AINC	-	0.0	-	V
Operating Temperature	T_{opr}	0	25	70	°C

NOTES

1. It is strongly recommended that all the supply pins (VDDA, VDDD, VDDP) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	-	-	8	-	Bits	-
Reference Current	IREF	-	1	-	mA	-
Differential Linearity Error	DLE	-	±0.3	±0.4	LSB	AINT : 0.0V ~ 1.2V (Ramp Input) AINC : 0.0V (GND) F_s : 1MHz
Integral Linearity Error	ILE	-	±0.5	±0.7	LSB	
Bottom Offset Voltage Error	EOB	-	±2.5	±4	LSB	EOB = AIN(0,1) - REFB
Top Offset Voltage Error	EOT	-	±1.5	±2	LSB	EOT = REFT - AIN(254,255)

NOTES

1. Converter Specifications (unless otherwise specified)
   VDDA=2.0V VDDD=2.0V
   VSSA=GND VSSD=GND
   REFT=1.1V REFB=0.5V
   Ta=25°C
2. TBD : To Be Determined

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Conversion Rate	F_s	30	-	34	MSPS	AINT : 1MHz Sine Waveform (source resolution ≥ 10bit)
Dynamic Supply Current	I_s (IREF)	-	20 (0.94)	20.5	mA	I_s = I(VDDA) + I(VDDD) + IREF F_s : 30MHz
Signal to Noise Distortion Ratio (SNDR)	SNDR	40	44	-	dB	AIN : 1MHz (Sine Input) F_s : 30MHz
Total Harmonic Distortion (THD)	THD	50	56	-	dB	AIN : 1MHz (Sine Input) F_s : 30MHz

FUNCTIONAL DESCRIPTION

1. BW1237X is a three step A/D Converter comprising three flash ADC each of which yields 3, 3 and 4 bits and two multiplying DAC. The N-bit flash ADC is composed of 2^n latching comparators, and multiplying DAC is composed of N+2 capacitors and a fully-differential amplifier.

2. BW1237X operates as follows. During the first "L" cycle of external clock the analog input data is tracked and sampled, and the input is held from the rising edge of the external clock, which is fed to the first 3-bit flash ADC, and the first multiplying DAC (MDAC). The first MDAC reconstructs a voltage corresponding to the first 3-bit flash ADC's output, and finally amplifies the residue voltage which is the voltage difference between the output of the first MDAC and the reconstructed voltage by the gain of 2^2. The second 3-bit flash ADC, and MDAC operate as the same manner and finally amplifies a residue voltage by 2^2. The third 4-bit flash ADC converts the output of the second MDAC and feed the result to the Digital Correction Logic (DCL).

3. BW1237X has the error correction scheme, which handles the offset error which stems from the mismatch between the first, second and third flash ADC's comparator.

MAIN BLOCK DESCRIPTION

1. SAH

SAH(sample and hold) is the circuit that samples the analog input signal and holds that value until next sample-time. It is required that the difference between the analog input signal and the output signal be as small as it can be. This SAH consists of fully differential op amp, switching transistors. and sampling capacitors. The sampling clocks are non-overlapping clocks(Q1, Q2) and sampling capacitor is 1.4pF. SAH uses its own bias to avoid interference of any other circuit. SAH amp is designed to have open-loop dc gain higher than 80dB and phase margin higher than 60 degree. Its input block is designed to be the rail-to-rail architecture using complementary differential pair.

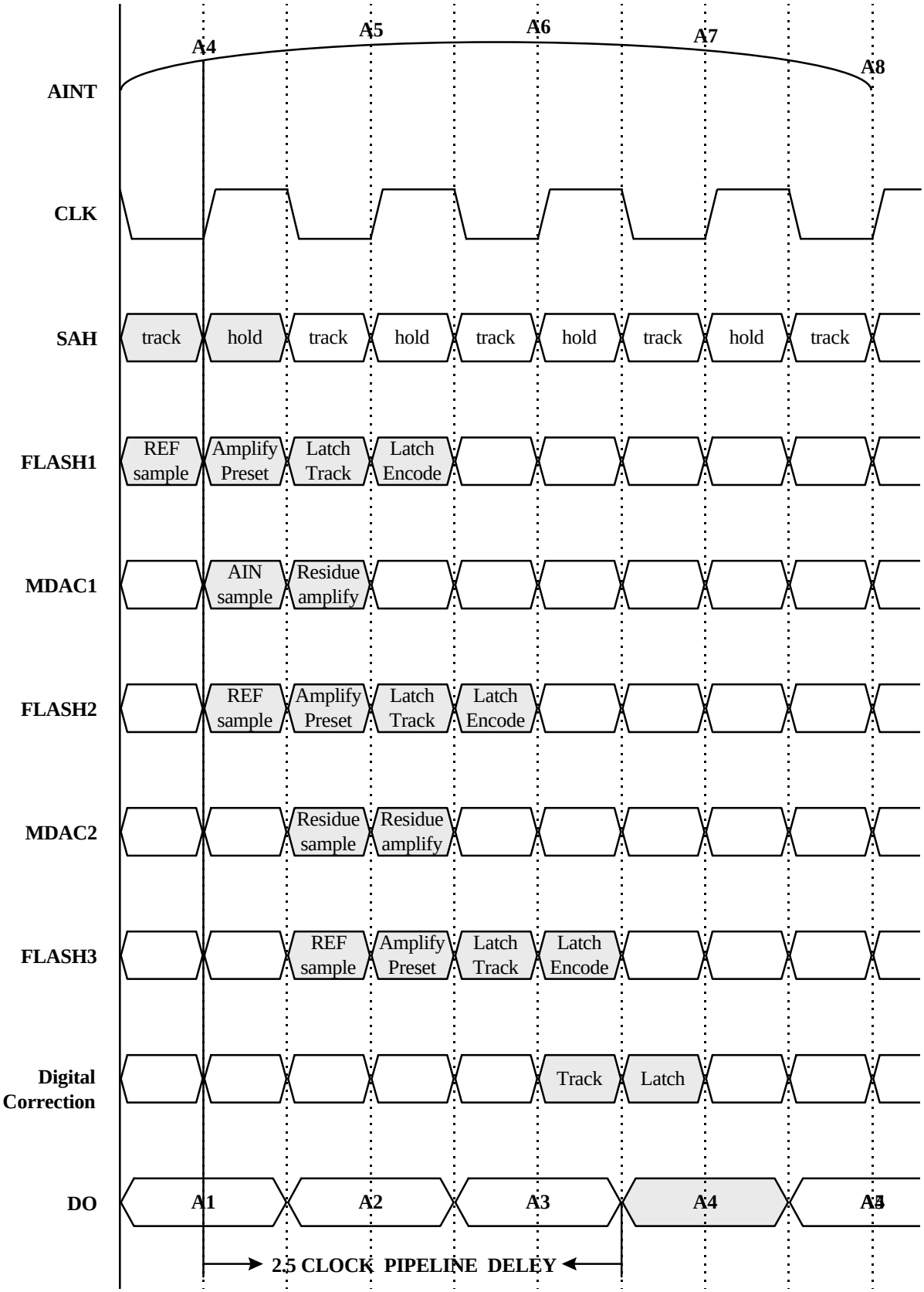
2. FLASH

The flash converter compares analog signal(SAH output) with reference voltage, and the result are transferred to MDAC and digital correction logic block. Its 8 comparators are fully differential. The comparators charge the reference voltage at the sampling capacitors (Q2) before comparing it with the SAH output (Q1). The output during Q1 is stored at the pre-latch block by Q1P clock signal.

3. MDAC

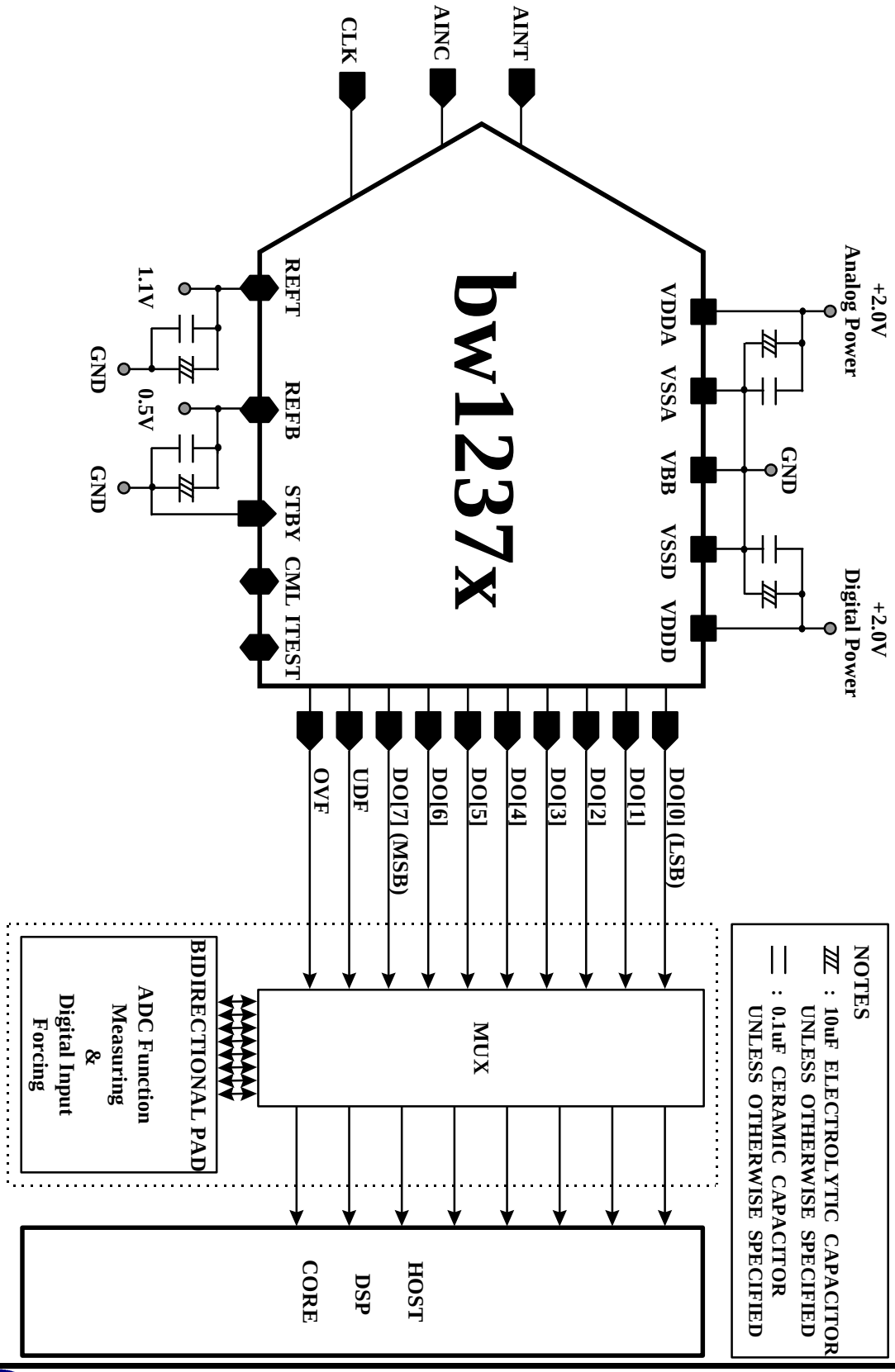
MDAC is the most important block and it governs the overall performances of ADC. MDAC consists of amp, selection logic and capacitor array (c_array). c_array is made up of the sampling capacitors and switches. Selection logic controls the internal switches of c_array. If Q1 is high, selection's output is all low, the switches of tsw1 are off and the switches of tsw2 are all on. Therefore the capacitors of c_array charges analog input values held at SAH and it is reversed during Q2 high.

TIMING DIAGRAM

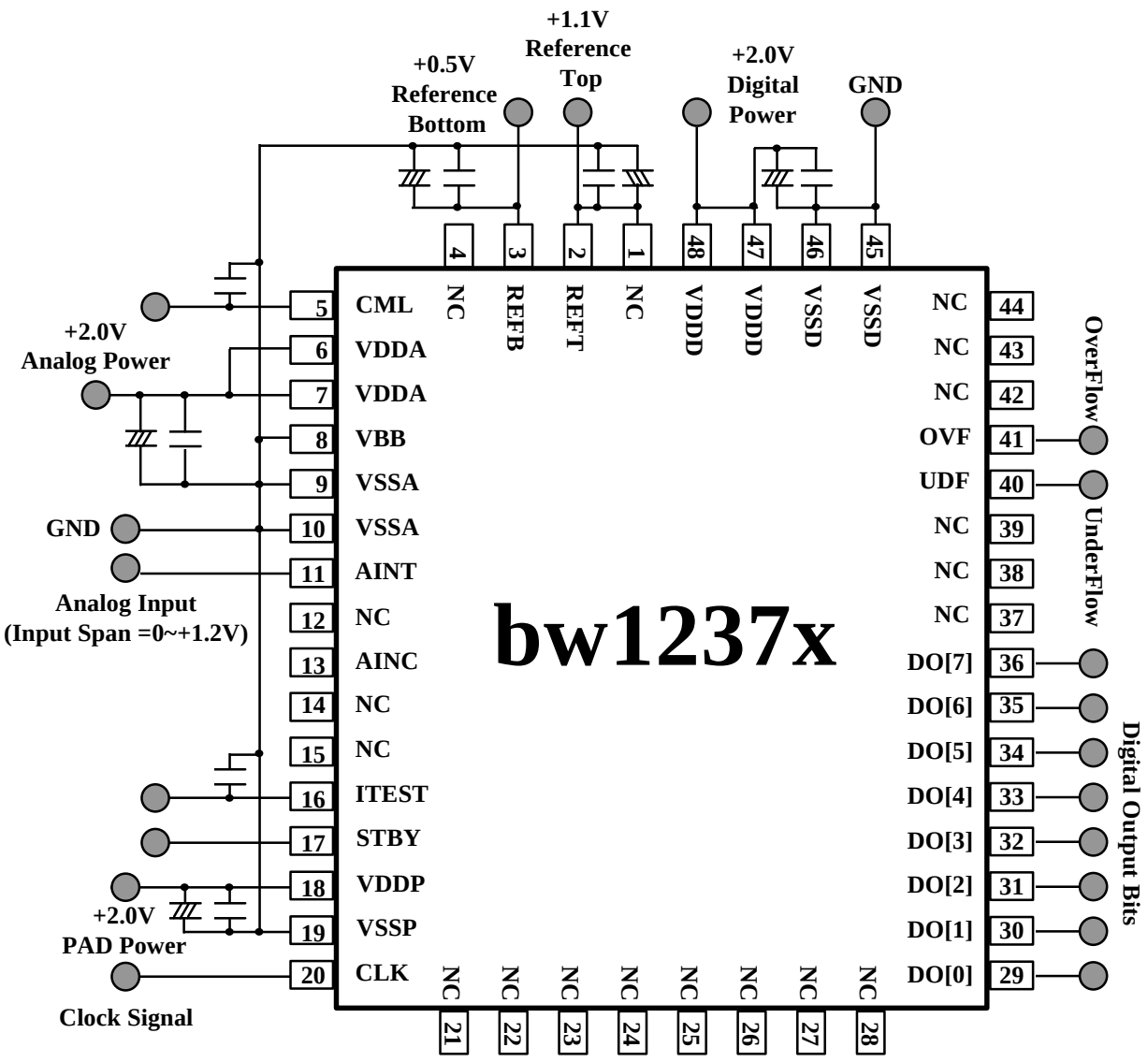


CORE EVALUATION GUIDE

1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.



PACKAGE CONFIGURATION



NOTES

: 10uF ELECTROLYTIC CAPACITOR UNLESS OTHERWISE SPECIFIED

: 0.1uF CERAMIC CAPACITOR UNLESS OTHERWISE SPECIFIED

NOTES

1. You can test ADC function by checking external bidirectional pad connected to internal signal path.
2. ESD (ElectroStatic Discharge) sensitive device. Although the digital control inputs are diode protected, permanent damage may occur on devices subjected to high electrostatic discharges. It is recommended that unused devices be stored in conductive foam or shunts to avoid performance degradation or loss of functionality. The protective foam should be discharged to the destination socket before devices are inserted.
3. NC denotes "No Connection".

PACKAGE PIN DESCRIPTION

NAME	PIN NO.	I/O TYPE	PIN DESCRIPTION
NC	1	-	No Connection
REFT	2	AB	+1.1V Reference Top Bias.
REFB	3	AB	+0.5V Reference Bottom Bias.
NC	4	-	No Connection
CML	5	AB	Internal Bias (Test Pin).
VDDA	6, 7	AP	+2.0V Analog Power.
VBB	8	AG	Sub Bias.
VSSA	9, 10	AG	Analog Ground.
AINT	11	AI	Positive Analog Input. Input Span = 0.0V ~ +1.2V.
NC	12	-	No Connection
AINC	13	AI	Negative Analog Input. Input = GND (Analog Ground).
NC	14, 15	-	No Connection
ITEST	16	AB	Open (Use Internal Bias)
STBY	17	DI	High (Power Saving Standby Mode) Low (Normal Operation)
VDDP	18	DP	PAD Power
VSSP	19	DG	PAD Ground
CLK	20	DI	Clock Input.
NC	21~28	-	No Connection
DO[7:0]	36~29	DO	Digital Output.
NC	37~39	-	No Connection
UDF	40	DO	UnderFlow Indication
OVF	41	DO	OverFlow Indication
NC	42~44	-	No Connection
VSSD	45, 46	DG	Digital Ground.
VDDD	47, 48	DP	Digital Power.

I/O TYPE ABBR.

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- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

FEEDBACK REQUEST

It should be quite helpful to our ADC core development if you specify your system requirements on ADC in the following characteristic cheking table and fill out the additional questions.
We appreciate your interest in our products. Thank you very much.

Characteristic	Min	Typ	Max	Unit	Remarks
Analog Power Supply Voltage				V	
Digital Power Supply Voltage				V	
Bit Resolution				Bit	
Reference Input Voltage				V	
Analog Input Voltage				Vpp	
Operating Temperature				°C	
Integral Non-linearity Error				LSB	
Differential Non-linearity Error				LSB	
Bottom Offset Voltage Error				LSB	
Top Offset Voltage Error				LSB	
Maximum Conversion Rate				MSPS	
Dynamic Supply Current				mA	
Power Dissipation				mW	
Signal-to-noise+distortion Ratio				dB	
Pipeline Delay				CLK	
Digital Output Format (Provide detailed description & timing diagram)					

1. Between single input-output and differential input-output configurations, which one is suitable for your system and why?

2. Please comment on the internal/external pin configurations you want our ADC to have, if you have any reason to prefer some type of configuration.

3. Freely list those functions you want to be implemented in our ADC, if you have any.