REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24									

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-01-05

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, RADIATION HARDENED CMOS STATIC CLOCK CONTROLLER/GENERATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-95820

SHEET 1 OF 24

DESC FORM 193
JUL 94

5962-E262-96

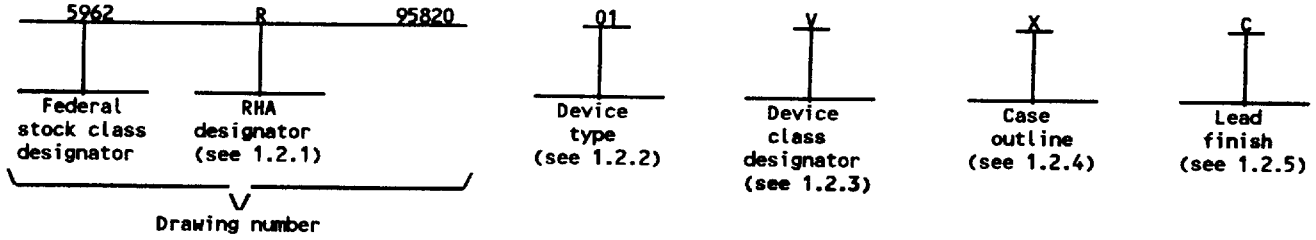
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0018189 009

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	82C85RH	Radiation Hardened, CMOS static clock controller/generator

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	CDIP2-T24	24	Dual-in-line package
X	CDFP4-F24	24	Flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD})	+6.5 V dc
Input, output or I/O voltage range	GND-0.3 V dc to V_{DD} +0.3 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering 10 seconds) (T_S)	+300 °C
Thermal resistance junction-to-case (θ_{JC}):	
Case outline J	12°C/W
Case outline X	10°C/W
Thermal resistance junction-to-ambient (θ_{JA}):	
Case outline J	52°C/W
Case outline X	70°C/W
Maximum package power dissipation at T_A = +125°C (P_D) 2/:	
Case outline J	0.96 W
Case outline X	0.71 W

1.4 Recommended operating conditions.

Operating supply voltage range (V_{DD})	4.5 V dc to +5.5 V dc
Operating temperature range (T_A)	-55°C to +125°C
Input low voltage range (V_{IL})	0 V dc to +0.8 V dc
Input high voltage range (V_{IH})	3.5 V dc to V_{DD}
Reset input high voltage range (V_{IH})	3.5 V dc to V_{DD}
Radiation features	
Total dose	> 100 kRads(SI)
Transient upset	> 10^8 RAD(SI)/sec 3/
Single event upset	4/
Single event latchup	4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If device power exceeds package dissipation capability provide heat sinking or derate linearly (derating is basedon θ_{JA}) at a rate of 19.2mW/°C for case J, 14.3mw/°C for Case X.
3/ Guaranteed by design or process but not tested.
4/ Value to be added when testing completed.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

TABLE 1. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLK or CLK50 output high voltage	V_{OH}	V_{DD} = 4.5 V, I_O = -5.0 mA, V_{IN} = 0 V or 4.5 V	1,2,3	All	V_{DD}-0.4		V
Output high voltage	V_{OH}	V_{DD} = 4.5 V, I_O = -2.5 mA, V_{IN} = 0 V or 4.5 V	1,2,3	All	V_{DD}-0.4		V
Output low voltage	V_{OL}	V_{DD} = 4.5 V, I_O = 5.0 mA, V_{IN} = 0 V or 4.5 V	1,2,3	All		0.4	V
Input leakage current	I_{IL} or I_{IH}	V_{DD} = 5.5 V, V_{IN} = 0 V or 5.5 V, Input pins except: 11 to 15, 21,23	1,2,3	All	-1.0	+1.0	µA
Bus hold high leakage current 2/	I_{BHH}	V_{DD} = 4.5 V, 5.5 V, V_{IN} = 3.0 V, Pins: 11 to 15, 21	1,2,3	All	-200	-20	µA
Standby power supply current	I_{DDSB}	V_{DD} = 5.5 V, V_{IN} = GND or V_{DD}, I_O = 0 mA	1,2,3	All		100	µA
Operating power supply current	I_{DDOP}	V_{DD} = 5.5 V, V_{IN} = GND or V_{DD}, I_O = 0 mA, Crystal Frequency = 15 MHz	1,2,3	All		80	mA
RESET input hysteresis 3/	$(+)V_T$ $(-)V_T$	V_{DD} = 4.5 V and 5.5 V	1,2,3	All	0.25		V
Input capacitance	C_{IN}	f = 1 MHz V_{DD} = Open See 4.4.1c	4	All		5	pF
Output capacitance	C_{OUT}		4	All		15	pF
Functional tests		See 4.4.1b V_{DD} = 4.5 V, 5.5 V, V_{IN} = GND or V_{DD}, f = 1MHz	7,8	All			
Noise immunity functional test		See 4.4.1b V_{DD} = 5.5 V, V_{IN} = GND or 3.5 V and V_{DD} = 4.5 V, V_{IN} = 0.8 V or V_{DD}	7,8	All			

See footnotes at end of table

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMING REQUIREMENTS							
External frequency high time	t_{EHEL}	90% to 90%V_{IN} See figure 3, V_{DD} = 4.5 V	9,10,11	All	25		ns
External frequency low time	t_{ELEH}	10% to 10%V_{IN} See figure 3, V_{DD} = 4.5 V	9,10,11	All	25		ns
$\overline{RES}$ or START valid to CLK low 3/	t_{START}	V_{DD} = 4.5 V and 5.5 V See figure 3	9,10,11	All	$2T_{ELEL}$ +3		ns
$\overline{STOP}$ command valid to CLK high 3/	t_{STOP}	V_{DD} = 4.5 V and 5.5 V See figure 3	9,10,11	All	$2T_{CLCL}$ +3	$3T_{CHCH}$ +55	ns
EFI or crystal period	t_{ELEL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	65		ns
External frequency input duty cycle	t_{EFIDC}		9,10,11	All	45	55	%
Crystal frequency	f		9,10,11	All	2.4	15	MHz
RDY1, RDY2 active setup to CLK	t_{R1VCL}	$\overline{ASYNC}$ = high See figure 3, V_{DD} = 4.5 V	9,10,11	All	55		ns
RDY1, RDY2 active setup to CLK	t_{R1VCH}	$\overline{ASYNC}$ = low See figure 3, V_{DD} = 4.5 V	9,10,11	All	55		ns
RDY1, RDY2 inactive setup to CLK	t_{R1VCL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	55		ns
RDY1, RDY2 hold to CLK	t_{CLR1X}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	0		ns
$\overline{ASYNC}$ setup to CLK	t_{AYVCL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	84		ns
$\overline{ASYNC}$ hold to CLK	t_{CLAYX}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	0		ns
$\overline{AEN1}$ $\overline{AEN2}$ setup to RDY1, RDY2	t_{A1VR1V}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	25		ns
$\overline{AEN1}$ $\overline{AEN2}$ hold to CLK	t_{CLA1X}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMING REQUIREMENTS - CONTINUED.							
CSYNC setup to EFI	t_{YHEH}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	17		ns
CSYNC hold to EFI	t_{YHEL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	17		ns
CSYNC pulse width	t_{YHYL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	$2t_{TELEL}$		ns
$\overline{RES}$ setup to CLK	t_{I1HCL}	See figure 3, V_{DD} = 4.5 V 5/	9,10,11	All	105		ns
S0, S1,$\overline{S2}$/$\overline{STOP}$ setup to CLK	t_{SVCH}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	55		ns
S0, S1,$\overline{S2}$/$\overline{STOP}$ hold to CLK	t_{CHSX}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	55		ns
$\overline{RES}$ START setup to CLK	t_{RSVCH}	See figure 3, V_{DD} = 4.5 V 5/	9,10,11	All	105		ns
$\overline{RES}$ (Low) or START (High) pulse width	t_{SHSL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	$2/3t_{CLCL}$		ns
$\overline{SLO}$/FST setup to PCLK	t_{SFPC}	See figure 3, V_{DD} = 4.5 V 5/	9,10,11	All	$t_{EHEL+170}$		ns
TIMING RESPONSES							
CLK/CLK50 cycle period	t_{CLCL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	200		ns
CLK HIGH time	tCHCL	See figure 3, V_{DD} = 4.5 V	9,10,11	All	$(1/3t_{CLCL})$ +3		ns
CLK LOW	t_{CLCH}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	$(2/3t_{CLCL})$ -15		ns
CLK50 HIGH time	t_{5CHCL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	$(1/2t_{CLCL})$ -7.5		ns
CLK50 LOW time	t_{5CLCH}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	$(1/2t_{CLCL})$ -7.5		ns
PCLK HIGH time	t_{PHPL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	$t_{CLCL-20}$		ns
PCLK LOW time	t_{PLPH}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	$t_{CLCL-20}$		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMING RESPONSES CONTINUED.							
Ready inactive to CLK	t_{RYLCL}	See figure 3, V_{DD} = 4.5 V 6/	9,10,11	All	-8		ns
Ready active to CLK	t_{RYHCH}	See figure 3, V_{DD} = 4.5 V 5/	9,10,11	All	$2/3(t_{CLCL})$ -15		ns
CLK to reset delay	t_{CLIL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All		65	ns
CLK to PCLK HIGH delay	t_{CLPH}	See figure 3, V_{DD} = 4.5 V	9,10,11	All		40	ns
CLK to PCLK LOW delay	t_{CLPL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All		40	ns
OSC to CLK HIGH delay	t_{OHCH}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	-5	60	ns
OSC to CLK LOW delay	t_{OHCL}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	2	70	ns
OSC LOW to CLK50 HIGH delay	t_{OLCH}	See figure 3, V_{DD} = 4.5 V	9,10,11	All	-5	60	ns
CLK LOW to CLK50 LOW skew	t_{CLC50L}	See figure 3, V_{DD} = 4.5 V	9,10,11	All		10	ns
CLK/CLK50 rise time 3/	tCH1CH2	See figure 3 V_{DD} = 4.5 V and 5.5 V, 1.0 V to 3.5 V	9,10,11	All		15	ns
CLK/CLK50 fall time 3/	tCL1CL2	See figure 3 V_{DD} = 4.5 V and 5.5 V, 3.5 V to 1.0 V	9,10,11	All		15	ns
Output rise time (except CLK) 3/	t_{OLOH}	See figure 3 V_{DD} = 4.5 V and 5.5 V, 0.8 V to 2.0 V	9,10,11	All		25	ns
Output fall time (except CLK) 3/	t_{OHOL}	See figure 3 V_{DD} = 4.5 V and 5.5 V, 2.0 V to 0.8 V	9,10,11	All		25	ns
Start/reset valid to CLK Low 3/	t_{OST}	See figure 3 V_{DD} = 4.5 V and 5.5 V (TYP) 4/	9,10,11	All		3	ms
RESET output time high 3/	t_{RST}	See figure 3 V_{DD} = 4.5 V and 5.5 V	9,10,11	All	$16(t_{CLCL})$		ms

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

1/ Devices supplied to this drawing will meet all levels M, D, L, and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C. All measurements referenced to ground.

2/ I_{BHH} should be measured after raising V_{IN} to V_{DD} and then lowering to 3.0 V.

3/ The parameters listed in the table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

4/ Oscillator start-up time depends on several factors including crystal frequency, crystal manufacturer, capacitive load, temperature, power supply voltage, ect. This parameter is given for information only.

5/ Applied only to T3, TW states.

6/ Applied only to T2 states.

Device type	01		
Case outlines	J and X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CSYNC	13	S0
2	PCLK	14	S1
3	$\overline{AEN1}$	15	$\overline{S2}/\overline{STOP}$
4	RDY1	16	RESET
5	READY	17	$\overline{RES}$
6	RDY2	18	OSC
7	$\overline{AEN2}$	19	$\overline{F/C}$
8	CLK	20	ER
9	GND	21	$\overline{ASYNC}$
10	CLK50	22	X2
11	START	23	X1
12	$\overline{SLO}/FST$	24	V_{DD}

FIGURE 1. Terminal connections.

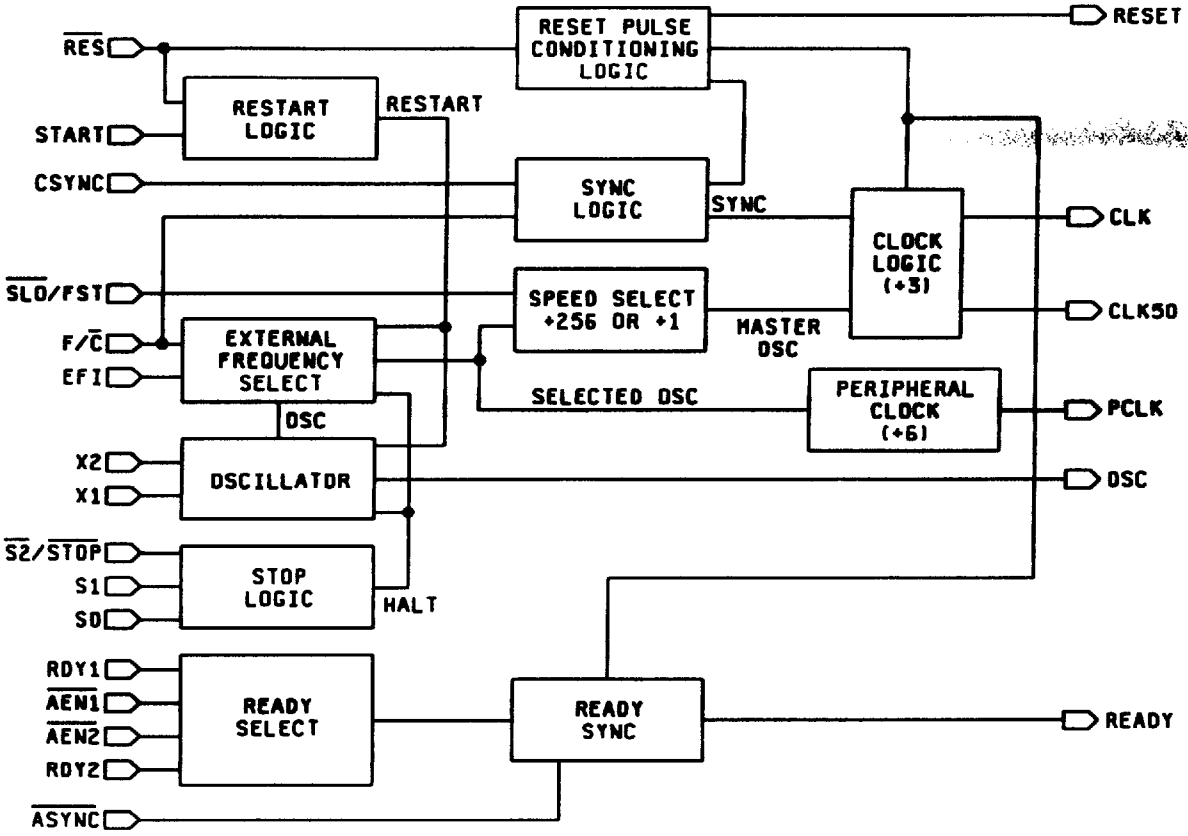
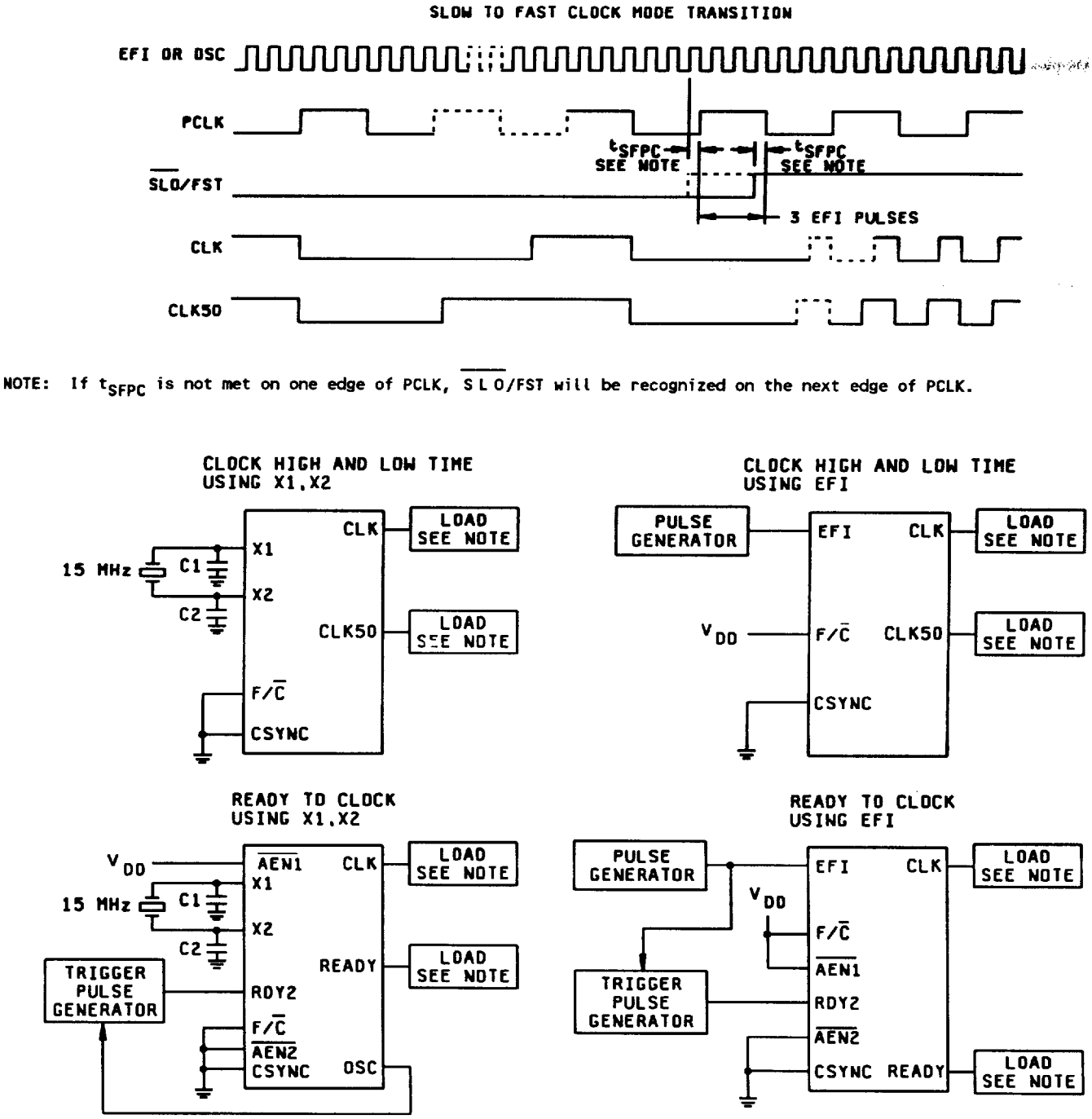


FIGURE 2. Block diagram.

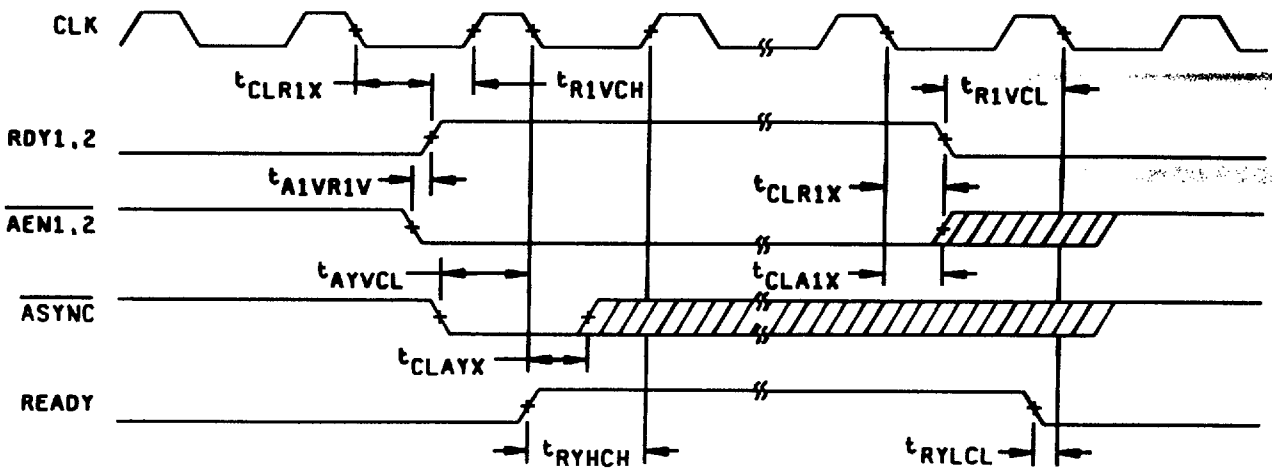


NOTE: If t_{SFPC} is not met on one edge of PCLK, $\overline{SLO/FST}$ will be recognized on the next edge of PCLK.

NOTE: C_L = 50 pF

FIGURE 3. Timing waveforms and load circuit.

WAVEFORMS FOR READY SIGNALS FOR ASYNCHRONOUS DEVICES



CLOCK STOP (F/$\overline{C}$ HIGH OR F/$\overline{C}$ LOW)

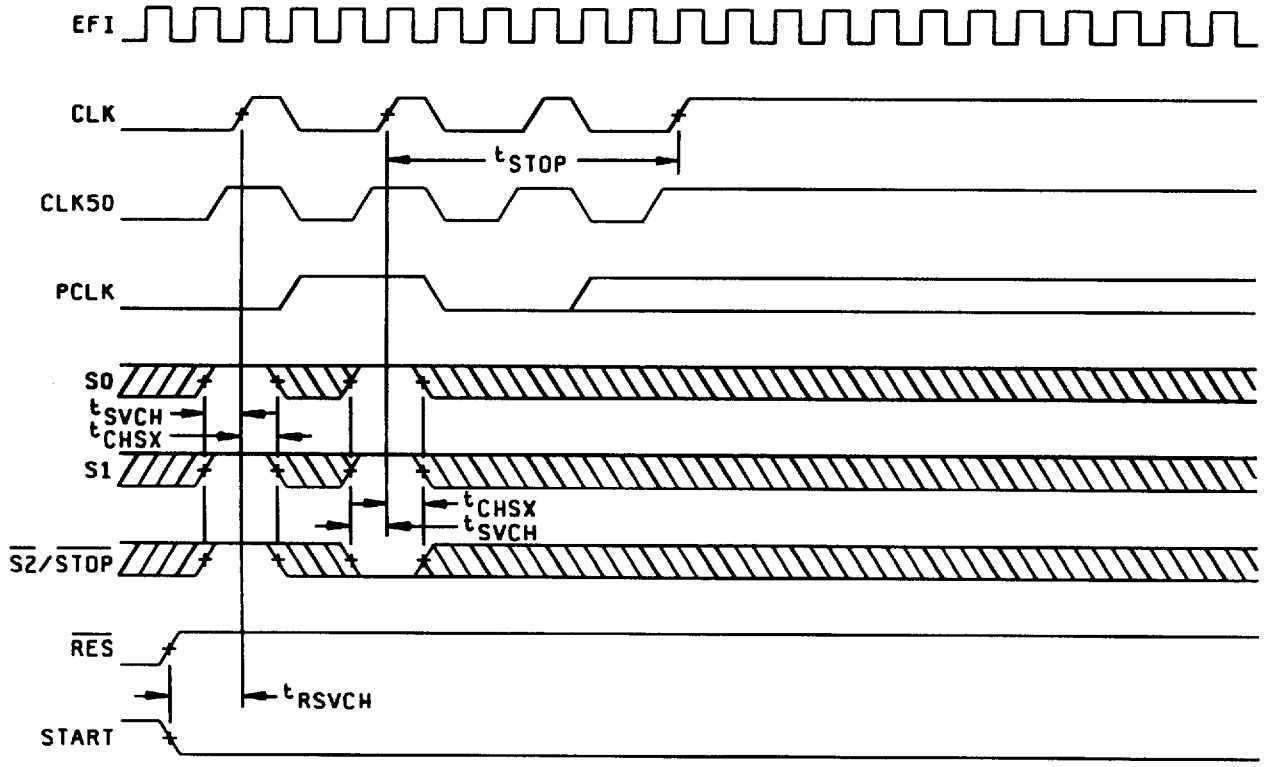


FIGURE 3. Timing waveforms and load circuit - Continued.

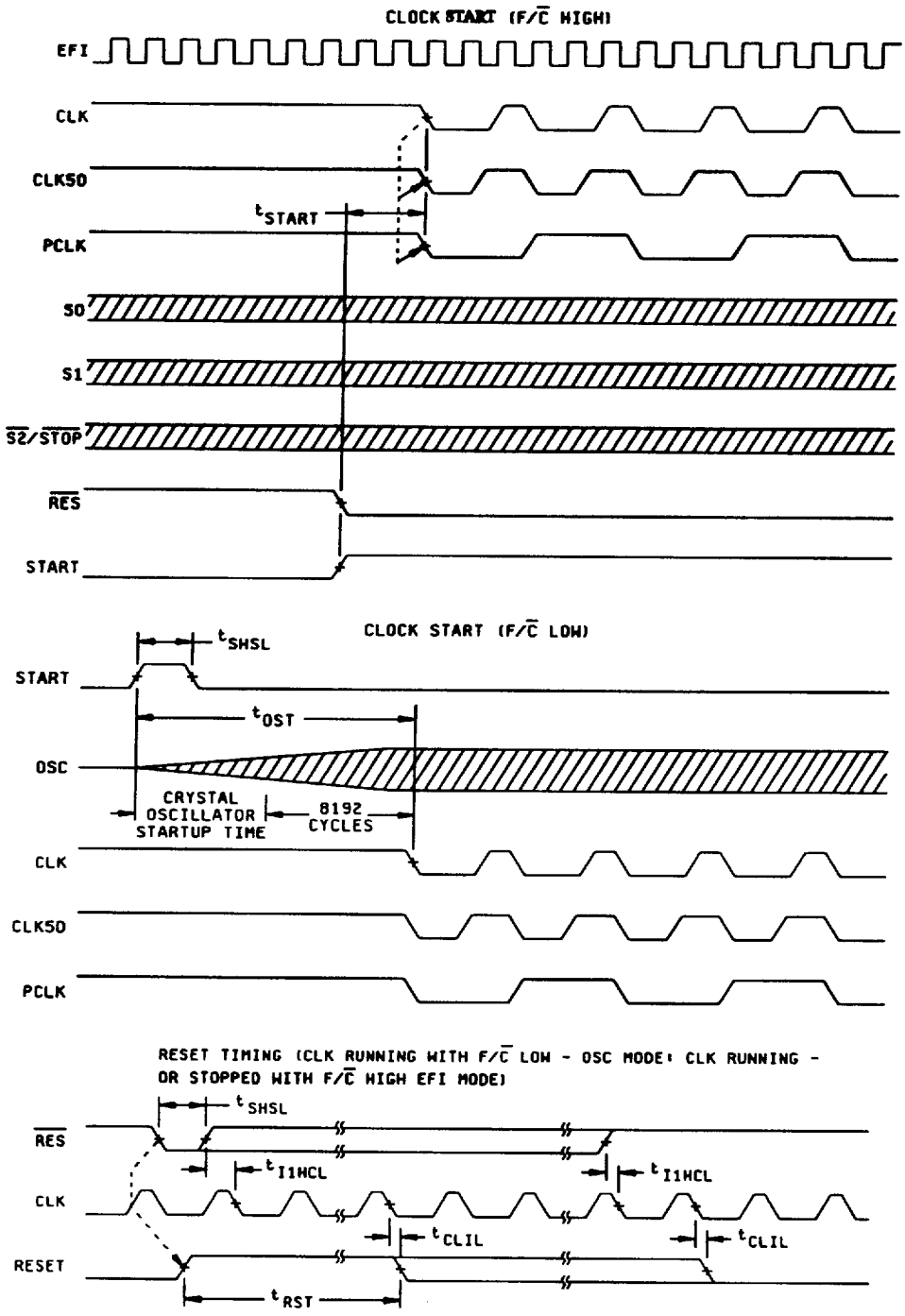
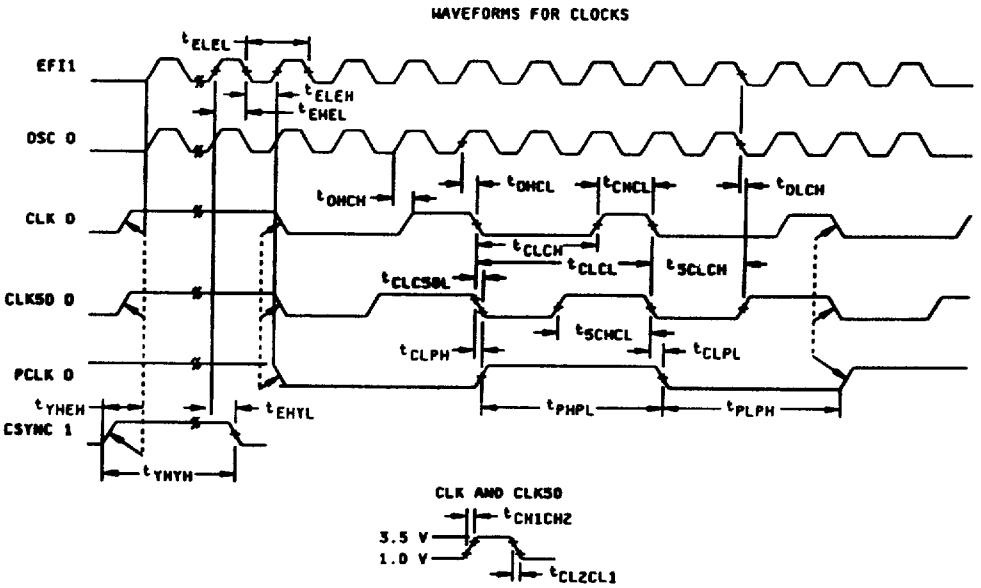


FIGURE 3. Timing waveforms and load circuit - Continued.



NOTE: Unless otherwise specified, all timing measurements are made at 1.5 V.

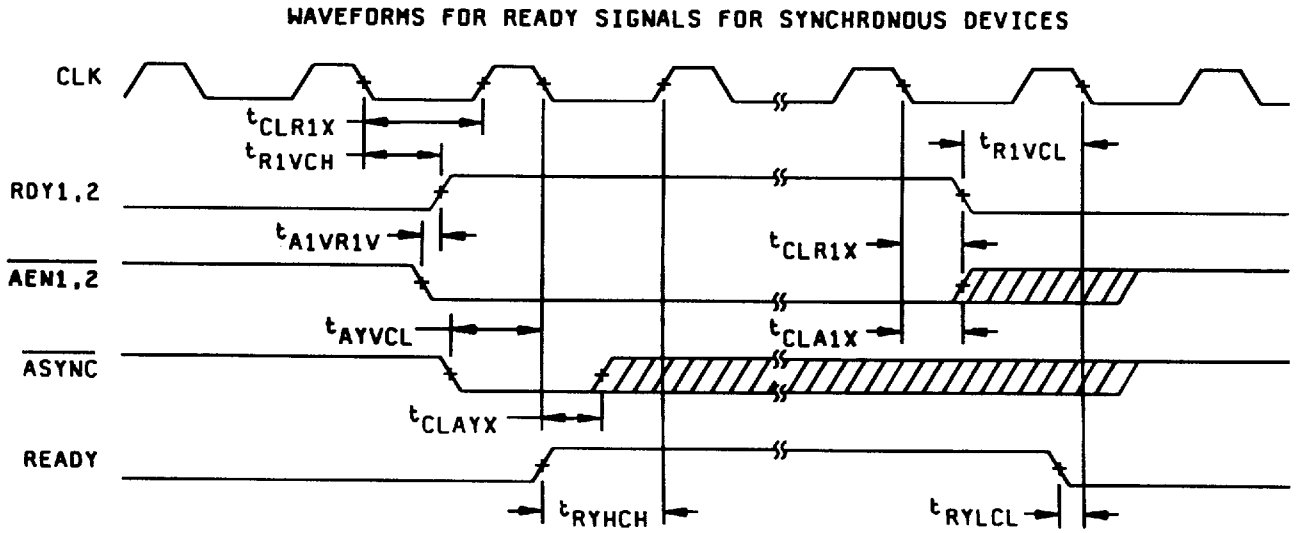
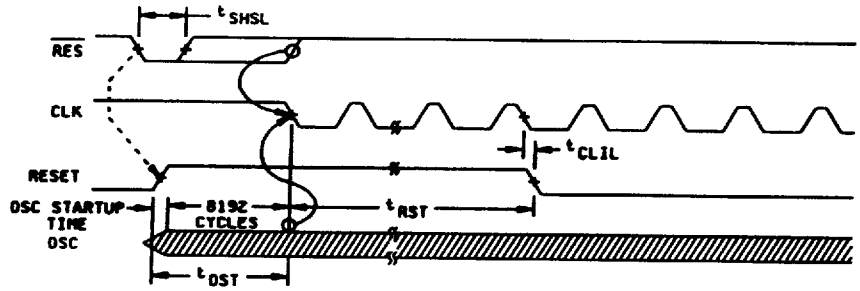


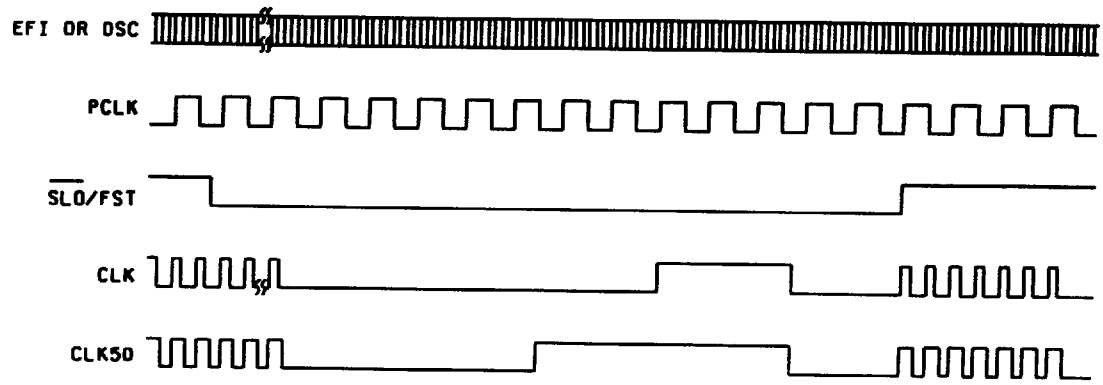
FIGURE 3. Timing waveforms and load circuit - Continued.

RESET TIMING OSCILLATOR STOPPED (F/$\overline{C}$ LOW)



NOTE: CLK, CLK50, and PCLK remain in the high state until $\overline{RES}$ goes high and 8192 valid oscillator cycles have been registered by the device internal counter TOST time period. After $\overline{RES}$ goes high and CLK, CLK50, and PCLK become active, the RESET output will remain high for a minimum of 16 CLK cycles (TRST).

SLO/FST TIMING OVERVIEW



FAST TO SLOW CLOCK MODE TRANSITION

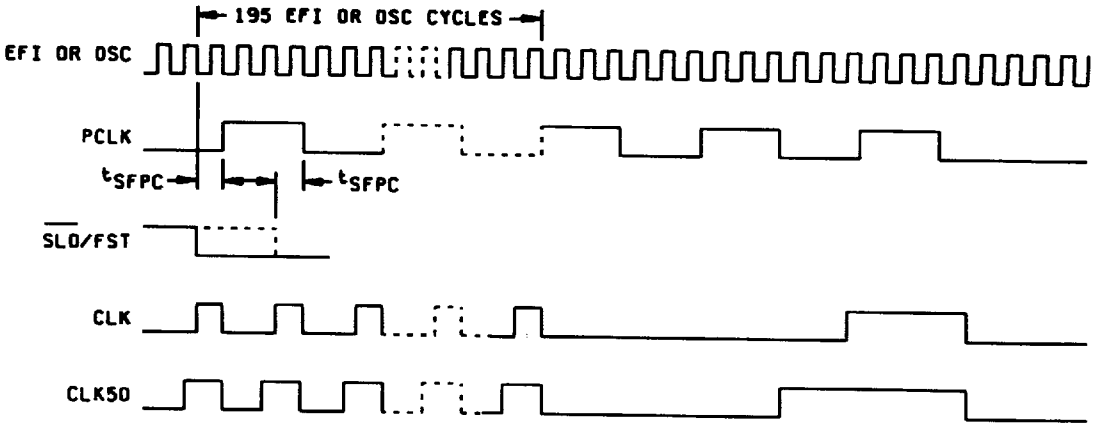
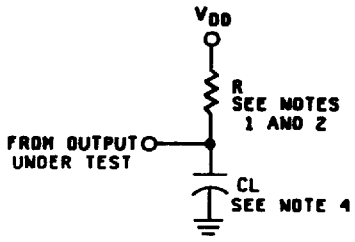
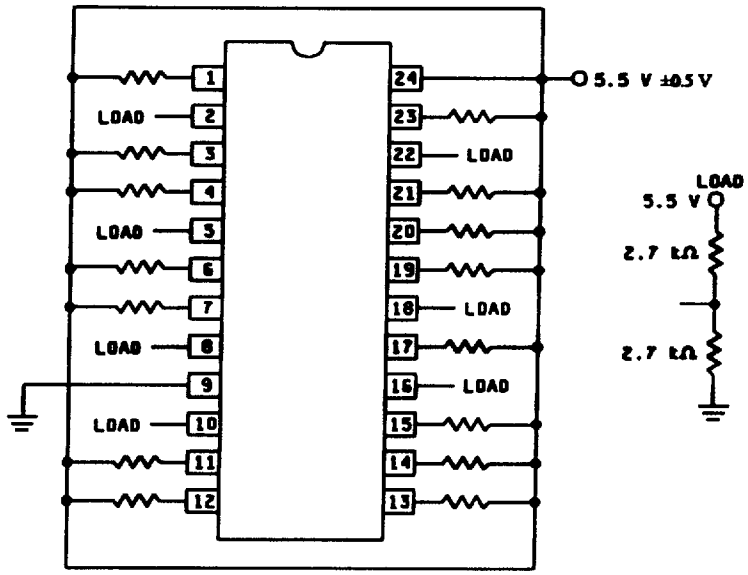


FIGURE 3. Timing waveforms and load circuit - Continued.



NOTES:
1. R = 370Ω at V = 2.25 for CLK and CLK50 outputs.
2. R = 494Ω at V = 2.87 for all other outputs.
3. C_L = 50 pF.
4. C_L includes probe and jig capacitance.

FIGURE 3. Timing waveforms and load circuit - Continued.



Note: R = 47 kΩ ±10%

FIGURE 4. Radiation exposure circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 or as modified in the device manufacturers approved Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535, or as modified in the QM plan, including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9, 10,11 1/	1,2,3,7,8,9,10,11 1/	1,2,3,7,8, 9,10,11 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9, 9,10,11	1,2,3,4,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9 10,11	1,2,3,7,8,9 10,11	1,2,3,7,8,9 10,11 3/
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7 and delta's.
3/ Delta limits as specified in table IIB herein shall be required where specified and the Delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in delta parameters (+25°).

Parameter	Symbol	Delta limits
Standby power supply current	I_{CCSB}	±20 µA
Input leakage current	I_{IH}, I_{IL}	±200 nA
Low level output voltage	V_{OL}	±80 mV
High level output voltage	V_{OH}	±150 mV

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-I-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (See 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

Pin symbol	Type	Description
X1 X2	I O	CRYSTAL CONNECTIONS: X1 and X2 are the are the crystal oscillator connections. The crystal frequency must be three times the maximum desired processor clock frequency. X1 is the oscillator circuit input and X2 is the output of the oscillator circuit.
EMI	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input signal. This input signal should be a square wave with a frequency of three times the maximum desired CLK output frequency.
F/$\overline{C}$	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ selects either the crystal oscillator or the EFI input as the main frequency source. When F/C is LOW, the device clocks are derived from the crystal oscillator circuit. When F/C is HIGH, CLK is generated from the EFI input. F/C cannot be dynamically switched during normal operation.
START	I	A low-to-high transition on START will restart the CLK, CLK50, and PCLK outputs after the appropriate restart sequence is completed. When in the crystal mode (F/$\overline{C}$ LOW) with the oscillator stopped, the oscillator will be restarted when a Start command is received. The CLK, CLK50, and PCLK outputs will start after the oscillator input signal (X1) reaches the Schmitt trigger input threshold and an 8 k internal counter reaches terminal count. If F/C is HIGH (EFI mode), CLK, CLK50, and PCLK will restart within 3 EFI cycles after START is recognized. The device will restart in the same mode ($\overline{SLO}$/FST) in which it stopped, A high level on START disables the STOP mode.
S0 S1 S2/$\overline{STOP}$	I I I	S2/$\overline{STOP}$, S1, S0 are used to stop the device clock outputs (CLK, CLK50, PCLK) and are sampled by the rising edge of CLK. CLK, CLK50, and PCLK are stopped by S2/$\overline{STOP}$, S1, S0 being in the LHH state on the low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low). When in the crystal mode (F/$\overline{C}$) low and a STOP command is issued, the device oscillator will stop along with the CLK, CLK50, and PCLK outputs. When in the EFI mode only the CLK, CLK50, and PCLK outputs will be halted. The oscillator circuit if operational, will continued to run. The oscillator and/or clock is restarted by the START input signal going true (HIGH) or the reset input ($\overline{RES}$) going low.
$\overline{SLO}$/FST	I	$\overline{SLO}$/FST is a level-triggered input. When HIGH, the CLK and CLK50 outputs run at the maximum frequency (crystal or EFI frequency divided by 3). When LOW, CLK, and CLK50 frequencies are equal to the crystal or EFI frequency divided by 768. $\overline{SLO}$/FST mode changes are internally synchronized to eliminate glitches on the CLK and CLK50, START, and STOP control of the oscillator or EFI is available in either the SLOW or FAST frequency modes. The $\overline{SLO}$/FST input must be held LOW for at least 195 OSC/EFI clock cycles before it will be recognized. This eliminates unwanted frequency changes which could be caused by glitches or noise transients. The $\overline{SLO}$/FST input must be held HIGH for at least 6 OSC/EFI clock pulses to guarantee a transition to FAST mode operation.

Pin symbol	Type	Description - Continued.
CLK	O	PROCESSOR CLOCK: CLK is the clock output used by the device processor and other peripheral devices. When SLO/FST is high, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by three. When SLO/FST is low, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by 768. CLK has a 33% duty cycle.
CLK50	O	50% DUTY CYCLE CLOCK: CLK50 is an auxiliary click with a 50 percent duty cycle and is synchronized to the falling edge of CLK. When SLO/FST is high, CLK50 has an output frequency which is equal to the crystal or EFI input frequency divided by 3. When SLO/FST is low, CLK50 has an output frequency equal to the crystal or EFI input frequency divided by 768.
PCLK	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is equal to the crystal or EFI input frequency divided by six and has a 50 percent duty cycle. PCLK frequency is unaffected by the state of the SLO/FST input.
OSC	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal oscillator circuit. OSC is unaffected by the state of the SLO/FST input. When the device is in the crystal mode (F/$\overline{C}$ LOW) and a STOP command is issued, the OSC output will stop in the HIGH state. When the device is in the EFI mode (F/C HIGH), the oscillator (if operational) will continue to run when a STOP command is issued and OSC remains active.
$\overline{RES}$	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The device provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. RES starts crystal oscillator operation.
RESET	O	RESET: RESET is an active HIGH signal which is used to reset the device processor. Its timing characteristics are determined by RES. RESET is guaranteed to be HIGH for a minimum of 16 CLK pulses after the rising edge of RES.
CSYNC	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple devices to be synchronized to provide multiple in-phase clock signals. When CSYNC is HIGH, the internal counters are reset and force CLK, CLK50, and PCLK into a HIGH state. When CSYNC is LOW, the internal counters are allowed to count and the CLK, CLK50, and PCLK outputs are active. CSYNC must be externally synchronized to EFI.
$\overline{AEN1}$ $\overline{AEN2}$	I I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). AEN1 validates RDY1 while AEN2 validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Buses.
RDY1 RDY2	I	BUS READY: (Transfer complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN1 and RDY2 is qualified by AEN2.
$\overline{ASYNC}$	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When ASYNC is LOW, two stages of READY synchronization are provided. When ASYNC is left open or HIGH a single stage of READY synchronization is provided.
READY	O	READY: READY is an active HIGH signal which is used to inform the device that it may conclude a pending data transfer.
GND	I	Ground.
V_{DD}		+5 V power supply.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.
b. Test conditions (SEP).
c. Number of upsets (SEP).
d. Number of transients (SEP).
e. Occurrence of latchup (SEP).