REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
G	Added device type 11. Added vendor cage 0EU86 for device types 05 through 09. -sld	99-08-27	Raymond Monnin

REV																			
SHEET																			
REV	G	G	G	G	G	G	G	G	G	G	G								
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS															
REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
94-06-24

REVISION LEVEL
G

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, DIGITAL, STATIC RANDOM ACCESS MEMORY, CMOS, 128K X 32-BIT,

SIZE	CAGE CODE	
A	**67268**	**5962-93187**

SHEET 1 OF 25

DSCC FORM 2233
APR 97

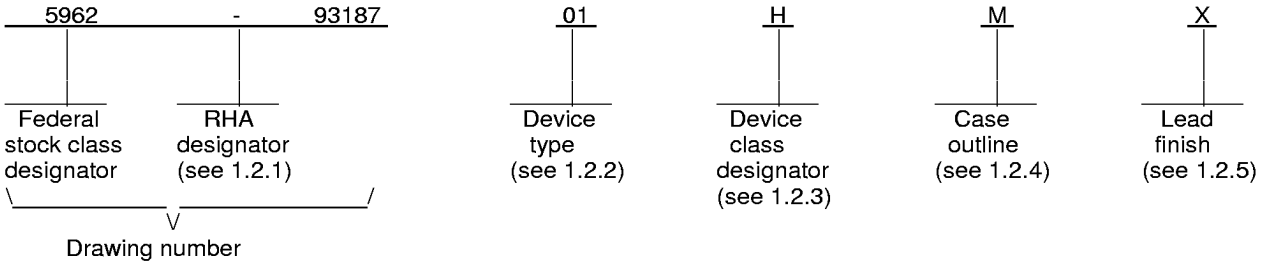
5962-E413-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowered high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WS-128K32-120HQ,ACT-S128K32-120PQ	SRAM, 128K X 32-bit	120 ns
02	WS-128K32-100HQ,ACT-S128K32-100PQ	SRAM, 128K X 32-bit	100 ns
03	WS-128K32-85HQ,ACT-S128K32-85PQ	SRAM, 128K X 32-bit	85 ns
04	WS-128K32-70HQ,ACT-S128K32-70PQ	SRAM, 128K X 32-bit	70 ns
05	WS-128K32-55HQ,ACT-S128K32-55PQ, AS8S128K32-55	SRAM, 128K X 32-bit	55 ns
06	WS-128K32-45HQ,ACT-S128K32-45PQ, AS8S128K32-45	SRAM, 128K X 32-bit	45 ns
07	WS-128K32-35HQ,ACT-S128K32-35PQ, AS8S128K32-35	SRAM, 128K X 32-bit	35 ns
08	WS-128K32-25HQ,ACT-S128K32-25PQ, AS8S128K32-25	SRAM, 128K X 32-bit	25 ns
09	WS-128K32-20HQ,ACT-S128K32-20PQ, AS8S128K32-20	SRAM, 128K X 32-bit	20 ns
10	WS-128K32-17HQ,ACT-S128K32-17PQ	SRAM, 128K X 32-bit	17 ns
11	WS-128K32-15HQ	SRAM, 128K X 32-bit	15 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows: 1/

Outline letter	Descriptive designator	Terminals	Package style
M	See figure 1	66	Hex-in-line, single cavity, without standoffs
N	See figure 1	66	Hex-in-line, single cavity, without standoffs
T	See figure 1	66	Hex-in-line, single cavity, with standoffs
U	See figure 1	66	Hex-in-line, single cavity, without standoffs
X	See figure 1	66	Hex-in-line, single cavity, with standoffs
Y	See figure 1	66	Hex-in-line, single cavity, without standoffs
4	See figure 1	66	Hex-in-line, single cavity, with standoffs
5	See figure 1	66	Hex-in-line, single cavity, with standoffs

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534 for classes H and K.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (any pin)	-0.5 V dc to +7.0 V dc
Power dissipation (P_D):	
Device types 01 through 08	2.2 W
Device type 09 through 11	4.4 W
Thermal resistance junction-to-case (θJ_C)	6.6°C/W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} +0.3 V dc
Output low voltage, maximum (V_{OL})	+0.4 V dc
Output high voltage, minimum (V_{OH})	+2.4 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. Unless otherwise specified, the following specification, standards, and handbooks of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

1/ Additional case outlines are available on 5962-95595.
2/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - Listing for Standard Microcircuits Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturer may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Block diagram. The block diagram shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DSCC-VA shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V dc, +4.5 V dc ≤ V_{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC PARAMETERS							
Supply current, 32-bit mode	I_{CC32}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz CMOS compatible V_{CC} = +5.5 V	1,2,3	01-04 05-11		120 600	mA
Standby current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, f = 5 MHz CMOS compatible V_{CC} = +5.5 V	1,2,3	01,02 03,04 05-08 09-11		2.4 5.0 60 80	mA
Input leakage current	I_{LI}	V_{CC} = +5.5 V, V_{IN} = GND or V_{CC}	1,2,3	All		10	uA
Output leakage current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND or V_{CC}	1,2,3	All		10	uA
Output low voltage	V_{OL}	V_{CC} = +4.5 V, I_{OL} = +2.1 mA	1,2,3	01-07		0.4	V
		V_{CC} = +4.5 V, I_{OL} = +8.0 mA		08-11		0.4	
Output high voltage	V_{OH}	V_{CC} = +4.5 V, I_{OH} = -1.0 mA	1,2,3	01-07	2.4		V
		V_{CC} = +4.5 V, I_{OH} = -4.0 mA		08-11	2.4		
DATA RETENTION							
Data retention supply voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -0.2 V	1,2,3	All	2.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = +3.0 V	1,2,3	01-04 05-11		1.6 11.6	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V dc, +4.5 V dc ≤ V_{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CAPACITANCE							
$\overline{OE}$ capacitance 2/	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C	4	All		50	pF
$\overline{WE}$ 1-4 capacitance 2/	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C	4	All		20	pF
$\overline{CS}$ 1-4 capacitance 2/	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C	4	All		20	pF
D0 - D31 capacitance 2/	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz, T_A = +25°C	4	All		20	pF
A0 - A16 capacitance 2/	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C	4	All		50	pF
FUNCTIONAL TESTING							
Functional tests		See 4.3.1c	7,8A,8B	All			
READ CYCLE AC TIMING							
Read cycle time	t_{RC}	See figure 4	9,10,11	01	120		ns
				02	100		
				03	85		
				04	70		
				05	55		
				06	45		
				07	35		
				08	25		
				09	20		
				10	17		
				11	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, V_{SS} = 0 V dc, $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ CYCLE AC TIMING - Continued.							
Address access time	t_{AA}	See figure 4	9,10,11	01		120	ns
				02		100	
				03		85	
				04		70	
				05		55	
				06		45	
				07		35	
				08		25	
				09		20	
				10		17	
				11		15	
Output hold from address change	t_{OH}	See figure 4	9,10,11	01-04	5		ns
				05-11	0		
Chip select access time	t_{ACS}	See figure 4	9,10,11	01		120	ns
				02		100	
				03		85	
				04		70	
				05		55	
				06		45	
				07		35	
				08		25	
				09		20	
				10		17	
				11		15	
Output enable to output valid	t_{OE}	See figure 4	9,10,11	01		60	ns
				02		50	
				03		45	
				04		35	
				05		30	
				06		25	
				07		20	
				08		15	
				09		12	
				10,11		10	
Chip select to output in low impedance 2/	t_{CLZ}	See figure 4	9,10,11	01-04	5		ns
				05-11	3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, V_{SS} = 0 V dc, $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ CYCLE AC TIMING - Continued.							
Output enable to output in low impedance 2/	t_{OLZ}	See figure 4	9,10,11	01-04	5		ns
				05-11	0		
Chip select to output in high impedance 2/	t_{CHZ}	See figure 4	9,10,11	01,02		35	ns
				03,04		25	
				05-07		20	
				08-11		12	
Output enable to output in high impedance 2/	t_{OHZ}	See figure 4	9,10,11	01,02		35	ns
				03,04		25	
				05-07		20	
				08-11		12	
WRITE CYCLE AC TIMING							
Write cycle time	t_{WC}	See figure 5	9,10,11	01	120		ns
				02	100		
				03	85		
				04	70		
				05	55		
				06	45		
				07	35		
				08	25		
				09	20		
				10	17		
				11	15		
Chip select to end of write	t_{CW}	See figure 5	9,10,11	01	100		ns
				02	80		
				03	75		
				04	60		
				05	45		
				06	30		
				07	25		
				08	20		
				09	15		
				10,11	14		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ Vss = 0 Vdc, $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
WRITE CYCLE AC TIMING - Continued.							
Address select to end of write	t_{AW}	See figure 5	9,10,11	01 02 03 04 05 06 07 08 09,10 11	100 80 75 60 45 30 25 20 15 14		ns
Data valid to end of write	t_{DW}	See figure 5	9,10,11	01 02 03 04 05,06 07 08 09 10,11	50 40 35 30 25 20 15 12 10		ns
Address setup time	t_{AS}	See figure 5	9,10,11	01-04 05-11	5.0 0		ns
Write pulse width	t_{WP}	See figure 5	9,10,11	01 02 03 04 05 06 07 08 09 10,11	80 70 55 50 45 30 25 20 15 14		ns
Write to output in high impedance 2/	t_{WHZ}	See figure 5	9,10,11	01,02 03-06 07 08 09 10,11	35 25 20 15 12 10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V dc, $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
WRITE CYCLE AC TIMING - Continued.							
Address hold time	t_{AH}	See figure 5	9,10,11	01-04	5		ns
				05-11	0		
Output active from end of write	t_{OW}	See figure 5	9,10,11	01-04	5		ns
				05-07	4		
				08-11	3		
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		ns

1/ Unless otherwise specified, the AC test conditions are as follows:

Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V, ± 0.5 V.
Output loading: See figure 7.

2/ Guaranteed by design, but not tested.

Case outlines M and N.

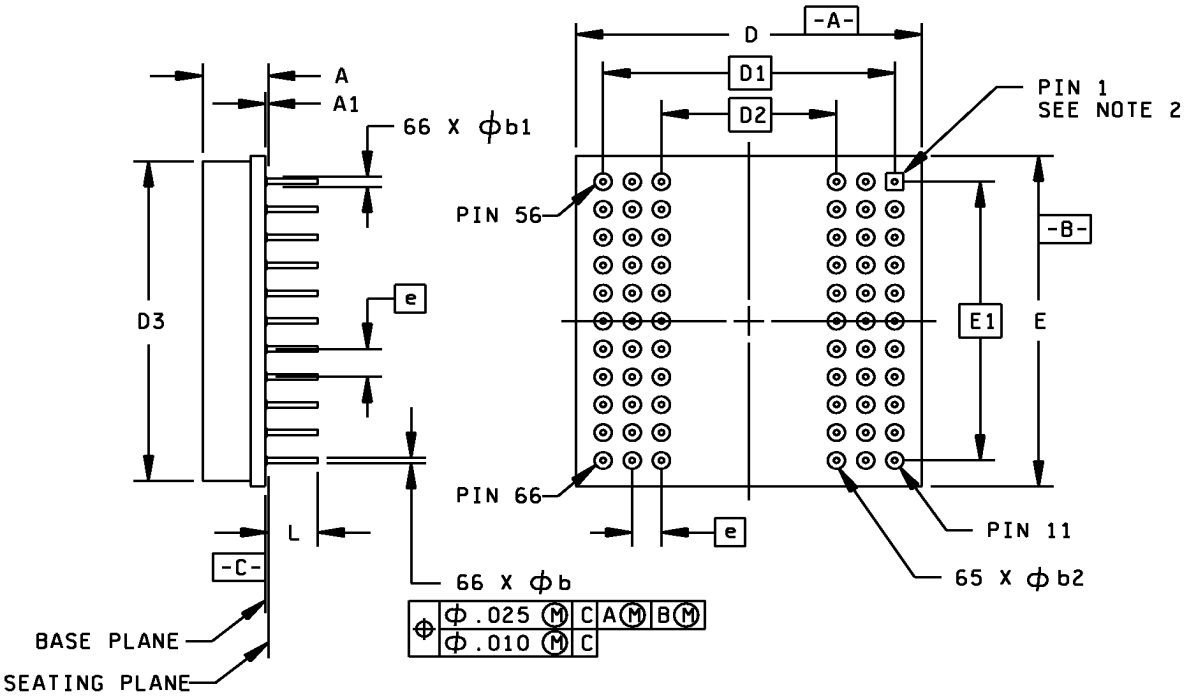


FIGURE 1. Case outline(s).

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.30	4.09	.130	.159
A1	0.13	0.50	.005	.020
øb	0.41	0.51	.016	.020
øb1	0.76 REF		.030 REF	
øb2	1.65	1.91	.065	.075
D/E	27.02	27.58	1.064	1.086
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		.600 BSC	
D3	26.16	26.42	1.030	1.040
e	2.54 BSC		.100 BSC	
L	4.19	4.69	.165	.185

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by a .070 inch (1.78 mm) square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

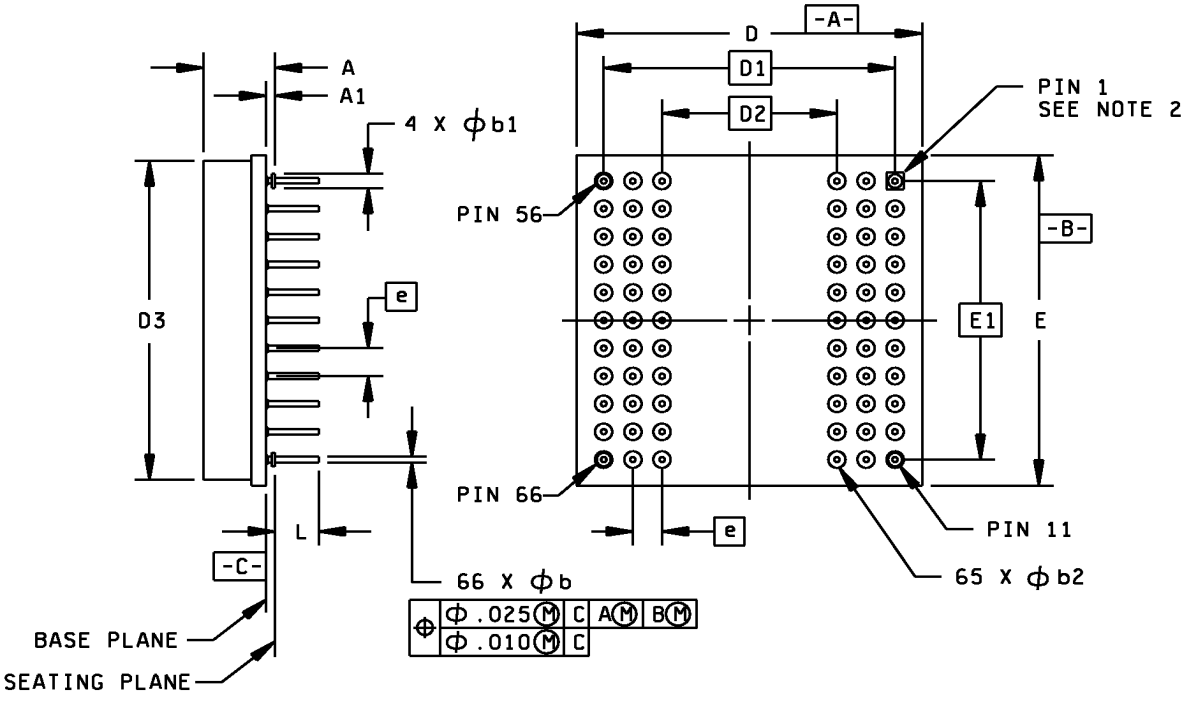


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	5.08	6.22	.200	.245
A1	0.64	0.89	.025	.035
øb	0.41	0.51	.016	.020
øb1	1.14	1.40	.045	.055
øb2	1.65	1.91	.065	.075
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		.600 BSC	
D3	28.96	29.21	1.140	1.150
e	2.54 BSC		.100 BSC	
L	3.68	3.94	.145	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by a .070 inch (1.78 mm) square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.43	4.95	.135	.195
A1	0.64	0.89	.025	.035
øb	0.41	0.51	.016	.020
øb1	1.14	1.40	.045	.055
øb2	1.65	1.91	.065	.075
D/E	27.02	27.58	1.064	1.086
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		.600 BSC	
D3	25.91	26.92	1.020	1.060
e	2.54 BSC		.100 BSC	
L	3.35	3.94	.132	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by a .060 inch (1.52 mm) square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outlines U and Y.

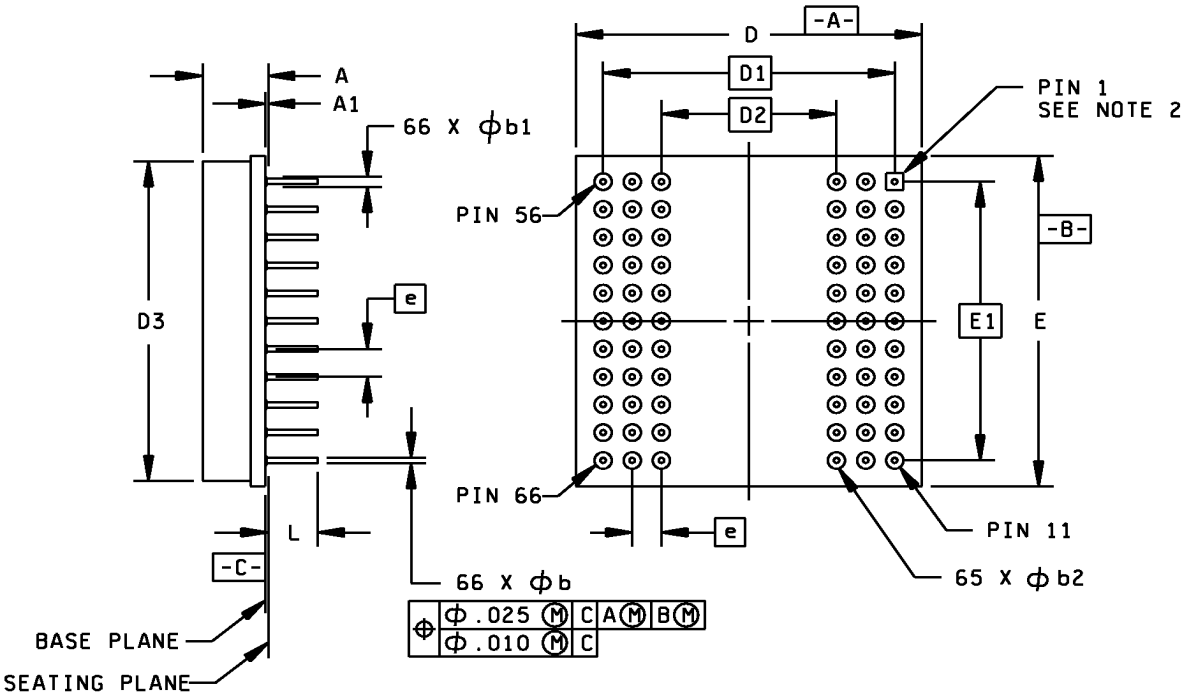


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.57	5.84	.180	.230
A1	0.13	0.50	.005	.020
øb	0.41	0.51	.016	.020
øb1	0.76	1.52	.030	.060
øb2	1.65	1.91	.065	.075
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		.600 BSC	
D3	28.96	29.21	1.140	1.150
e	2.54 BSC		.100 BSC	
L	4.19	4.69	.165	.185

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by a .070 inch (1.78 mm) square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Device types	All	Device types	All	Device types	All
Case outlines	M,N,T,U,X,Y, 4,5	Case outlines	M,N,T,U,X,Y, 4,5	Case outlines	M,N,T,U,X,Y, 4,5
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	23	I/O15	45	V_{CC}
2	I/O9	24	I/O14	46	$\overline{CS}4$
3	I/O10	25	I/O13	47	$\overline{WE}4$
4	A13	26	I/O12	48	I/O27
5	A14	27	$\overline{OE}$	49	A3
6	A15	28	See note	50	A4
7	A16	29	$\overline{WE}1$	51	A5
8	See Note	30	I/O7	52	$\overline{WE}3$
9	I/O0	31	I/O6	53	$\overline{CS}3$
10	I/O1	32	I/O5	54	GND
11	I/O2	33	I/O4	55	I/O19
12	$\overline{WE}2$	34	I/O24	56	I/O31
13	$\overline{CS}2$	35	I/O25	57	I/O30
14	GND	36	I/O26	58	I/O29
15	I/O11	37	A6	59	I/O28
16	A10	38	A7	60	A0
17	A11	39	See Note	61	A1
18	A12	40	A8	62	A2
19	V_{CC}	41	A9	63	I/O23
20	$\overline{CS}1$	42	I/O16	64	I/O22
21	See note	43	I/O17	65	I/O21
22	I/O3	44	I/O18	66	I/O20

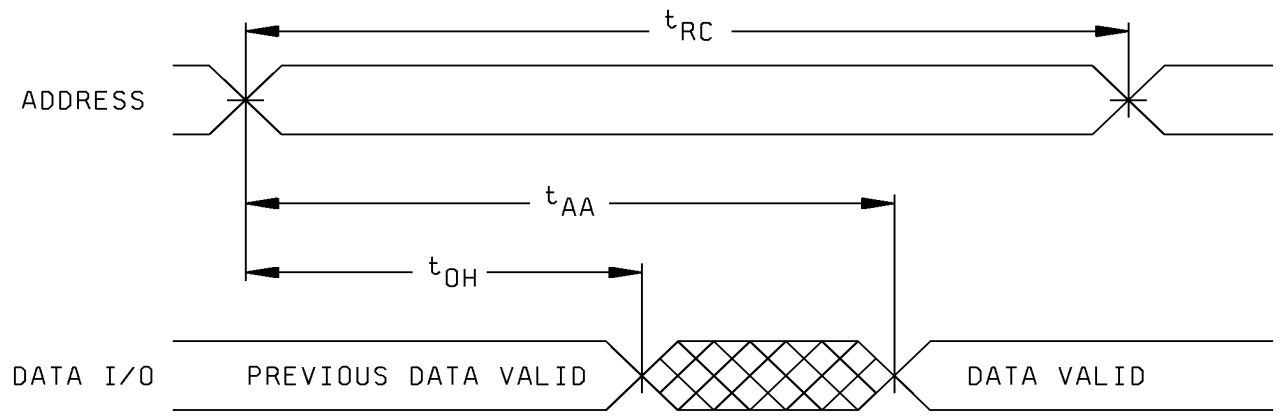
NOTE:
1. Case outlines M, T, U, and 4, pins 8, 21, 28, and 39 are no connects and for case outlines N, X, Y, and 5, pins 8, 21, 28, and 39 are grounds.

FIGURE 2. Terminal connections.

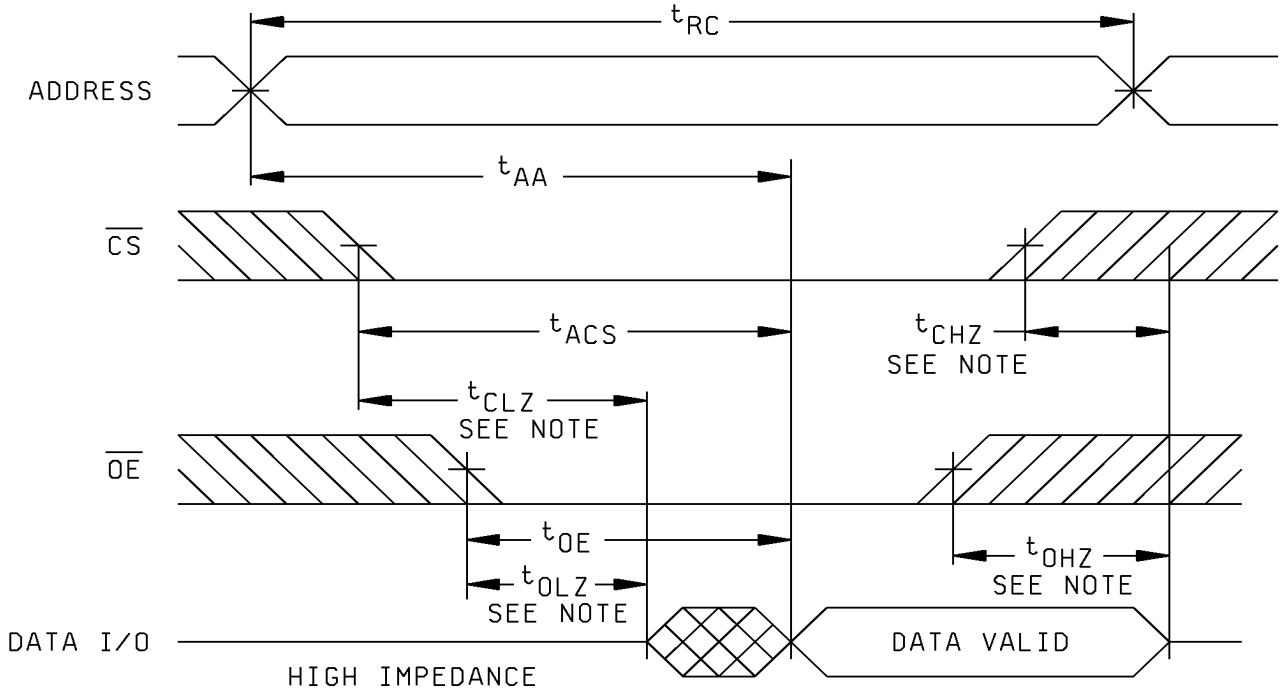
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby (deselect/power down)
L	L	H	Read	Data Out	Active
L	H	H	Output disable	High Z	Active (deselect)
L	X	L	Write	Data In	Active

Notes:
1. H = V_{IH} = High Logic Level
2. L = V_{IL} = Low Logic Level
3. X = Do not care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth table.



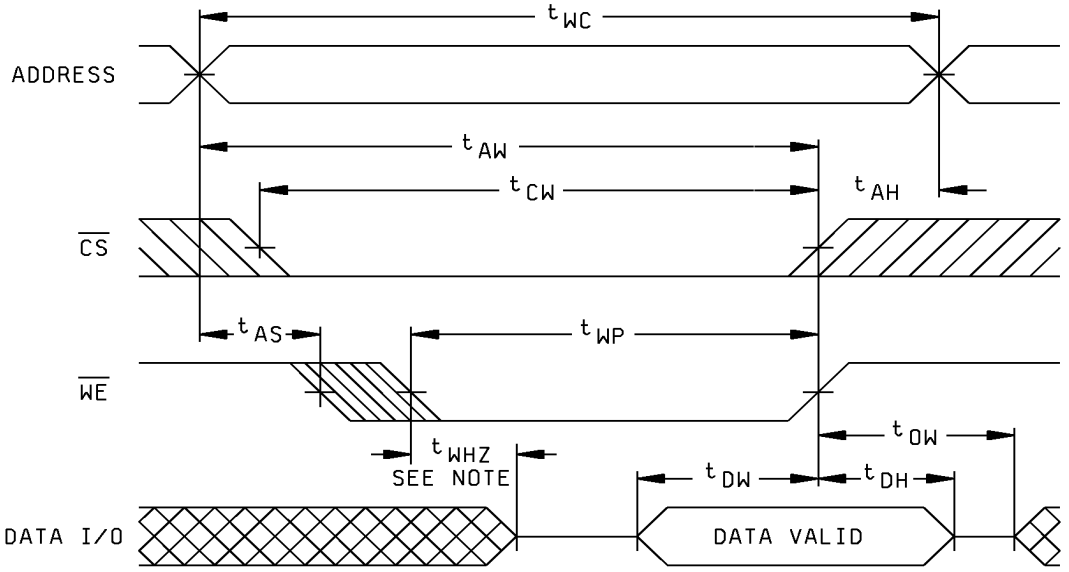
READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



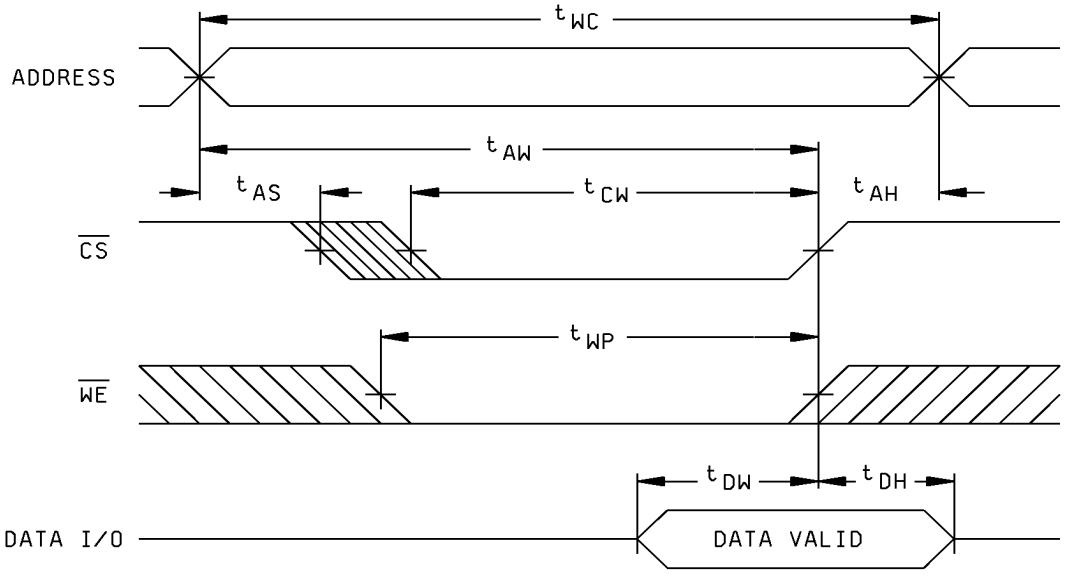
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

NOTE: Guaranteed by design, but not tested.

FIGURE 4. Read cycle timing diagram.



WRITE CYCLE 1 $\overline{WE}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED

NOTE: Guaranteed by design, but not tested.

FIGURE 5. Write cycle timing diagram.

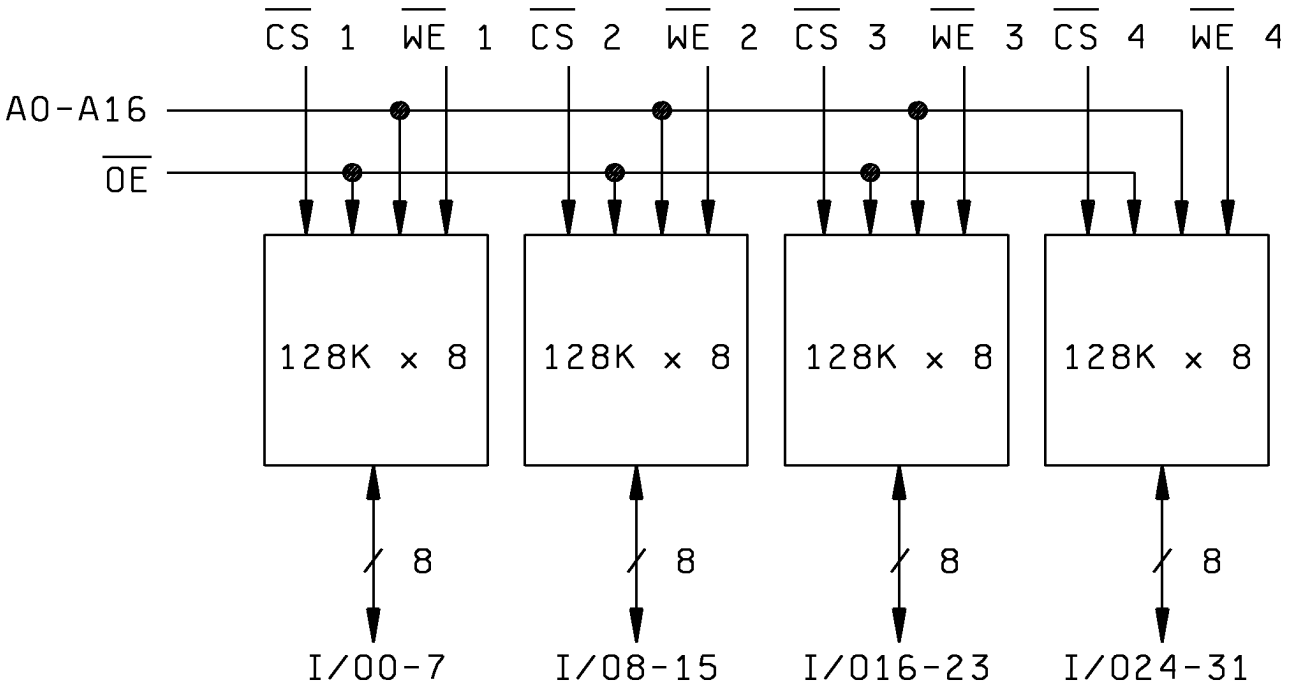
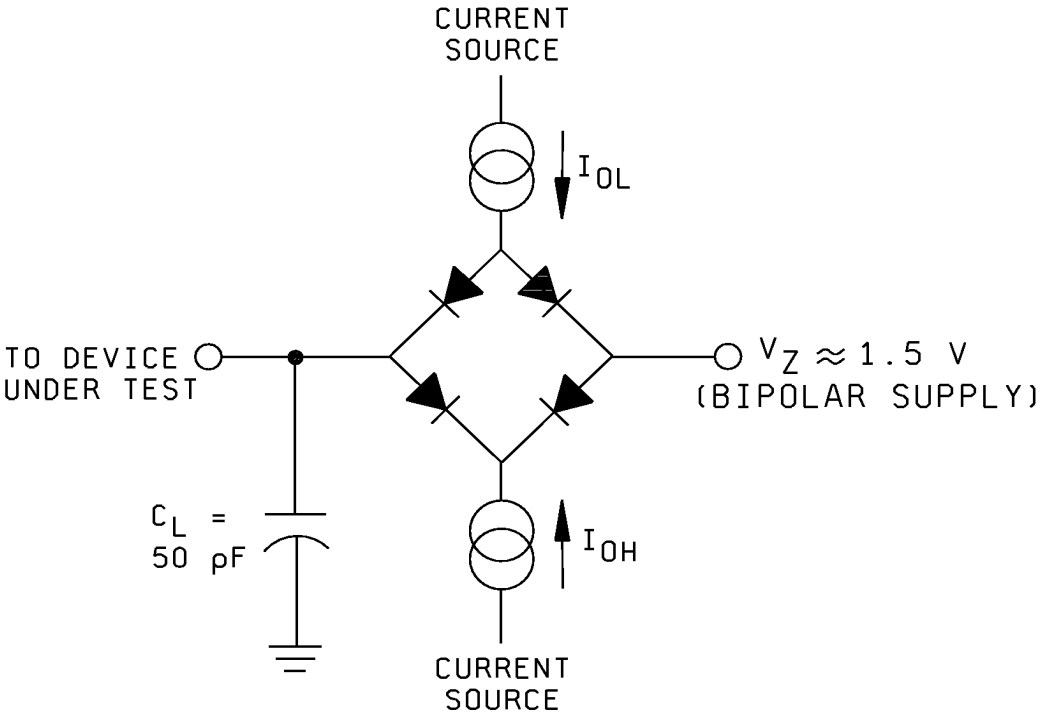


FIGURE 6. Block diagram.



Parameter	Typ.	Unit
Input Pulse Level	0 - 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Load Capacitance	50	pf

NOTES:
1. V_Z is programmable from -2V to +7V.
2. I_{OL} and I_{OH} are programmable from 0 to 16mA.
3. Tester impedance is ZO = 75 Ohms.
4. V_Z is typically the midpoint of V_{OH} and V_{OL}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical test parameters	1*,2,3,4,7,8A,8B,9,10, 11
Group A test requirements	1,2,3,4,7,8A,8B,9,10, 11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10, 11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and perodic inspection. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSSC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000 or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-08-27

Approved sources of supply for SMD 5962-93187 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSSC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard 1/ microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-9318701HTX	54230	WS128K32N-120HQ
5962-9318701HTX	88379	ACT-S128K32N-120P2Q
5962-9318701HUX	54230	WS128K32N-120HSQ
5962-9318701HUX	88379	ACT-S128K32N-120P6Q
5962-9318701HXX	54230	WS128K32-120HQ
5962-9318701HXX	88379	ACT-S128K32C-120P2Q
5962-9318701HYX	54230	WS128K32-120HSQ
5962-9318701HYX	88379	ACT-S128K32C-120P6Q
5962-9318701H4X	54230	WS128K32N-120H1Q
5962-9318701H5X	54230	WS128K32-120H1Q
5962-9318702HTX	54230	WS128K32N-100HQ
5962-9318702HTX	88379	ACT-S128K32N-100P2Q
5962-9318702HUX	54230	WS128K32N-100HSQ
5962-9318702HUX	88379	ACT-S128K32N-100P6Q
5962-9318702HXX	54230	WS128K32-100HQ
5962-9318702HXX	88379	ACT-S128K32C-100P2Q
5962-9318702HYX	54230	WS128K32-100HSQ
5962-9318702HYX	88379	ACT-S128K32C-100P6Q
5962-9318702H4X	54230	WS128K32N-100H1Q
5962-9318702H5X	54230	WS128K32-100H1Q
5962-9318703HTX	54230	WS128K32N-85HQ
5962-9318703HTX	88379	ACT-S128K32N-085P2Q
5962-9318703HUX	54230	WS128K32N-85HSQ
5962-9318703HUX	88379	ACT-S128K32N-085P6Q
5962-9318703HXX	54230	WS128K32-85HQ
5962-9318703HXX	88379	ACT-S128K32C-085P2Q
5962-9318703HYX	54230	WS128K32-85HSQ
5962-9318703HYX	88379	ACT-S128K32C-085P6Q
5962-9318703H4X	54230	WS128K32N-85H1Q
5962-9318703H5X	54230	WS128K32-85H1Q
5962-9318704HTX	54230	WS-128K32N-70HQ
5962-9318704HTX	88379	ACT-S128K32N-070P2Q
5962-9318704HUX	54230	WS-128K32N-70HSQ
5962-9318704HUX	88379	ACT-S128K32N-070P6Q
5962-9318704HXX	54230	WS128K32-70HQ
5962-9318704HXX	88379	ACT-S128K32C-070P2Q
5962-9318704HYX	54230	WS128K32-70HSQ
5962-9318704HYX	88379	ACT-S128K32C-070P6Q
5962-9318704H4X	54230	WS128K32N-70H1Q
5962-9318704H5X	54230	WS128K32-70H1Q

Standard 1/ microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-9318705HMX	88379	ACT-S128K32N-055P3Q
5962-9318705HNX	88379	ACT-S128K32C-055P3Q
5962-9318705HTX	54230	WS128K32N-55HQ
5962-9318705HTX	88379	ACT-S128K32N-055P2Q
5962-9318705HUX	54230	WS128K32N-55HSQ
5962-9318705HUX	88379	ACT-S128K32N-055P6Q
5962-9318705HXX	54230	WS128K32-55HQ
5962-9318705HXX	88379	ACT-S128K32C-055P2Q
5962-9318705HYX	54230	WS128K32-55HSQ
5962-9318705HYX	88379	ACT-S128K32C-055P6Q
5962-9318705H4X	0EU86	AS8S128K32PN-55/883C
5962-9318705H4X	54230	WS128K32N-55H1Q
5962-9318705H4X	88379	ACT-S128K32N-055P7Q
5962-9318705H5X	0EU86	AS8S128K32P-55/883C
5962-9318705H5X	54230	WS128K32-55H1Q
5962-9318705H5X	88379	ACT-S128K32C-055P7Q
5962-9318706HMX	88379	ACT-S128K32N-045P3Q
5962-9318706HNX	88379	ACT-S128K32C-045P3Q
5962-9318706HTX	54230	WS128K32N-45HQ
5962-9318706HTX	88379	ACT-S128K32N-045P2Q
5962-9318706HUX	54230	WS128K32N-45HSQ
5962-9318706HUX	88379	ACT-S128K32N-045P6Q
5962-9318706HXX	54230	WS128K32-45HQ
5962-9318706HXX	88379	ACT-S128K32C-045P2Q
5962-9318706HYX	54230	WS128K32-45HSQ
5962-9318706HYX	88379	ACT-S128K32C-045P6Q
5962-9318706H4X	0EU86	AS8S128K32PN-45/883C
5962-9318706H4X	54230	WS128K32N-45H1Q
5962-9318706H4X	88379	ACT-S128K32N-045P7Q
5962-9318706H5X	0EU86	AS8S128K32P-45/883C
5962-9318706H5X	54230	WS128K32-45H1Q
5962-9318706H5X	88379	ACT-S128K32C-045P7Q
5962-9318707HMX	88379	ACT-S128K32N-035P3Q
5962-9318707HNX	88379	ACT-S128K32C-035P3Q
5962-9318707HTX	54230	WS128K32N-35HQ
5962-9318707HTX	88379	ACT-S128K32N-035P2Q
5962-9318707HUX	54230	WS128K32N-35HSQ
5962-9318707HUX	88379	ACT-S128K32N-035P6Q
5962-9318707HXX	54230	WS128K32-35HQ
5962-9318707HXX	88379	ACT-S128K32C-035P2Q
5962-9318707HYX	54230	WS128K32-35HSQ
5962-9318707HYX	88379	ACT-S128K32C-035P6Q
5962-9318707H4X	0EU86	AS8S128K32PN-35/883C
5962-9318707H4X	54230	WS128K32N-35H1Q
5962-9318707H4X	88379	ACT-S128K32N-035P7Q
5962-9318707H5X	0EU86	AS8S128K32P-35/883C
5962-9318707H5X	54230	WS128K32-35H1Q
5962-9318707H5X	88379	ACT-S128K32C-035P7Q

Standard 1/ microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-9318708HMX	88379	ACT-S128K32N-025P3Q
5962-9318708HNX	88379	ACT-S128K32C-025P3Q
5962-9318708HTX	54230	WS128K32N-25HQ
5962-9318708HTX	88379	ACT-S128K32N-025P2Q
5962-9318708HUX	54230	WS128K32N-HSQ
5962-9318708HUX	88379	ACT-S128K32N-025P6Q
5962-9318708HXX	54230	WS128K32-25HQ
5962-9318708HXX	88379	ACT-S128K32C-025P2Q
5962-9318708HYX	54230	WS128K32-25HSQ
5962-9318708HYX	88379	ACT-S128K32C-025P6Q
5962-9318708H4X	0EU86	AS8S128K32PN-25/883C
5962-9318708H4X	54230	WS128K32N-25H1Q
5962-9318708H4X	88379	ACT-S128K32N-025P7Q
5962-9318708H5X	0EU86	AS8S128K32P-25/883C
5962-9318708H5X	54230	WS128K32-25H1Q
5962-9318708H5X	88379	ACT-S128K32C-025P7Q
5962-9318709HMX	88379	ACT-S128K32N-020P3Q
5962-9318709HNX	88379	ACT-S128K32C-020P3Q
5962-9318709HTX	54230	WS128K32N-20HQ
5962-9318709HTX	88379	ACT-S128K32N-020P2Q
5962-9318709HUX	54230	WS128K32N-20HSQ
5962-9318709HUX	88379	ACT-S128K32N-020P6Q
5962-9318709HXX	54230	WS128K32-20HQ
5962-9318709HXX	88379	ACT-S128K32C-020P2Q
5962-9318709HYX	54230	WS128K32-20HSQ
5962-9318709HYX	88379	ACT-S128K32C-020P6Q
5962-9318709H4X	0EU86	AS8S128K32PN-20/883C
5962-9318709H4X	54230	WS128K32N-20H1Q
5962-9318709H4X	88379	ACT-S128K32N-020P7Q
5962-9318709H5X	0EU86	AS8S128K32P-20/883C
5962-9318709H5X	54230	WS128K32-20H1Q
5962-9318709H5X	88379	ACT-S128K32C-020P7Q
5962-9318710HMX	88379	ACT-S128K32N-017P3Q
5962-9318710HNX	88379	ACT-S128K32C-017P3Q
5962-9318710HTX	54230	WS128K32N-17HQ
5962-9318710HTX	88379	ACT-S128K32N-017P2Q
5962-9318710HUX	54230	WS128K32N-17HSQ
5962-9318710HUX	88379	ACT-S128K32N-017P6Q
5962-9318710HXX	54230	WS128K32-17HQ
5962-9318710HXX	88379	ACT-S128K32C-017P2Q
5962-9318710HYX	54230	WS128K32-17HSQ
5962-9318710HYX	88379	ACT-S128K32C-017P6Q
5962-9318710H4X	54230	WS128K32N-17H1Q
5962-9318710H4X	88379	ACT-S128K32N-017P7Q
5962-9318710H5X	54230	WS128K32-17H1Q
5962-9318710H5X	88379	ACT-S128K32C-017P7Q

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9318711H4X	54230	WS128K32N-15H1Q
5962-9318711H5X	54230	WS128K32-15H1Q

1/ The lead finish designator "X" shown for each PIN representing a hermetic package is available in the A or C lead finishes and are available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor Incorporated 8701 Cross Park Drive Austin, TX 78754-4566
54230	White Electronic Designs Corporation 3601 East University Drive Phoenix, AZ 85034
88379	Aeroflex Circuit Technology Corporation 35 South Service Road Plainview, NY 11803-4193

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