
HN62454N Series

262144-word $\times$ 16-bit/524288-word $\times$ 8-bit CMOS Mask
Programmable ROM

HITACHI

ADE-203-404B (Z)

Rev. 2.0

Jun. 26, 1997

Description

The Hitachi HN62454N series is a 4-Mbit CMOS mask programmable ROM organized either as 262144-word $\times$ 16-bit or as 524288-word $\times$ 8-bit. As it has realized high speed normal access 100 ns and page mode access 40 ns, it is the most suitable to the program and data memory for micro computer system. It has the package variations of standard 40-pin plastic DIP, standard 40-pin plastic SOP and standard 44-pin plastic TSOPII.

Features

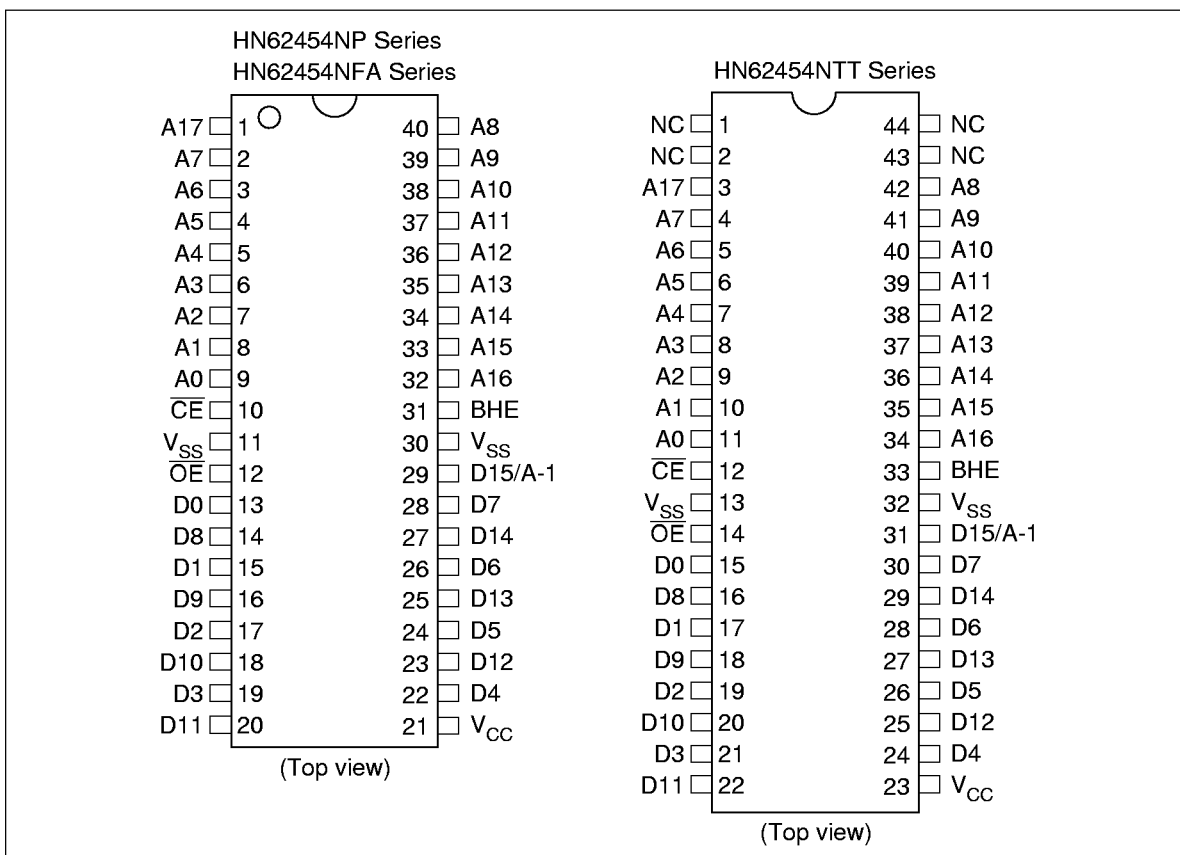
- Single 5 V supply : 5.0 V $\pm$ 10%
- Access time:
 - Normal access time: 100 ns (max)
 - Page access time: 40 ns (max)
- Power dissipation
 - Active: 550 mW (max)
 - Standby: 165 μ W (max)
- Byte-wide or word-wide data organization with byte/word selection (BHE)
- 4-word page access on word-wide mode
- 8-byte page access on byte-wide mode
- Three-state data output for wired or-tying
- Directly TTL compatible all inputs and outputs

Ordering Information

Type No.	Access time	Package
HN62454NP-10	100 ns	600-mil 40-pin plastic DIP (DP-40)
HN62454NFA-10	100 ns	525-mil 40-pin plastic SOP (FP-40D)
HN62454NTT-10	100 ns	400-mil 44-pin plastic TSOPII (TTP-44D)

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Pin Arrangement



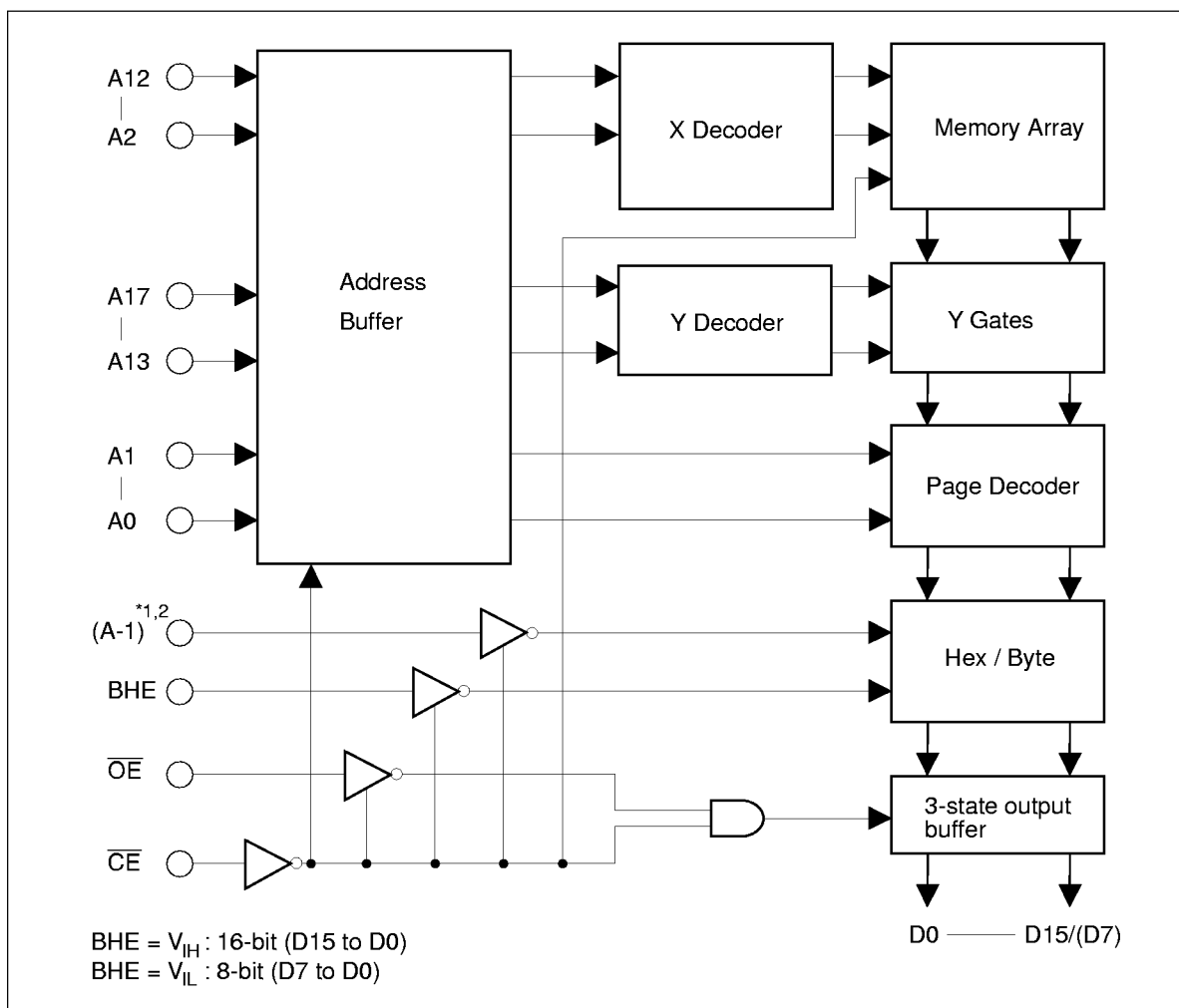
Pin Description

Pin name	Function
A2 to A17	Address input
A-1, A0, A1	Page address input
D0 to D15	Data output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word selection
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram

Notes: 1. A-1 is least significant address.

2. When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.



Operation Table

Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	Data output		Address input	
					D0-D7	D8-D15	LSB	MSB
Standby	H	$\times^{*1}$	$\times$	$\times$	High-Z	High-Z	—	—
Output disable	L	H	$\times$	$\times$	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

Note: 1. $\times$: Don't care.

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.3 to +7.0	V
All input and output voltage relative to V_{SS}	V_{in} , V_{out}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	-55 to +125	°C
Temperature range under bias	T_{bias}	-20 to +85	°C

DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	-0.3	—	0.8	V

DC Characteristics ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = 0$ to +70°C)

Parameter	Symbol	Min	Max	Unit	Test conditions
Operating V_{CC} current	I_{CC}	—	100	mA	$V_{CC} = 5.5 \text{ V}$, $I_{DOUT} = 0 \text{ mA}$, $t_{RC} = 100 \text{ ns}$
Standby V_{CC} current	I_{SB1}	—	30	μA	$V_{CC} = 5.5 \text{ V}$, $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$
	I_{SB2}	—	3	mA	$V_{CC} = 5.5 \text{ V}$, $\overline{CE} \geq 2.2 \text{ V}$
Input leakage current	$ I_{IL} $	—	10	μA	$V_{in} = 0$ to V_{CC}
Output leakage current	$ I_{OL} $	—	10	μA	$\overline{CE} = 2.2 \text{ V}$, $V_{OUT} = 0$ to V_{CC}
Output high voltage	V_{OH}	2.4	—	V	$I_{OH} = -205 \text{ μA}$
Output low voltage	V_{OL}	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$

Capacitance ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = 25^\circ\text{C}$, $V_{in} = 0 \text{ V}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{in}	—	10	pF
Output capacitance	C_{out}	—	15	pF

AC Characteristics ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = 0 \text{ to } +70^\circ\text{C}$)**Test Conditions**

- Input pulse levels: 0.4 to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1TTL + $C_L = 100 \text{ pF}$ (including jig)

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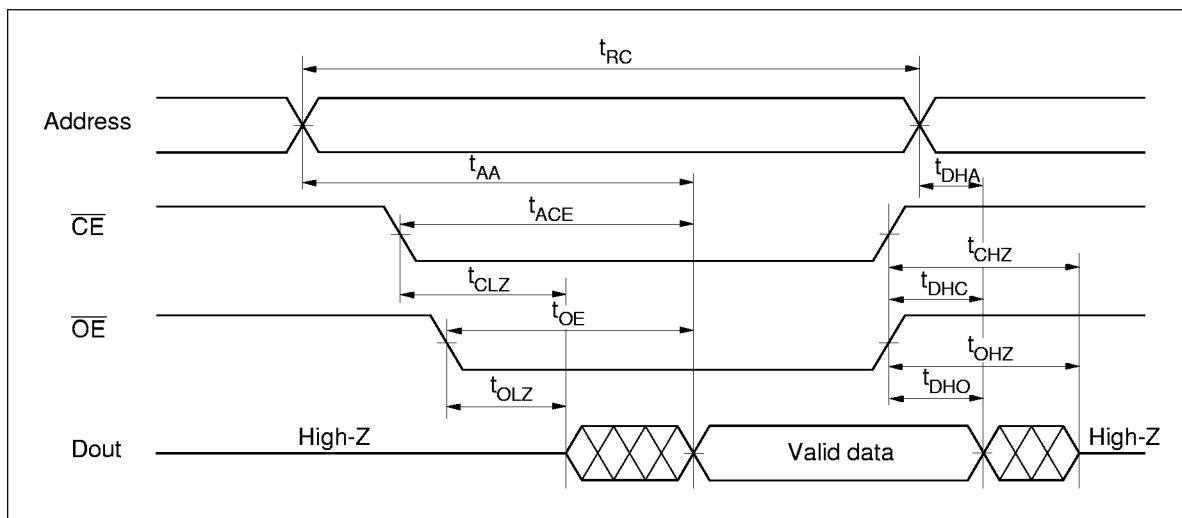
Read Cycle

Parameter	Symbol	HN62454N-10		Unit	Notes
		Min	Max		
Read cycle time	t_{RC}	100	—	ns	
Page read cycle time	t_{PC}	40	—	ns	
Address access time	t_{AA}	—	100	ns	3
Page address access time	t_{PA}	—	40	ns	
$\overline{CE}$ access time	t_{ACE}	—	100	ns	3
$\overline{OE}$ access time	t_{OE}	—	40	ns	3
BHE access time	t_{BHE}	—	100	ns	
Output hold time from address change	t_{DHA}	0	—	ns	2
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns	2
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns	2
Output hold time from BHE	t_{DHB}	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	30	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	30	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	ns	4
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	ns	4
BHE to output in low-Z	t_{BLZ}	5	—	ns	

- Notes: 1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.
2. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
3. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
4. t_{CLZ} , t_{OLZ} : Determined by slower.
5. $\overline{CE}$ and $\overline{OE}$ are enable A17 to A0 are valid.
6. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must be applied to them.
7. Page address is determined as below.
 Word mode (BHE = 'V_{IH}'): A0, A1
 Byte mode (BHE = 'V_{IL}'): A-1, A0, A1
8. $\overline{CE}$ and $\overline{OE}$ are enable.

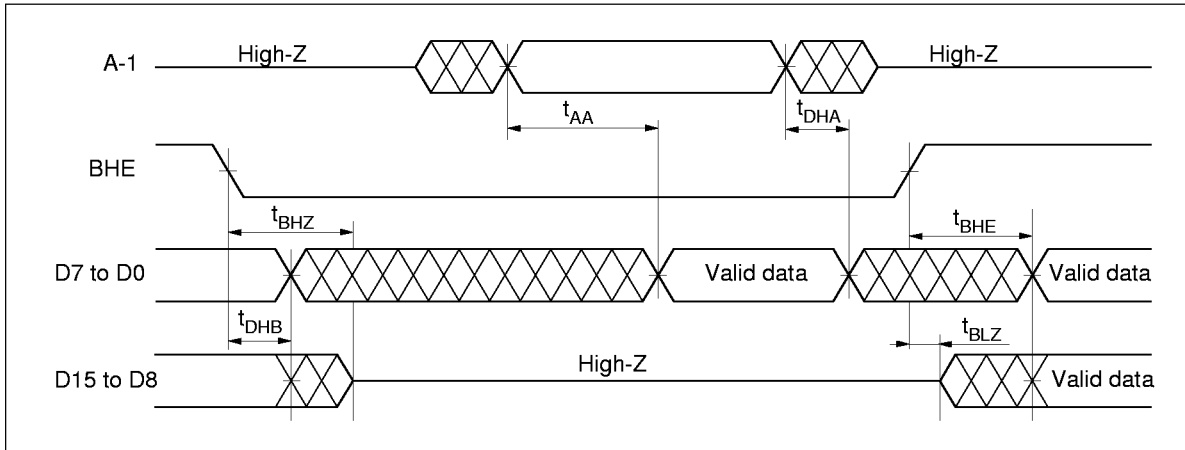
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')*2, 3, 4

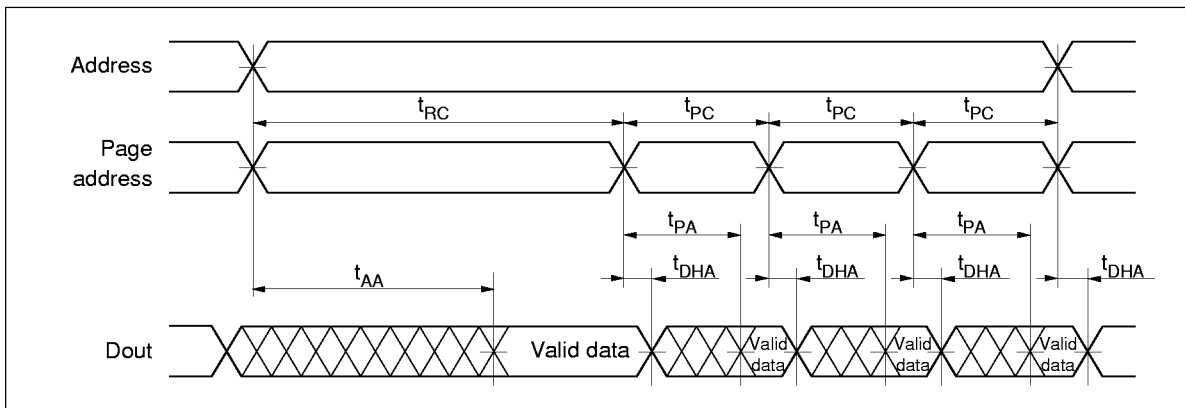


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Word Mode, Byte Mode Switch^{*5, 6}



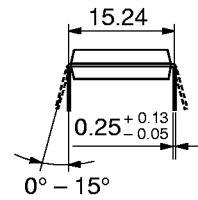
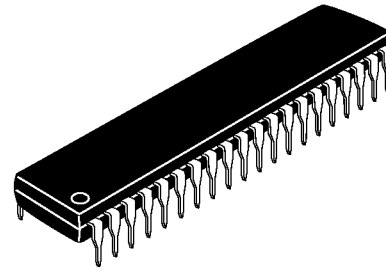
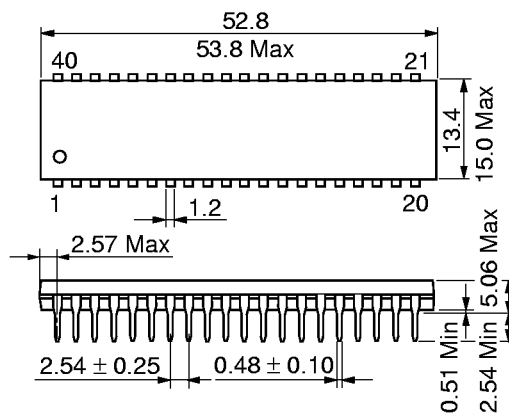
Page Mode^{*7, 8}



Package Dimensions

HN62454NP Series (DP-40)

Unit: mm



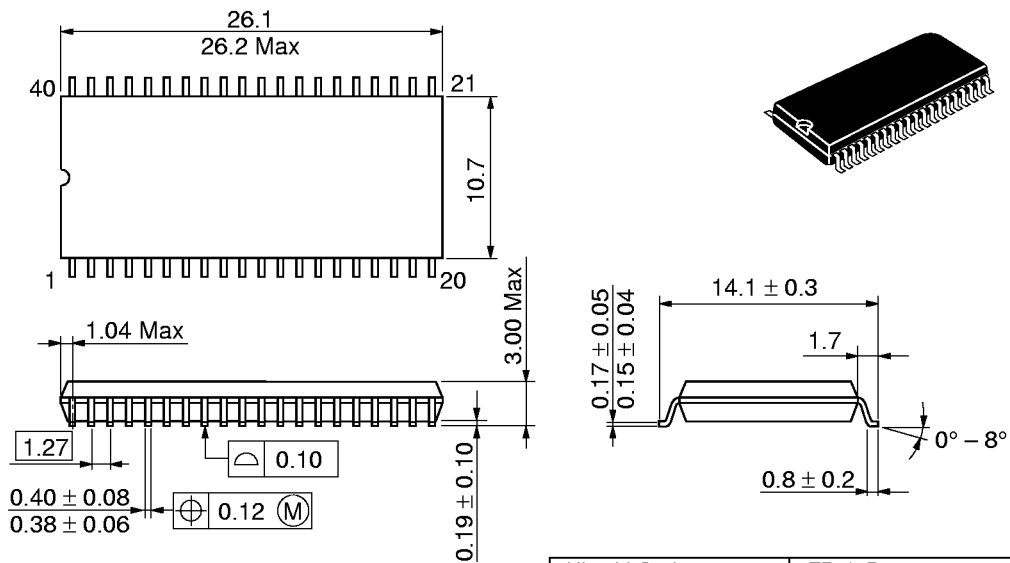
Hitachi Code	DP-40
JEDEC Code	MO-015J Mod.
EIAJ Code	SC-511-40D
Weight (reference value)	6.0 g

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Package Dimensions (cont.)

HN62454NFA Series (FP-40D)

Unit: mm

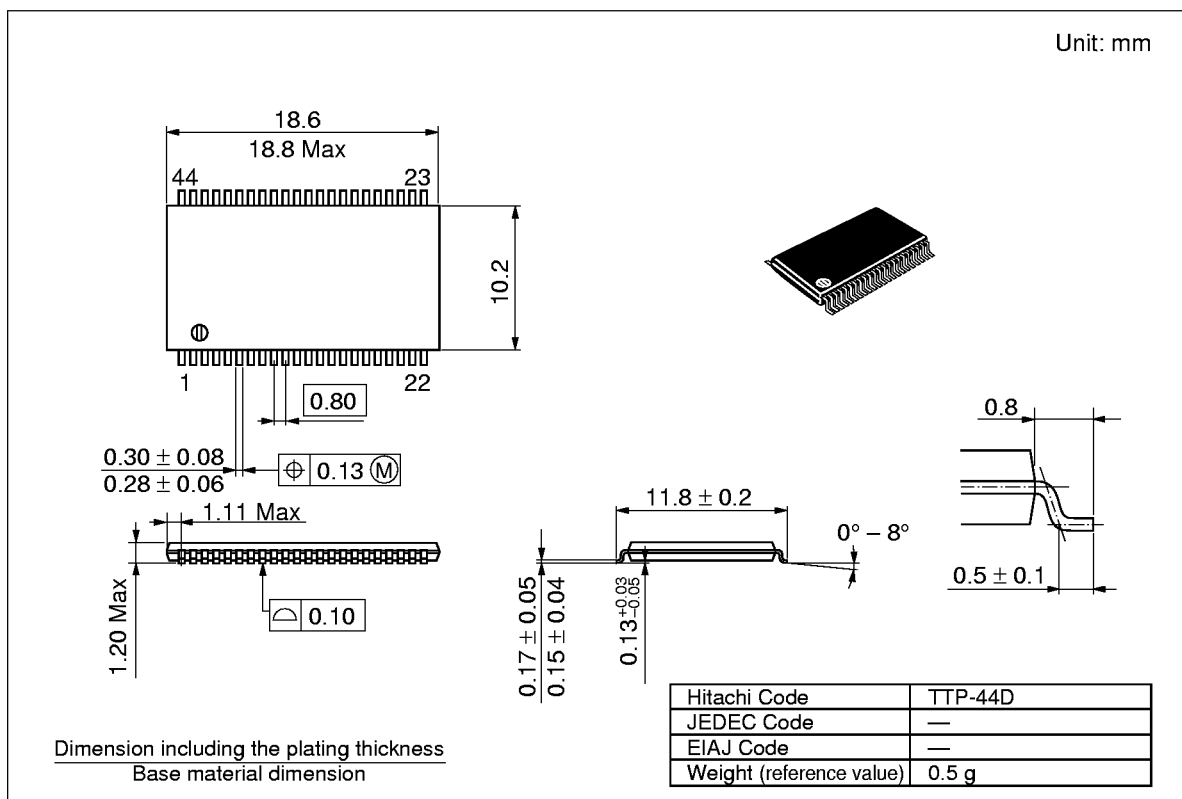


Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-40D
JEDEC Code	—
EIAJ Code	—
Weight (reference value)	1.5 g

Package Dimensions (cont.)

HN62454NTT Series (TTP-44D)



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 20, 1995	Initial issue	M. Shirai	T. Wada
0.1	Jul. 19, 1995	Change of Type No. HN62454NP-8 to HN62454NP-85 HN62454NFP-8 to HN62454NFP-85 HN62454NTT-8 to HN62454NTT-85 DC Characteristics I_{CC} Test condition: $t_{RC} = 80/100$ ns to $t_{RC} = 85/100$ ns AC Characteristics t_{RC} (min): 80/100 ns to 85/100 ns t_{AA} (max): 80/100 ns to 85/100 ns t_{ACE} (max): 80/100 ns to 85/100 ns t_{BHE} (max): 80/100 ns to 85/100 ns	M. Shirai	T. Wada
1.0	May. 21, 1996	Change of Format Deletion of HN62454N-85 Series DC Characteristics I_{CC} (max): 120/100 ns to 100 ns I_{CC} Test condition: $t_{RC} = 85/100$ ns to $t_{RC} = 100$ ns	M. Shirai	T. Wada
2.0	Jun. 26, 1997	Operation Table Deletion of note 2 Capacitance Deletion of note AC Characteristics Test Condition: Input pulse levels: 0.45 V to 2.4 V to 0.4 V to 2.4 V		