REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Change V_{IL}, tp(clock), f_{MAX}, and propagation delay limits. Delete minimum limits from I_{IL} and propagation delays. Convert to military drawing format. Case E inactive for new design	87-03-03	D. Cool
D	Change drawing CAGE number to 67268. Change I_{IL} condition. Change t_{PLH2}. Correct vendor p/n. Case 2, device types 01 and 02 are inactive.	87-12-01	D. Cool
E	Change clock pulse and setup times. Split V_{IL} into temperatures. Change propagation delays. Add footnotes to table I. Change footnote 1/ in 1.3. Add figure 5. Editorial changes throughout. Delete CAGE number 04713. Add CAGE numbers 18324 and 27014. Change in t_{PLH}CLK, t_s (device 03), I_{IH}, I_{CC}, f_{MAX}, and figure 2. Change in table II.	88-05-28	D. Cool
F	Technical change in table I, t_{PLZ}, device 03. Added clarification to voltage waveforms. Added a source to device type 03. Editorial changes throughout.	89-10-17	W. Heckman
G	Technical change in table I, I_O. Change to the truth table in figure 2. Clarify the note in figure 2. Editorial changes throughout.	92-07-16	M. L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	G	G	G	G	G	G	G	G											
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS	REV	G	E	E	G	G	G	G	G	G	G	G	G	G	G
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
30 April 1984

REVISION LEVEL
G

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, BIPOLAR, ADVANCED LOW-POWER SCHOTTKY TTL, COUNTERS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	83022

SHEET 1 OF 22

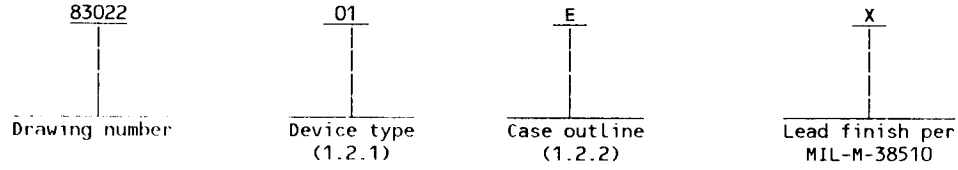
DESC FORM 193
JUL 91

5962-E463

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALS161	Synchronous 4-bit binary counter with asynchronous clear
02	54ALS163	Synchronous 4-bit binary counter with synchronous clear
03	54ALS561	Synchronous 4-bit binary counter with three-state outputs

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, (P_D) 1/:	
Device type 01	115.5 mW
Device type 02	137.5 mW
Device type 03	209 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit test; e.g., I_O.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL}):	
V_{IL} = +125°C	0.7 V dc
V_{IL} = +25°C	0.8 V dc
V_{IL} = -55°C	0.8 V dc
Width of clock pulse (t_p CLK):	
Device types 01 and 02	20 ns minimum
Device type 03:	
High	20 ns minimum
Low	25 ns minimum
Width of asynchronous clear pulse (t_p $\overline{ACLR}$), t_p $\overline{CLR}$	
Device types 01, and 03	20 ns minimum
Width of asynchronous load pulse (t_p $\overline{ALOAD}$):	
Device type 03	20 ns minimum
Setup times before clock:	
Data:	
Device types 01 and 02	20 ns minimum
Device type 03	25 ns minimum
Synchronous CLR; SCLR	
Low:	
Device type 02	20 ns minimum
Device type 03	21 ns minimum
Inactive:	
Device type 02	20 ns minimum
Device type 03	35 ns minimum
Asynchronous CLR, ACLR	
Inactive:	
Device types 01 and 03	10 ns minimum
Asynchronous ALOAD:	
Inactive:	
Device type 03	12 ns minimum
Synchronous LOAD:	
Device types 01 and 02	20 ns minimum
Low:	
Device type 03	20 ns minimum
Inactive:	
Device type 03	35 ns minimum
ENP/ENT:	
Low:	
Device types 01 and 03	25 ns minimum
Device type 02	20 ns minimum
High:	
Device types 01 and 03	25 ns minimum
Hold times (t_h):	
Device types 01, 02, and 03	0 ns minimum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY
MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY
MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Counting sequence. The counting sequence shall be as specified on figure 4.

3.2.6 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
High level output voltage	V_{OH1}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL}: at -55°C = 0.8 V +25°C = 0.8 V +125°C = 0.7 V	I_{OH} = -0.4 mA 2/	1, 2, 3	01, 02	2.5		V
			I_{OH} = -0.4 mA RCO and CCO		03	2.5		V
	V_{OH2}		I_{OH} = -1.0 mA Q outputs		03	2.4		V
Low level output voltage	V_{OL1}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL}: at -55°C = 0.8 V +25°C = 0.8 V +125°C = 0.7 V	I_{OL} = 4.0 mA 2/ All outputs		01, 02		0.4	V
			I_{OL} = 4.0 mA RCO and CCO		03		0.4	V
	V_{OL2}		I_{OL} = 12 mA Q outputs		03		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA			All		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.4 V unused inputs = 4.5 V			All		-0.2	mA
High level input current	I_{IH1}	V_{CC} = 5.5 V V_{IN} = 2.7 V unused inputs = 0.0 V	$\overline{LOAD}$, CLK, ENT		01, 02		20	μA
			ENT/ENP		03		40	μA
			All other inputs		All		20	μA
	I_{IH2}	V_{CC} = 5.5 V V_{IN} = 7.0 V unused inputs = 0.0 V	$\overline{LOAD}$, CLK, ENT		01, 02		0.1	mA
			ENT/ENP		03		0.2	mA
			All other inputs		All		0.1	mA
Output current	I_O	V_{CC} = 5.5 V, V_{OUT} = 2.25 V 3/	Q outputs		All	-20	-112	mA
			RCO and CCO outputs		03	-15	-100	mA
Off-state output current	I_{OZL}	V_{CC} = 5.5 V V_{OUT} = 0.4 V	Q outputs		03		-20	μA
	I_{OZH}	V_{CC} = 5.5 V V_{OUT} = 2.7 V			03		20	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	01		21	mA
				02		25	
	I_{CCH}			03		35	mA
	I_{CCL}					38	
	I_{CCZ}					36	
Functional tests		See 4.3.1c 4/	7, 8	All			
Maximum input clock or count up frequency	f_{MAX}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500Ω See figures 4 and 5 5/	9, 10, 11	01	25		MHz
				02	35		
				03	20		
Propagation delay time, CLK to Q	t_{pLH1}			01	4	15	ns
				02	4	21	
				03	4	15	
	t_{pHL1}			01	6	20	ns
				02	6	25	
				03	5	21	
Propagation delay time, CLK to RCO	t_{pLH2}			01	5	24	ns
				02, 03	5	35	
	t_{pHL2}			01	5	20	ns
				02	5	26	
				03	8	29	
Propagation delay time, CLK to CCO	t_{pLH3}			03	8	35	ns
	t_{pHL3}			03	5	20	
Propagation delay time, ALOAD to Q	t_{pLH4}			03	10	38	ns
	t_{pHL4}			03	7	27	
Propagation delay time, ALOAD to RCO	t_{pLH5}			03	15	55	ns
	t_{pHL5}			03	12	35	
Propagation delay time, ALOAD to CCO	t_{pLH6}			03	25	65	ns
	t_{pHL6}			03	12	42	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Propagation delay time, DATA to Q	t_{pLH7}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500Ω See figures 4 and 5 5/	9, 10, 11	03	8	35	ns
	t_{pHL7}			03	7	29	
Propagation delay time, ENT to RCO	t_{pLH8}			01	3	13	ns
				02	3	20	
				03	5	20	
	t_{pHL8}			01	3	13	ns
				02	3	16	
				03	4	18	
Propagation delay time, ENT to CCO	t_{pLH9}			03	12	35	ns
	t_{pHL9}			03	4	25	
Propagation delay time, ENP to CCO	t_{pLH10}			03	5	22	ns
	t_{pHL10}			03	4	14	
Propagation delay time, CLR to Q	t_{pHL11}			01	8	24	ns
				03	7	28	
Propagation delay time, CLR to RCO	t_{pHL12}			01	11	24.5	ns
Output enable time, G to Q	t_{pZH}			03	5	24	ns
	t_{pZL}			03	8	28	
Output disable time, G to Q	t_{pHZ}			03	2	15	ns
	t_{pLZ}			03	2	20	

1/ Unused inputs that do not directly control the pin under test must be $\ge$ 2.5 V or $\le$ 0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.

2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or the V_{IH} minimum input.

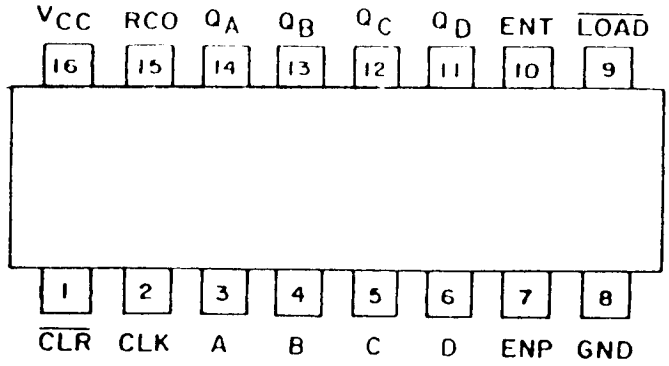
3/ The output conditions have been chosen to produce a current that closely approximates one-half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and the duration of the test condition shall not exceed 1 second.

4/ Functional tests shall be conducted at input test conditions of GND $\le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.

5/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or $\le$ 0.3 V.

Device types 01 and 02

Cases E and F



Device types 01 and 02

Case 2

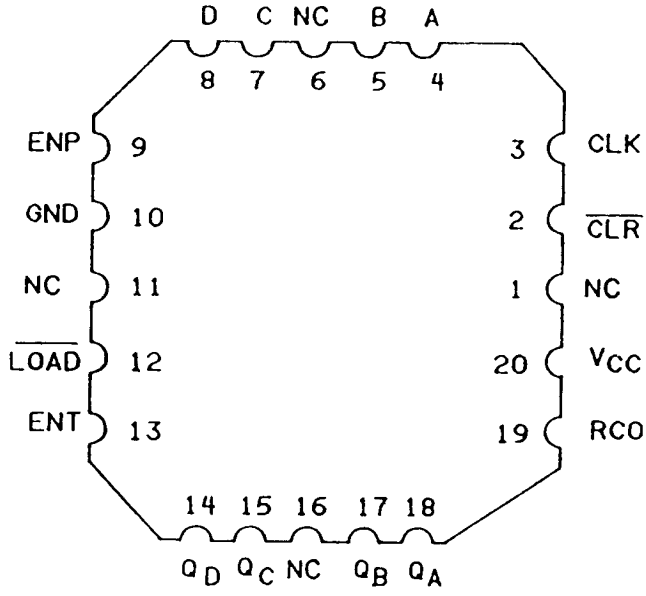
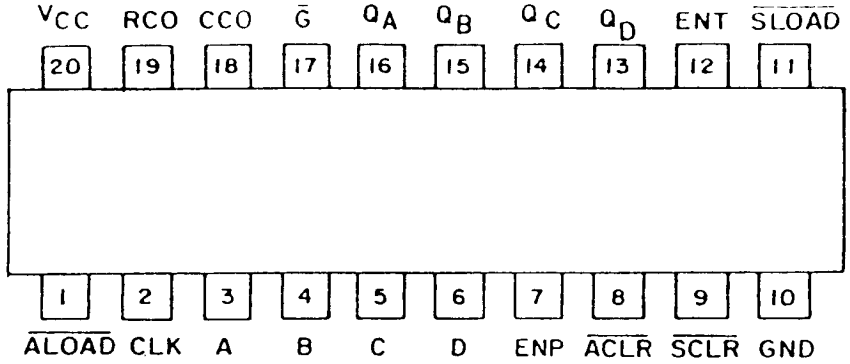


FIGURE 1. Terminal connections (top view).

Device type 03

Cases R and S



Device type 03

Case 2

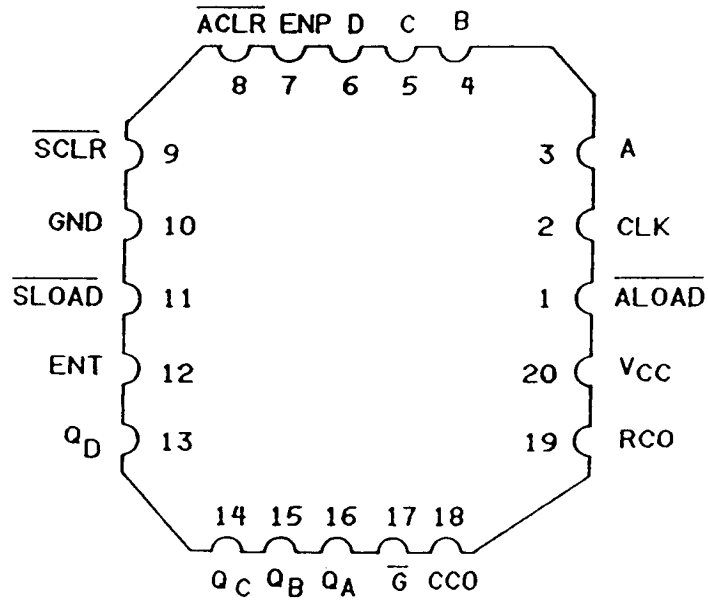


FIGURE 1. Terminal connections (top view) - Continued.

Device types 01 and 02

Synchronous truth table

Inputs at time t_n									Outputs at time t_{n+1}				
CLK	ENP	ENT	$\overline{LOAD}$	A	B	C	D	$\overline{CLR}$	Q_A	Q_B	Q_C	Q_D	RCO
CP	L	X	H	X	X	X	X	H	NC	NC	NC	NC	NC
CP	X	L	H	X	X	X	X	H	NC	NC	NC	NC	L
CP	H	H	H	X	X	X	X	H	Previous count plus 1 See up count sequence table				H if count = 15 L if count < 15
CP	X	H	L	X	X	X	X	H	A	B	C	D	H if count = 15 L if count < 15
CP	X	L	L	X	X	X	X	H	A	B	C	D	L

Device type 01

Asynchronous truth table (clear function)

Inputs at time t_n									Outputs at time t_{n+1}				
CLK	ENP	ENT	$\overline{LOAD}$	A	B	C	D	$\overline{CLR}$	Q_A	Q_B	Q_C	Q_D	RCO
X	X	X	X	X	X	X	X	L	L	L	L	L	L

Device type 02

Synchronous truth table (clear function)

Inputs at time t_n									Outputs at time t_{n+1}				
CLK	ENP	ENT	$\overline{LOAD}$	A	B	C	D	$\overline{CLR}$	Q_A	Q_B	Q_C	Q_D	RCO
CP	X	X	X	X	X	X	X	L	L	L	L	L	L

L = V_{IL} for inputs, V_{OL} for outputs.
H = V_{IH} for inputs, V_{OH} for outputs.
X = V_{IH} or V_{IL}.
CP = Clock pulse.
NC = No change.

FIGURE 2. Truth tables.

Device types 01 and 02

Up count sequence table

Q_A (LSB)	Q_B	Q_C	Q_D (MSB)
L	L	L	L
H	L	L	L
L	H	L	L
H	H	L	L
L	L	H	L
H	L	H	L
L	H	H	L
H	H	H	L
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth tables - Continued.

Device type 03

Operation	$\overline{G}$	$\overline{ACLR}$	$\overline{ALOAD}$	$\overline{SCLR}$	$\overline{SLOAD}$	ENT	ENP	CLK	A	B	C	D	Q_A	Q_B	Q_C	Q_D	RCO	CCO
Q outputs disabled	H	X	X	X	X	H	X	X	X	X	X	X	Z	Z	Z	Z	H if cnt = 15 L if cnt ≠ 15	See note 2
See note 1	H	H	H	H	H	H	H	H										
Asynchronous clear	L	L	X	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L
Asynchronous load	L	H	L	X	X	H	X	X	X	X	X	X	A	B	C	D	H if cnt = 15 L if cnt ≠ 15	See note 2
Synchronous clear	L	H	H	L	X	X	X	↑	X	X	X	X	L	L	L	L	L	L
Synchronous load	L	H	H	H	L	H	X	↑	X	X	X	X	A	B	C	D	H if cnt = 15 L if cnt ≠ 15	See note 2
Count	L	H	H	H	H	H	H	↑	X	X	X	X	Previous count plus 1				H if cnt = 15 L if cnt ≠ 15	See note 2
Inhibit counting	L	H	H	H	H	H	L	X	X	X	X	X	No change				H if cnt = 15 L if cnt ≠ 15	See note 2
						L	X										L	

NOTES:

1. Counting continues.
2. CCO produces a high level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enable, otherwise CCO is low.

FIGURE 2. Truth tables - Continued.

Device type 03

Count up sequence					
Q_D	Q_C	Q_B	Q_A	RCO	CCO
L	L	L	L	L	L
L	L	L	H	L	L
L	L	H	L	L	L
L	L	H	H	L	L
L	H	L	L	L	L
L	H	L	H	L	L
L	H	H	L	L	L
L	H	H	H	L	L
H	L	L	L	L	L
H	L	L	H	L	L
H	L	H	L	L	L
H	L	H	H	L	L
H	H	L	L	L	L
H	H	L	H	L	L
H	H	H	L	L	L
H	H	H	H	H	See note

NOTE: CCO produces a high level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled, otherwise CCO is low.

FIGURE 2. Truth tables - Continued.

Device type 01

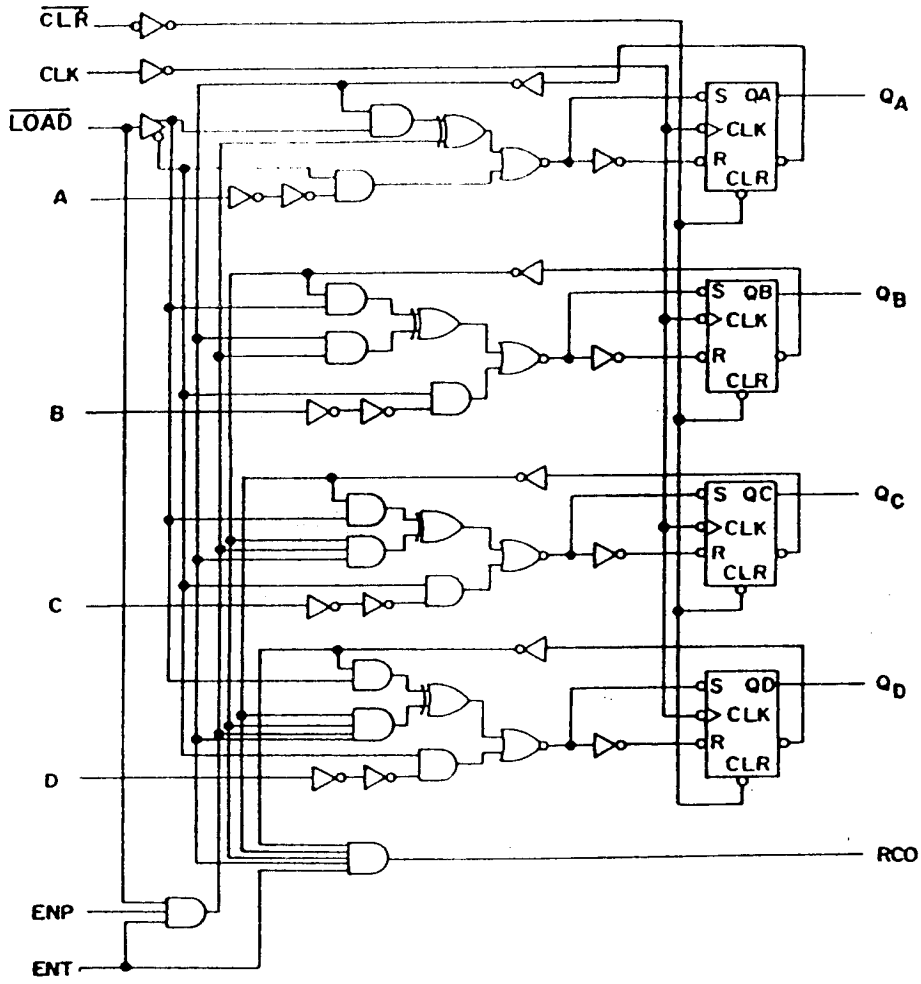


FIGURE 3. Logic diagrams.

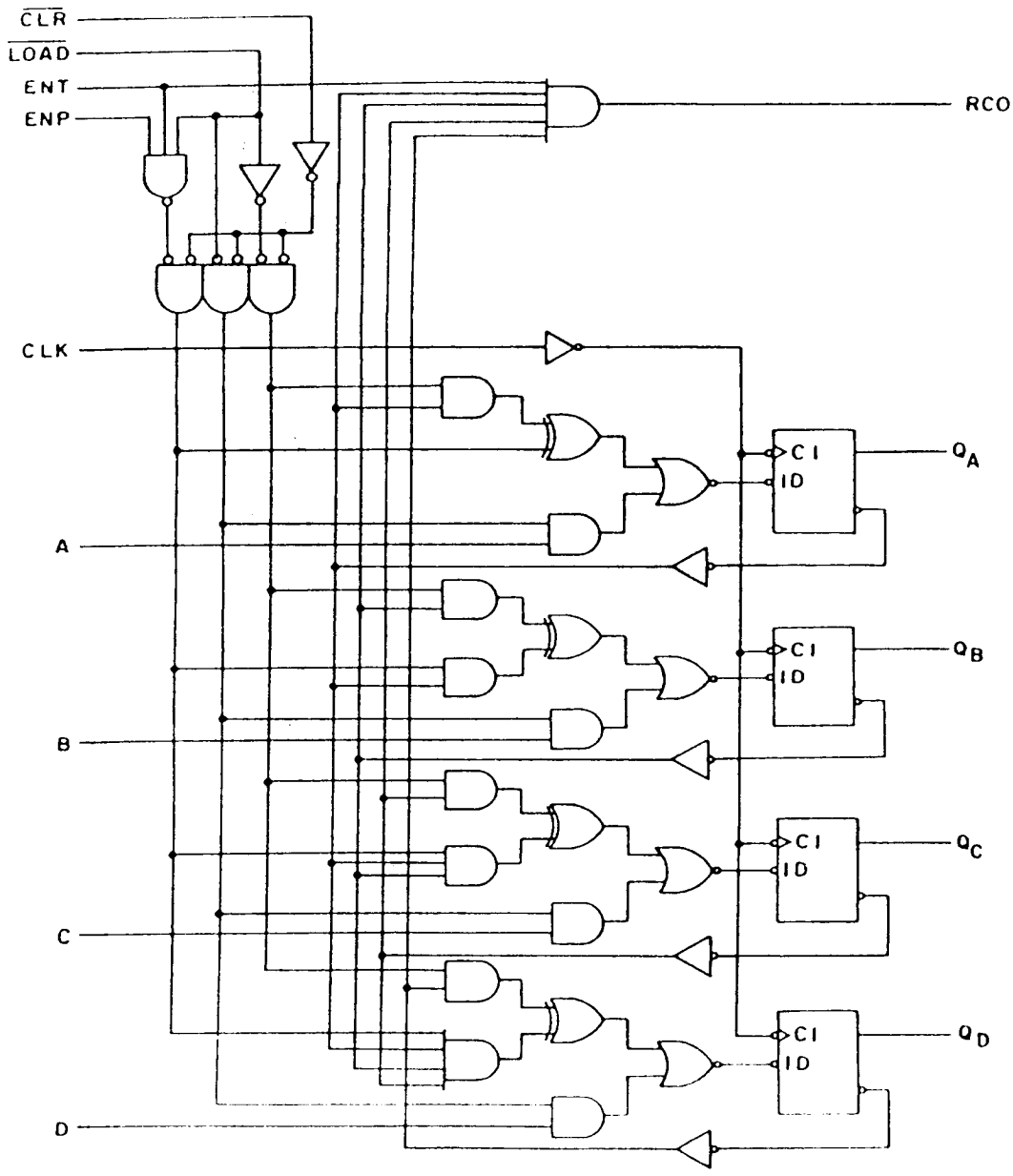


FIGURE 3. Logic diagrams - Continued.

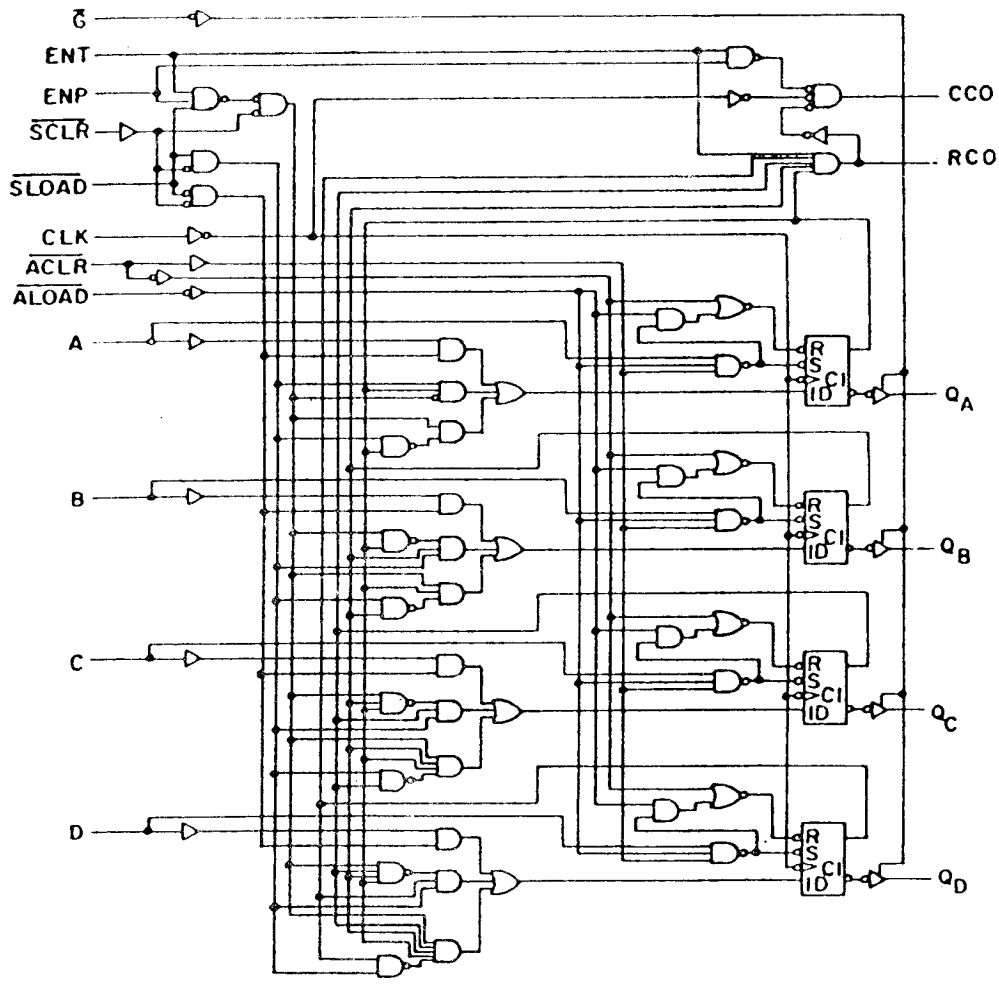


FIGURE 3. Logic diagrams - Continued.

Device types 01 and 02

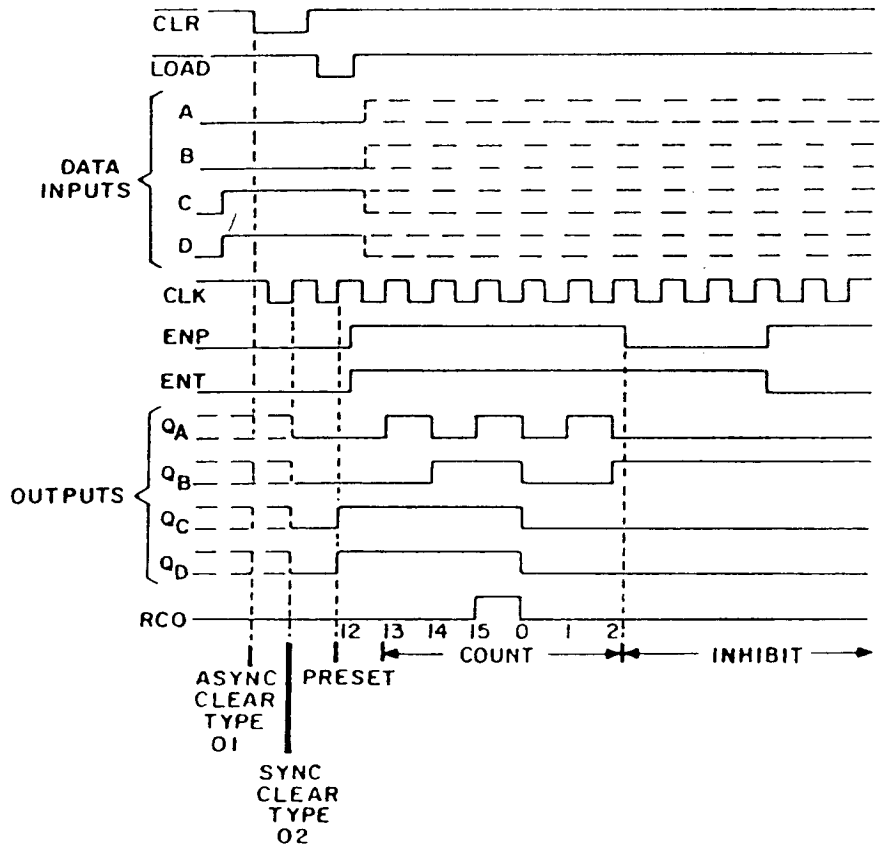


FIGURE 4. Counting sequence.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		83022
		REVISION LEVEL G	SHEET 17

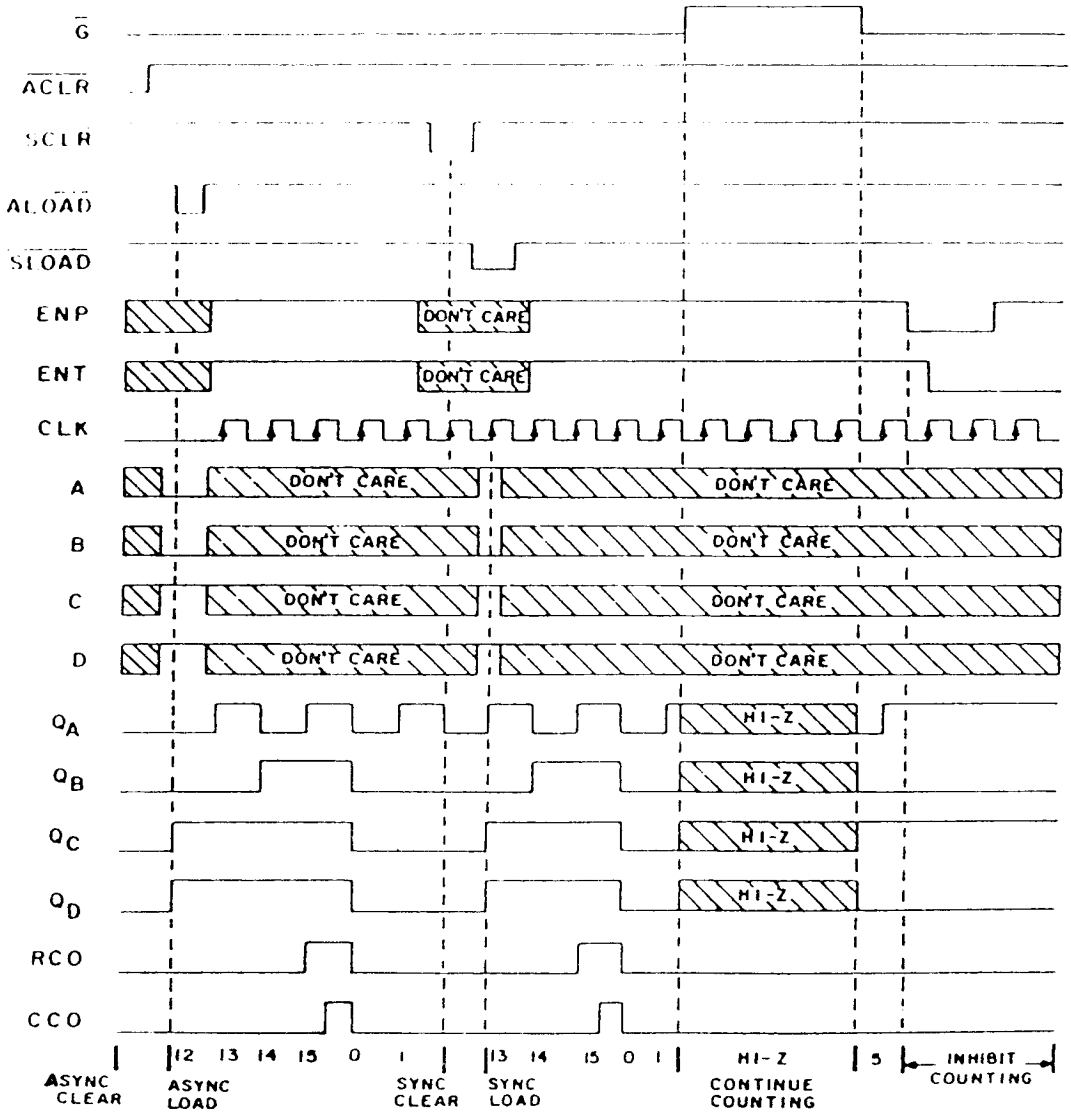
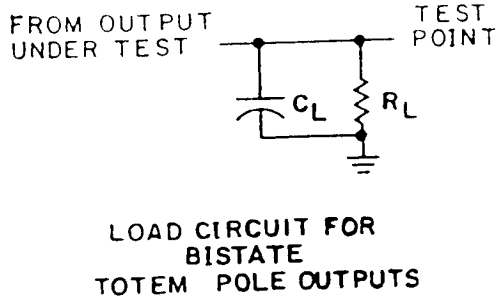
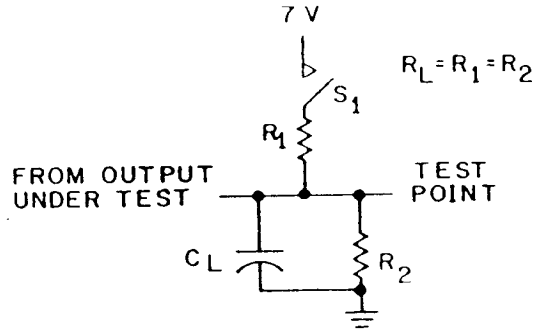


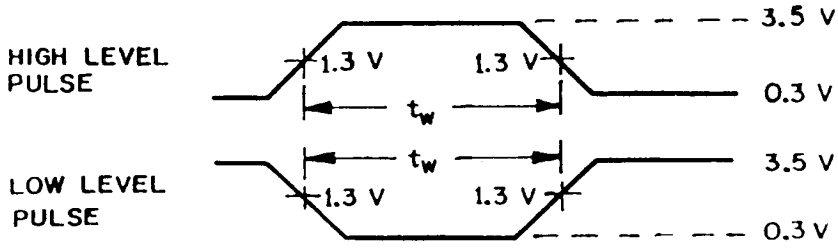
FIGURE 4. Counting sequence - Continued.

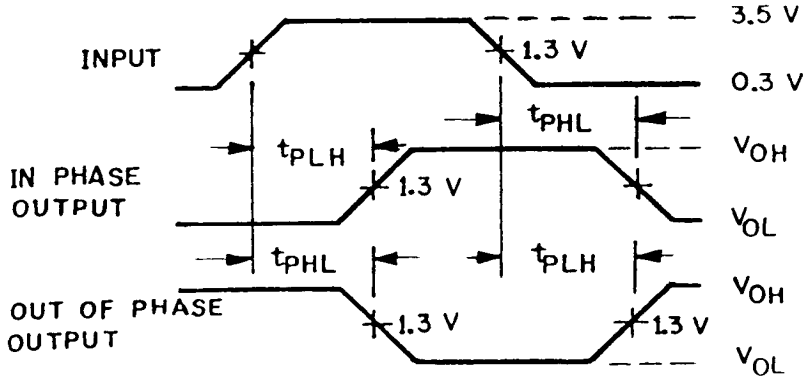


LOAD CIRCUIT FOR
BISTATE
TOTEM POLE OUTPUTS



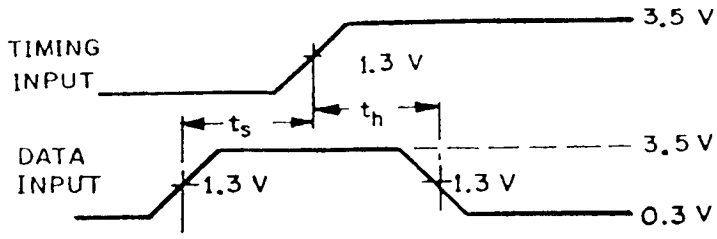
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

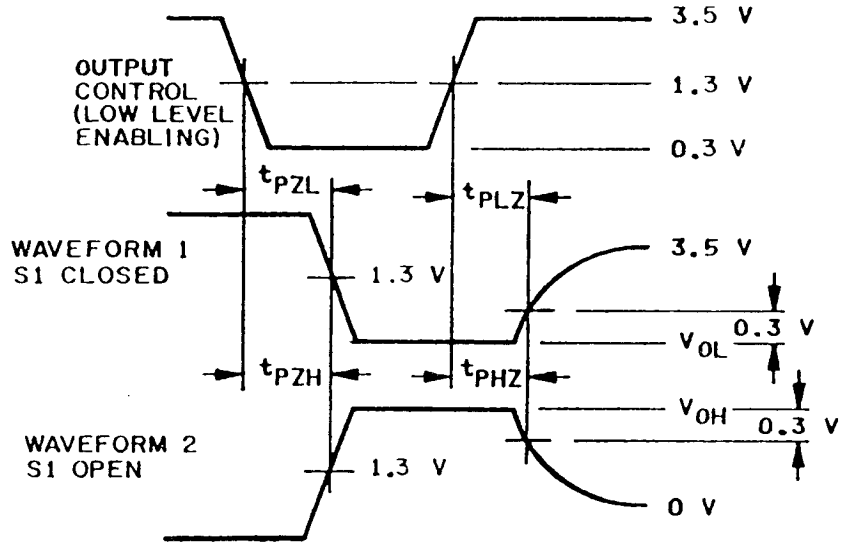




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

FIGURE 5. Test circuit and switching waveforms.





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE STATE OUTPUTS

NOTES:
1. C_L includes probe and jig capacitance.
2. All inputs have the following characteristics: PRRR ≤ 10 MHz, duty cycle = 50 percent, $t_r = t_f = 3 \pm 1$ ns.
3. The output are measured one at a time with one input transition per measurement.
4. Waveform 1 is for an output with internal conditions such that the output is low when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. When measuring propagation delay times of three-state outputs, switch S1 is open.

FIGURE 5. Test circuit and switching waveforms - Continued.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5005)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the device specified in this drawing will be replaced by the microcircuit identified as PIN M38510/3800XB--.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone 513-296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.