512MB- 64Mx64 SDRAM, UNBUFFERED W/PLL

FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3 volt $\pm$ 0.3v Power Supply
- 144 Pin SO-DIMM JEDEC

DESCRIPTION

The WED3DG6464V is a 64Mx64 synchronous DRAM module which consists of eight 64Mx8 stack SDRAM components in TSOP- 11 package, and one 2K EEPROM in an 8- pin TSSOP package for Serial Presence Detect which are mounted on a 144 Pin SO-DIMM multilayer FR4 Substrate.

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

PINOUT

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	VSS	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	VCC	102	VCC
7	DQ2	8	DQ34	55	VSS	56	VSS	103	A6	104	A7
9	DQ3	10	DQ35	57	NC	58	NC	105	A8	106	BA0
11	VCC	12	VCC	59	NC	60	NC	107	VSS	108	VSS
13	DQ4	14	DQ36	61	CLK0	62	CKE0	109	A9	110	BA1
15	DQ5	16	DQ37	63	VCC	64	VCC	111	A10	112	A11
17	DQ6	18	DQ38	65	RAS\	66	CAS\	113	VCC	114	VCC
19	DQ7	20	DQ39	67	WE\	68	CKE1	115	DQM2	116	DQM6
21	VSS	22	VSS	69	CS0\	70	A12	117	DQM3	118	DQM7
23	DQM0	24	DQM4	71	CS1\	72	NC	119	VSS	120	VSS
25	DQM1	26	DQM5	73	NC	74	NC	121	DQ24	122	DQ56
27	VCC	28	VCC	75	VSS	76	VSS	123	DQ25	124	DQ57
29	A0	30	A3	77	NC	78	NC	125	DQ26	126	DQ58
31	A1	32	A4	79	NC	80	NC	127	DQ27	128	DQ59
33	A2	34	A5	81	VCC	82	VCC	129	VCC	130	VCC
35	VSS	36	VSS	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	VSS	92	VSS	139	VSS	140	VSS
45	VCC	46	VCC	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	VCC	144	VCC

PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0	Clock input
CKE0, CKE1	Clock Enable input
$\overline{CS0}$, $\overline{CS1}$	Chip select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0-7	DQM
VDD	Power Supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM

CS1
CS0
DQM0

| DM | CS# | DQS |

DQ0 — DQ0
DQ1 — DQ1
DQ2 — DQ2   U0   U8
DQ3 — DQ3
DQ4 — DQ4
DQ5 — DQ5
DQ6 — DQ6
DQ7 — DQ7

DQM1

DQ8 — DQ0
DQ9 — DQ1
DQ10 — DQ2   U1   U9
DQ11 — DQ3
DQ12 — DQ4
DQ13 — DQ5
DQ14 — DQ6
DQ15 — DQ7

DQM2

Q16 — DQ0
Q17 — DQ1
Q18 — DQ2   U2   U10
Q19 — DQ3
Q20 — DQ4
Q21 — DQ5
Q22 — DQ6
Q23 — DQ7

DQM3

DQ24 — DQ0
DQ25 — DQ1
DQ26 — DQ2   U3   U11
DQ27 — DQ3
DQ28 — DQ4
DQ29 — DQ5
DQ30 — DQ6
DQ31 — DQ7

DQM4

DQ32 — DQ0
DQ33 — DQ1
DQ34 — DQ2   U4   U12
DQ35 — DQ3
DQ36 — DQ4
DQ37 — DQ5
DQ38 — DQ6
DQ39 — DQ7

DQM5

DQ40 — DQ0
DQ41 — DQ1
DQ42 — DQ2   U5   U13
DQ43 — DQ3
DQ44 — DQ4
DQ45 — DQ5
DQ46 — DQ6
DQ47 — DQ7

DQM6

DQ48 — DQ0
DQ49 — DQ1
DQ50 — DQ2   U6   U14
DQ51 — DQ3
DQ52 — DQ4
DQ53 — DQ5
DQ54 — DQ6
DQ55 — DQ7

DQM7

DQ56 — DQ0
DQ57 — DQ1
DQ58 — DQ2   U7   U15
DQ59 — DQ3
DQ60 — DQ4
DQ61 — DQ5
DQ62 — DQ6
DQ63 — DQ7

CLK0 — PLL — U0–U15

BA0,BA1 → U0–U15
A0–A12 → U0–U15
RAS → U0–U15
CAS → U0–U15
CKE0 → U0–U7
CKE1 → U8–U15
WE → U0–U15

SERIAL PD
SCL — A0 A1 A2 — SDA

NOTE: All resistor values are 22 ohms
unless otherwise specified.
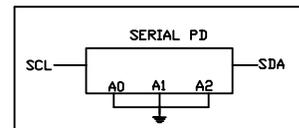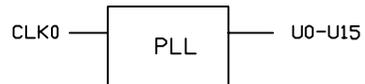
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to VSS	V_{IN}, Vout	-1.0 ~ 4.6	V
Voltage on VDD supply relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Storage Temperature	TSTG	-55 ~ +150	°C
Power Dissipation	PD	16	W
Short Circuit Current	IOS	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage Referenced to: V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input High Voltage	VIH	2.0	3.0	VDDQ+0.3	V	1
Input Low Voltage	VIL	-0.3	—	0.8	V	2
Output High Voltage	VOH	2.4	—	—	V	IOH= -2mA
Output Low Voltage	VOL	—	—	0.4	V	IOL= -2mA
Input Leakage Current	ILI	-10	—	10	µA	3

Note: 1. VIH (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. VIL (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE
(T_A = 23°C, f = 1MHz, V_{DD} = 3.3V, VREF=1.4V ± 200mV)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12)	CIN1	-	15	pF
Input Capacitance ($\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	CIN2	-	15	pF
Input Capacitance (CKE0)	CIN3	-	15	pF
Input Capacitance (CLK0)	CIN4	-	20	pF
Input Capacitance ($\overline{CS0}$)	CIN5	-	15	pF
Input Capacitance (DQM0-DQM7)	CIN6	-	15	pF
Input Capacitance (BA0-BA1)	CIN7	-	15	pF
Data input/output capacitance (DQ0-DQ63)	Cout	-	22	pF
Data input/output capacitance (CB0-7)	Cout 1	-	22	pF

White Electronic Designs Corp reserves the right to change products or specifications without notice.

OPERATING CURRENT CHARACTERISTICS

(V_{CC} = 3.3V, T_A = 0°C to +70°C)

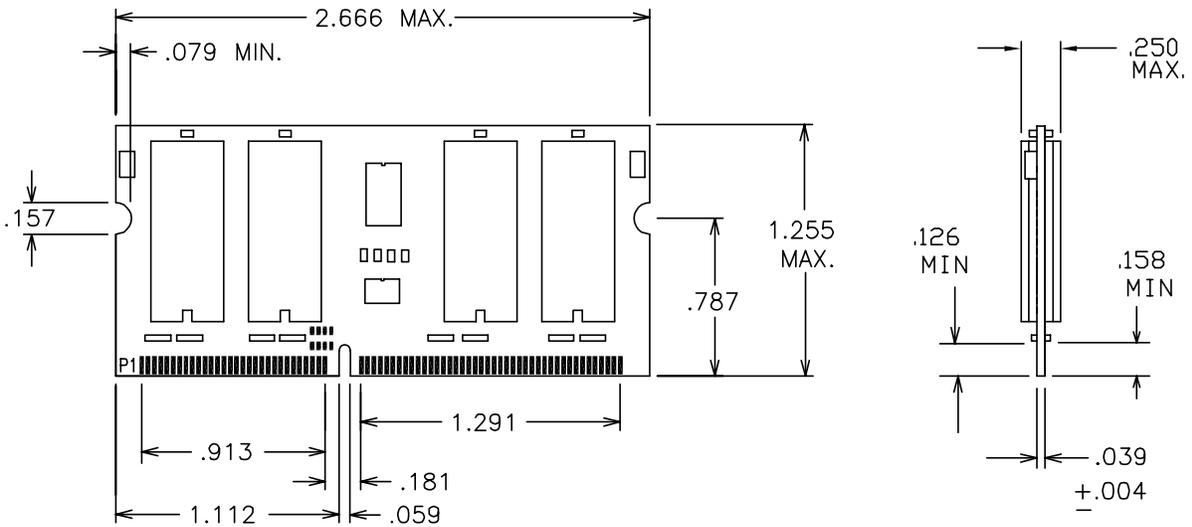| Parameter	Symbol	Conditions	Version 133	Version 100	Units	Note
Operating Current (One bank active)	ICC1	Burst Length = 1 tRC ≥ tRC(min) IOL = 0mA	960	880	mA	1
Precharge Standby Current in Power Down Mode	ICC2P	CKE ≤ VIL(max), tCC = 10ns	40		mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tCC = ∞	40			
Precharge Standby Current in Non-Power Down Mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are charged one time during 20	320		mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	160			
Active standby current in power-down mode	ICC3P	CKE ≥ VIL(max), tCC = 10ns	65		mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	65			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	400		mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ input signals are stable	280		mA	
Operating current (Burst mode)	ICC4	Io = mA Page burst 4 Banks activated tCCD = 2CLK	1,120	1,040	mA	1
Refresh current	ICC5	tRC ≥ tRC(min)	1,920	1,680	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	50	50	mA	

Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS (VIH/VIL = VDDQ/VssQ)

Part Number	Speed	Cas Latency
WED3DG6464V10D1	100MHz	CL=2
WED3DG6464V7D1	133MHz	CL=2
WED3DG6464V75D1	133MHz	CL=3

Note: For industrial temperature range product, add an "I" to the end of the part number.

PACKAGE DIMENSIONS

ALL DIMENSIONS ARE IN INCHES