mosaic

Mosaic Semiconductor Inc.

128K x 8 SRAM Module

PUMA 67S4000-85/10/12

Issue 1.0 : January 1993

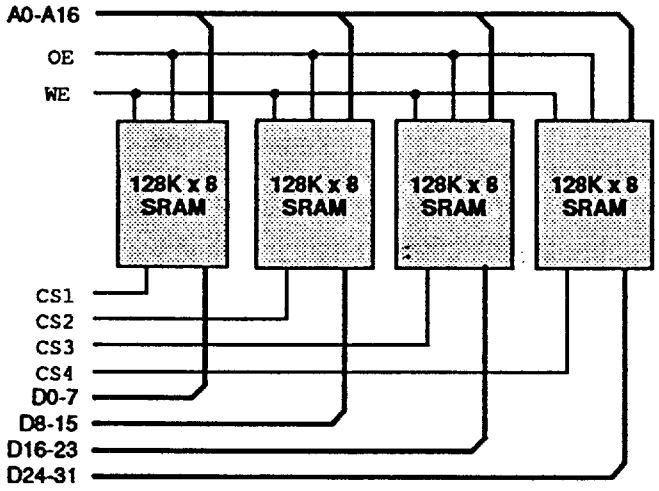
ADVANCE PRODUCT INFORMATION

4,194,304 bit CMOS High Speed Static RAM

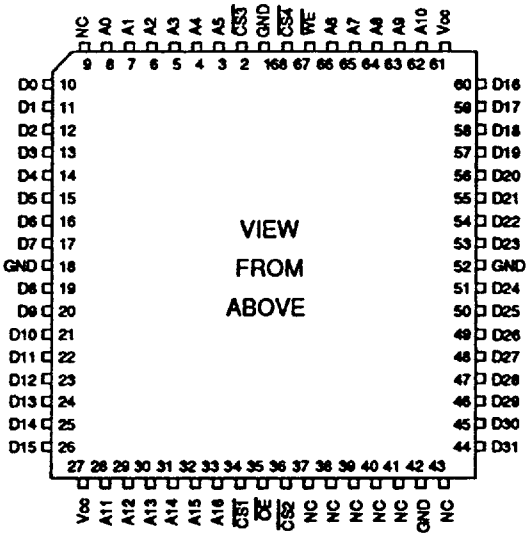
Features

Fast Access times of 85/100/120 ns.
JEDEC 68 J leaded Ceramic Surface Mount Package.
User Configurable as 8 / 16 / 32 bit wide.
Operating Power 90 / 180 / 300 mW (typ).
Low Power Standby 40 µW (typ) -L version.
3.0V Battery Back-up Capability
TTL Compatible Inputs and Outputs
Completely Static Operation
May be processed to non-compliant MIL-STD-883

Block Diagram



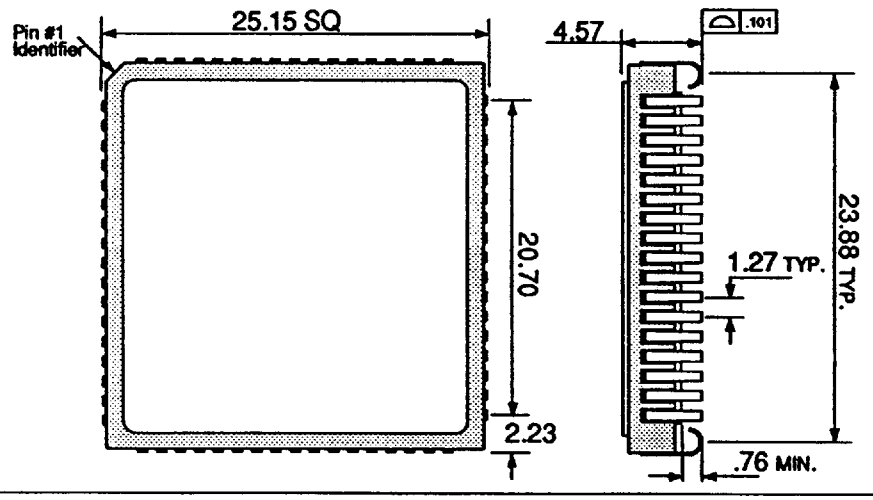
Pin Definition



Pin Functions

A0 - A16	Address Inputs
D0 - D31	Data Inputs/Outputs
$\overline{CS1-4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm.



Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{ss} (2)	V_T	-0.5V to +7	V
Power Dissipation	P_T	4	W
Storage Temperature	T_{STG}	-55 to +125	°C

Notes: (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the conditions above for extended periods may affect device reliability.
(2) Pulse width:- 3.0V for less than 30ns.

Recommended Operating Conditions

		min	*typ*	*max*	*Units*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	-0.3(1)	-	0.8	V	
Operating Temperature	T_A	0	-	70	°C	
	T_{AI}	-40	-	85	°C	(67S4000I)
	T_{AM}	-55	-	125	°C	(67S4000M,67S4000MB)

Note: (1) V_{IL} can be -3.0V pulse of less than 30ns.

DC Electrical Characteristics (V_{CC}=5V±10%,T_A=-55°C to +125°C)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*
Input Leakage Current		I_{LI}	V_{IN} = 0V to V_{CC}	-	-	2	µA
Output Leakage Current	32 bit	I_{LO}	$\overline{CS}$(2) = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	-	-	8	µA
Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}$(2) = V_{IL}, $I_{I/O}$ = 0mA, $V_{IL} \geq V_{IN} \geq V_{IH}$	-	60	180	mA
Average Supply Current	32 bit	I_{CC32}	$\overline{CS}$(2) = V_{IL}, Minimum cycle, $I_{I/O}$ = 0mA	-	180	320	mA
	16 bit	I_{CC16}	As above	-	90	160	mA
	8 bit	I_{CC8}	As above	-	45	80	mA
Standby Supply Current	TTL levels	I_{SB}	$\overline{CS}$(2) = V_{IH}	-	4	12	mA
	CMOS levels	I_{SB1}	$\overline{CS}$(2) ≥ V_{CC}-0.2V, 0.2V ≥ V_{IN} ≥ V_{CC}-0.2V	-	0.08	8	mA
	L-Part	I_{SB2}	$\overline{CS}$(2) ≥ V_{CC}-0.2V, 0.2V ≥ V_{IN} ≥ V_{CC}-0.2V	-	8	400	µA
Output Voltage Low		V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output Voltage High		V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V

Notes: (1) Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.
(2) $\overline{CS}$ above is accessed through $\overline{CS1}$-$\overline{4}$ These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

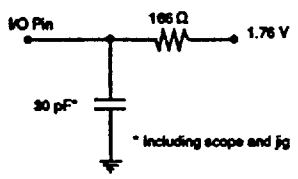
Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address, $\overline{OE}$, $\overline{WE}$	C_{IN1}	V_{IN}=0V	-	32	pF
	$\overline{CS1}$-4	C_{IN2}	V_{IN}=0V	-	8	pF
I/O Capacitance:	D0-D31	$C_{I/O}$	$V_{I/O}$=0V	-	32	pF

Note: This parameter is calculated and not measured.

AC Test Conditions

*PUMA module tested in 32bit mode.
*Input pulse levels: 0.0V to 3.0V
*Input rise and fall times: 5 ns
*Input and Output timing reference levels: 1.5V
*V_{CC}=5V±10%

Output Load



Operating Modes

The Table below shows the logic inputs required to control the operating modes of each of the SRAMs on the PUMA 67S4000

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	V_{CC} *Current*	*I/O Pin*	*Reference Cycle*
Not Selected	1	X	X	I_{SB},I_{SB1}	High Z	-
Read	0	0	1	I_{CC}	D_{OUT}	Read Cycle
Write	0	1	0	I_{CC}	D_{IN}	Write Cycle No.1
Write	0	0	0	I_{CC}	D_{IN}	Write Cycle No.2

$1 = V_{IH}$
$0 = V_{IL}$
$X = V_{IL}$ or V_{IH}

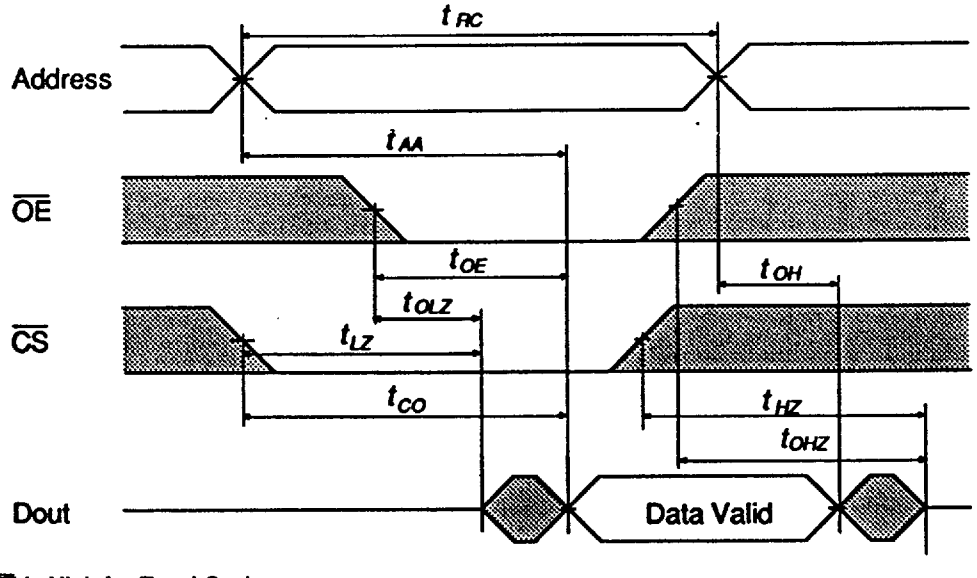
Note: $\overline{CS}$ is accessed through $\overline{CS1}$-$\overline{4}$. For correct operation, $\overline{CS1}$-$\overline{4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation.

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

		85		10		12			
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Units*	*Notes*
Read Cycle Time	t_{RC}	85	-	100	-	120	-	ns	
Address Access Time	t_{AA}	-	85	-	100	-	120	ns	
Chip Select Access Time	t_{CO}	-	85	-	100	-	120	ns	
Output Enable to Output Valid	t_{OE}	-	40	-	50	-	60	ns	
Output Hold from Address Change	t_{OH}	10	-	15	-	15	-	ns	
Chip Selection to Output in Low Z	t_{LZ}	10	-	10	-	10	-	ns	3
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns	3
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	35	0	45	ns	3
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	45	ns	3

Read Cycle Timing Waveform (1,2)

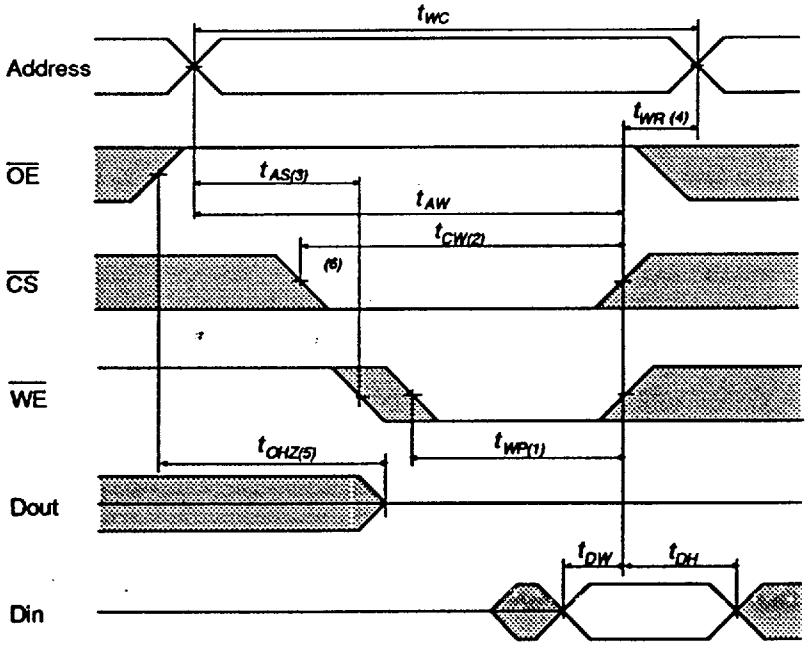


Notes (1) $\overline{WE}$ is High for Read Cycle.
(2) Address valid prior to or coincident with $\overline{CS}$ transition Low.
(3) t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are not tested but guaranteed by design.

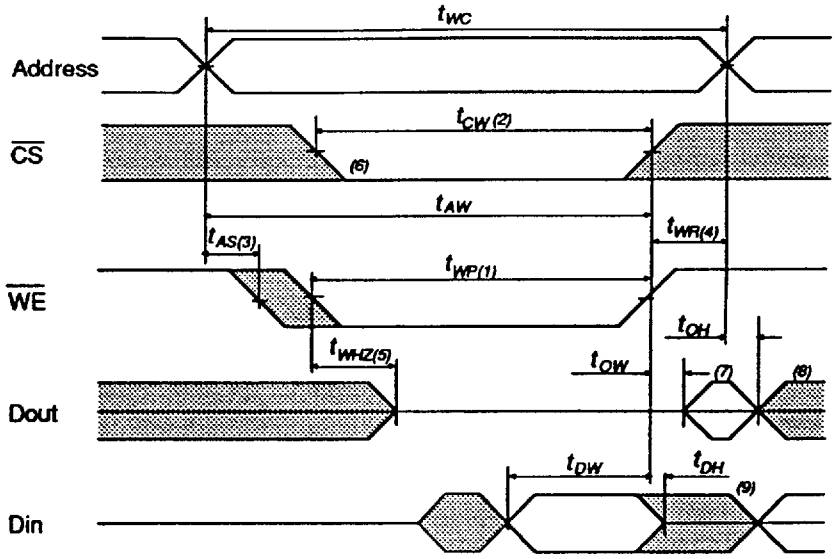
Write Cycle

Parameter	Symbol	85 min	85 max	10 min	10 max	12 min	12 max	Units	Notes
Write Cycle Time	t_{WC}	85	-	100	-	120	-	ns	
Chip Selection to End of Write	t_{CW}	75	-	90	-	100	-	ns	
Address Valid to End of Write	t_{AW}	75	-	90	-	100	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	65	-	75	-	90	-	ns	
Write Recovery Time	t_{WR}	5	-	5	-	10	-	ns	
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	ns	9
Data to Write Time Overlap	t_{DW}	35	-	40	-	50	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	10	-	10	-	10	-	ns	

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



AC Characteristics Notes

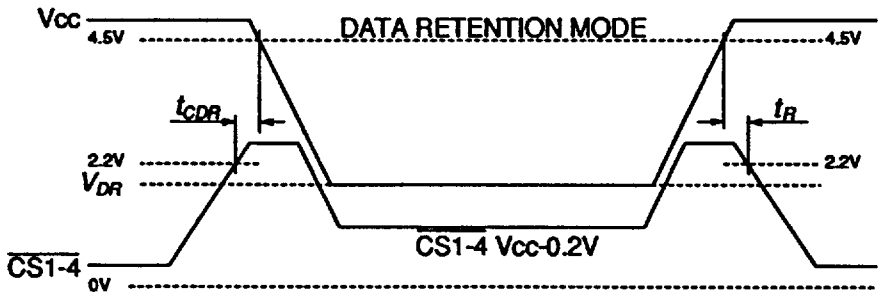
(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})
(6) Dout is in the same phase as written data of this write cycle.
(7) Dout is the read data of next address.
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
(9) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is not tested but guaranteed by design.

Low V_{CC} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ(2)*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS1\text{-}4} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS1\text{-}4}$ ≥2.8V, 0.2V≥V_{IN}≥2.8V	-	4	1200	µA
CS high to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes: (1) Typical figures are measured at 25°C.

Low V_{CC} Data Retention Timing Waveform



Ordering Information

PUMA 67S4000LMB-85

Speed	85	= 85 ns
	10	= 100 ns
	12	= 120 ns
Temperature range	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Processed to MIL-STD-883 Method 5004, non-compliant
Power Consumption	Blank	= Standard Power
	L	= Low Power
Memory Type	S4000	= 128Kx32 SRAM (Configurable as 256Kx16 and 512Kx8)
Package	PUMA 67	= 68 J Leaded Ceramic Module

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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