APPIAN TECHNOLOGY INC

DATA SHEET

ZyMOS

POACH/VGA-50™

POACH 51

T-52-33-45

FEATURES

* *single video chip for IBM PS/2 ™- and IBM PC/XT/AT/AT386/AT386SX ™- , MCA ™- compatible systems*
* *fully hardware-compatible with IBM VGA ™*
* *fully backward-compatible with IBM EGA ™, CGA ™ and MDA ™*
* *fully Hercules ™-compatible (analog mode)*
* *supports high-resolution 800 x 600 display with 256 colors from a 256K palette*
* *supports high-resolution 1024 x 768 interlaced display with 16 colors from a 256K palette*
* *supports high-resolution 800 x 600 display with 16 colors from a 256K palette*
* *supports 640 x 480 pixels with 256 colors out of a 256K palette*
* *supports 512 x 512 pixels with 256 colors out of a 256K palette*
* *supports auto-detect mode switching*
* *auto bus width sensing*
* *auto monitor detect*
* *50-MHz pixel clock*
* *supports 1-Mbit 256K x 4 and 256-Kbit 64K x 4 DRAMs*
* *supports additional 132 columns in text mode with 25, 30, 43 or 60 rows*
* *flicker-free display*
* *supports fast RAM BIOS*
* *8- or 16-bit bus*
* *low-power CMOS*
* *available in a 100-pin plastic flat package*

DESCRIPTION

POACH 51 is a one-chip implementation of the logic needed to support the new PS/2 VGA graphic standard. It is hardware-register-compatible with existing video modes, including CGA, EGA, MCGA, Hercules, and MDA. In addition, POACH/VGA-50 offers many advanced features such as eight or 16-bit bus support, 640 x 480 pixels with 256 colors, 1024 x 768 pixels in 16 colors, and support of 1-Mbit page mode DRAMs. POACH/VGA-50 offers OEM system and add-in board makers a cost-effective and high-performance video solution for MS/DOS- and OS/2-compatible PC/XT/AT/AT386/AT386SX systems.

AUGUST 1989

DESCRIPTION *(cont.)*

POACH 51 contains five components of the graphics sub-system: the CRT, Graphics, and Attribute Controllers, the Timing Sequencer and Miscellaneous Logic. Only six additional TTL parts plus RAMDAC and MEMORY are required for a 16-bit PC AT.

To ease applications development, software drivers are provided for all enhanced text and graphics modes. And, to ease hardware design to market, schematics and board layout kits are also be available for both 8- and 16-bit boards.

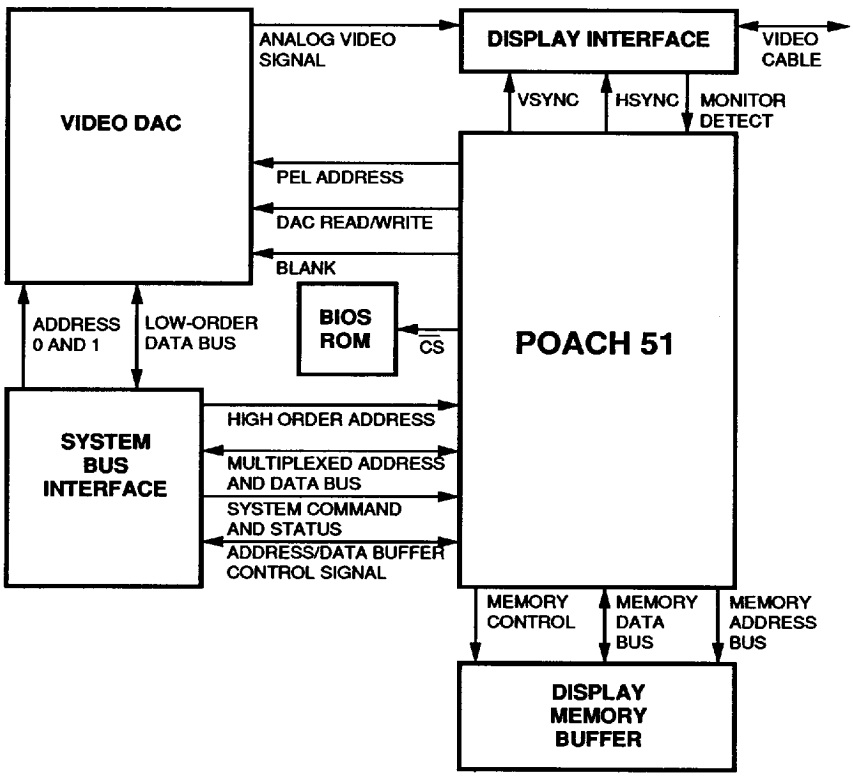


Figure 1. POACH/VGA-50 System Block Diagram

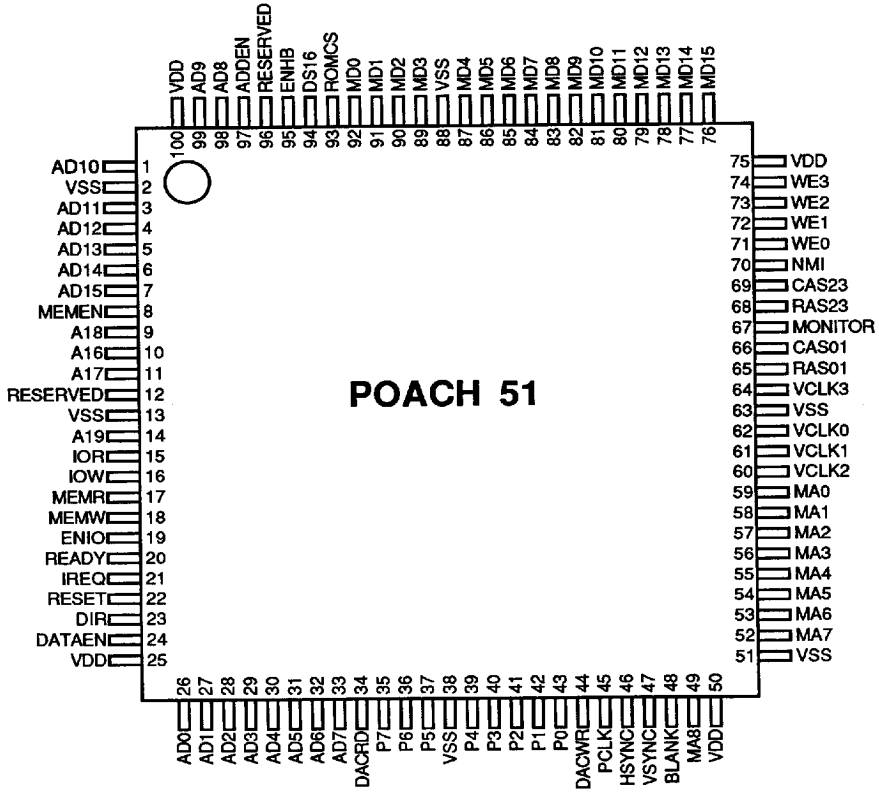


Figure 2. POACH 51 Plastic Flat Package Pin Diagram

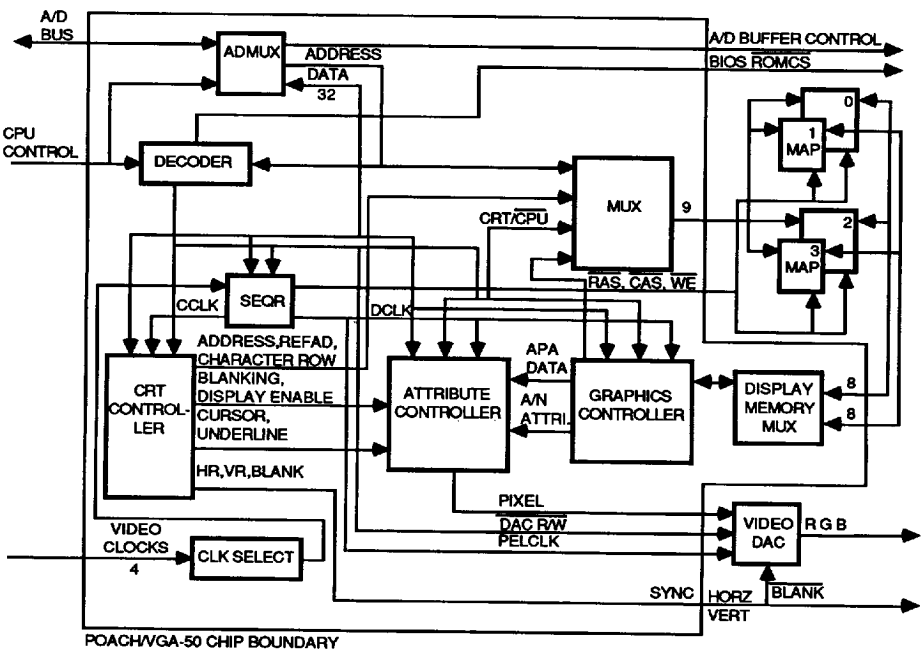


Figure 3. POACH 51 IC Block Diagram

GRAPHICS MODES

DOS MODES	RESOLUTION	VIDEO BOARD	COLORS
4,5	320x200	VGA, EGA, CGA, MCGA	4 out of 256K
6	640x200	VGA, EGA, CGA, MCGA	2 out of 256K
D	320x200	VGA, EGA	16 out of 256K
E	640x200	VGA, EGA	16 out of 256K
F	640x350	VGA, EGA	Monochrome
10	640x350	VGA, EGA	16 out of 256K
11	640x480	VGA, MCGA	2 out of 256K
12	640x480	VGA	16 out of 256K
13	320x200	VGA, MCGA	256 out of 256K
14	360x480	VGA	256 out of 256K

TEXT MODES

DOS MODE	RES.	CHAR. BOX	COL.	ROWS	BOARD	COLORS
0,1	320x200	8x8	40	25	CGA	16 out of 256K
	320x350	8x14	40	25	EGA	16 out of 256K
	320x400	8x16	40	25	MCGA	16 out of 256K
	360x400	9x16	40	25	VGA	16 out of 256K
2,3	640x200	8x8	80	25	CGA	16 out of 256K
	640x350	8x14	80	25	EGA	16 out of 256K
	640x400	8x16	80	25	MCGA	16 out of 256K
	720x400	9x16	80	25	VGA	16 out of 256K
7	720x350	9x14	80	25	MDA	Monochrome
	720x350	9x14	80	25	EGA	Monochrome
	720x400	9x16	80	25	VGA	Monochrome

ENHANCED GRAPHICS MODES

MODES	RES.	CHAR. BOX	COL.	ROWS	COLORS (OUT OF 256K)
51 (text)	720x602	9x14	80	43	16
52 (text)	720x480	9x8	80	60	16
53 (text)	1056x400	8x16	132	25	16
54 (text)	800x400	8x16	100	25	16
55 (text)	800x480	8x8	100	60	16
56 (text)	1056x480	8x8	132	60	16
59 (text)	1056x344	8x8	132	43	16
5A (text)	1188x480	9x8	132	60	16
5B (graphic)	800x600	8x8	100	75	16
5C (graphic)	640x400	8x16	80	25	256
5D (graphic)	640x480	8x16	80	30	256
5E (graphic)	800x600	8x16	100	75	256
5F (graphic)	1024x768	8x16	128	48	16
60 (graphic)	960x720	8x16	120	45	16
61 (graphic)	1280x640	8x16	160	40	16
62 (graphic)	512x512	8x16	64	32	256
63 (graphic)	720x540	8x16	90	30	16
64 (graphic)	720x540	8x16	90	30	256
Hercules™	720x348	9x12	80	25	monochrome

POACH 51 Pin Description

T-52-33-45

Pin No.[1]	Symbol	Type	Description
10	A16	Input	Address bus, bit 16
11	A17	Input	Address bus, bit 17
9	A18	Input	Address bus, bit 18
14	A19	Input	Address bus, bit 19
26	AD0	Input/Output	Multiplexed address and data, bit 0
27	AD1	Input/Output	Multiplexed address and data, bit 1
28	AD2	Input/Output	Multiplexed address and data, bit 2
29	AD3	Input/Output	Multiplexed address and data, bit 3
30	AD4	Input/Output	Multiplexed address and data, bit 4
31	AD5	Input/Output	Multiplexed address and data, bit 5
32	AD6	Input/Output	Multiplexed address and data, bit 6
33	AD7	Input/Output	Multiplexed address and data, bit 7
98	AD8	Input/Output	Multiplexed address and data, bit 8
99	AD9	Input/Output	Multiplexed address and data, bit 9
1	AD10	Input/Output	Multiplexed address and data, bit 10
3	AD11	Input/Output	Multiplexed address and data, bit 11
4	AD12	Input/Output	Multiplexed address and data, bit 12
5	AD13	Input/Output	Multiplexed address and data, bit 13
6	AD14	Input/Output	Multiplexed address and data, bit 14
7	AD15	Input/Output	Multiplexed address and data, bit 15
97	ADDEN	Output	Address buffer enable (active low)
48	BLANK	Output	BLANK output (active-low)
66	CAS01	Output	Column address strobe of MAP 0 and MAP 1 (active low)
69	CAS23	Output	Column address strobe of MAP 2 and MAP 3 (active low)
34	DACRD	Output	DAC read strobe (active low)

POACH 51 Pin Description *(cont.)*

T-52-33-45

Pin No.	Symbol	Type	Description
44	DACWR	Output	DAC write strobe (active low)
24	DATAEN	Output	Data buffer enable (active low)
23	DIR	Output	Data buffer direction control for READ cycle (active high for write to memory I/O)
94	DS16[2]	Output	Enable 16-bit transfer (active low) open drain
19	ENIO	Input	Enable I/O (active low)
95	ENHB[2]	Input	Bus high-byte enable (active low)
46	HSYNC	Output	Horizontal synchronization pulse-programmable polarity
15	IOR	Input	I/O read strobe (active low)
16	IOW	Input	I/O write strobe (active low)
21	IREQ	Output	Interrupt request (programmable polarity)
59	MA0	Output	Multiplexed address bus of display memory
58	MA1	Output	Multiplexed address bus of display memory
57	MA2	Output	Multiplexed address bus of display memory
56	MA3	Output	Multiplexed address bus of display memory
55	MA4	Output	Multiplexed address bus of display memory
54	MA5	Output	Multiplexed address bus of display memory
53	MA6	Output	Multiplexed address bus of display memory
52	MA7	Output	Multiplexed address bus of display memory
49	MA8	Output	Multiplexed address bus of display memory
92	MD0	Input/Output	Multiplexed display memory data bus of MAP 1 and MAP 3
91	MD1	Input/Output	Multiplexed display memory data bus of MAP 1 and MAP 3
90	MD2	Input/Output	Multiplexed display memory data bus of MAP 1 and MAP 3
89	MD3	Input/Output	Multiplexed display memory data bus of MAP 1 and MAP 3

POACH 51 Pin Description *(cont.)*

T-52-33-45

Pin No.	Symbol	Type	Description
87	MD4	Input/Output	Multiplexed display memory data bus of MAP 1 and MAP 3
86	MD5	Input/Output	Multiplexed display memory data bus of MAP 1 and MAP 3
85	MD6	Input/Output	Multiplexed display memory data bus of MAP 1 and MAP 3
84	MD7	Input/Output	Multiplexed display memory data bus of MAP 1 and MAP 3
83	MD8	Input/Output	Multiplexed display memory data bus of MAP 0 and MAP 2, or chip configuration byte during power-up
82	MD9	Input/Output	Multiplexed display memory data bus of MAP 0 and MAP 2, or chip configuration byte during power-up
81	MD10	Input/Output	Multiplexed display memory data bus of MAP 0 and MAP 2, or chip configuration byte during power-up
80	MD11	Input/Output	Multiplexed display memory data bus of MAP 0 and MAP 2, or chip configuration byte during power-up
79	MD12	Input/Output	Multiplexed display memory data bus of MAP 0 and MAP 2, or chip configuration byte during power-up
78	MD13	Input/Output	Multiplexed display memory data bus of MAP 0 and MAP 2, or chip configuration byte during power-up
77	MD14	Input/Output	Multiplexed display memory data bus of MAP 0 and MAP 2, or chip configuration byte during power-up
76	MD15	Input/Output	Multiplexed display memory data bus of MAP 0 and MAP 2, or chip configuration byte during power-up
8	MEMEN	Input	Enable display memory (active high)
17	MEMR	Input	Memory read strobe (active low)
18	MEMW	Input	Memory write strobe (active low)
67	MONITOR	Input	Monitor-type detector
70	NMI	Output	Non-maskable interrupt (active high)

POACH 51 Pin Description *(cont.)*

T-52-33-45

Pin No.	Symbol	Type	Description
43	P0	Output	Video DAC pixel address, bit 0
42	P1	Output	Video DAC pixel address, bit 1
41	P2	Output	Video DAC pixel address, bit 2
40	P3	Output	Video DAC pixel address, bit 3
39	P4	Output	Video DAC pixel address, bit 4
37	P5	Output	Video DAC pixel address, bit 5
36	P6	Output	Video DAC pixel address, bit 6
35	P7	Output	Video DAC pixel address, bit 7
45	PCLK	Output	Pixel clock output
65	RAS01	Output	Row address strobe of MAP 0 and MAP 1 (active low)
68	RAS23	Output	Row address strobe of MAP 2 and MAP 3 (active low)
20	READY (RDY)	Output	I/O channel ready open drain output (active low)
96	RESERVED	Output	NC
12	RESERVED	Input	Pull up required
22	RESET	Input	System reset (active high)
93	ROMCS	Output	BIOS EPROM chip select (active low)
25	V_{DD}	-	+5V DC
50	V_{DD}	-	+5V DC
75	V_{DD}	-	+5V DC
100	V_{DD}	-	+5V DC
62	VCLK0	Input	Video clock input
61	VCLK1	Input	Video clock input
60	VCLK2	Input	Video clock input
64	VCLK3	Input	Video clock input
13	V_{SS}	-	Ground

T-52-33-45

POACH 51 Pin Description *(cont.)*

Pin No.	Symbol	Type	Description
38	V_{SS}	-	Ground
51	V_{SS}	-	Ground
63	V_{SS}	-	Ground
88	V_{SS}	-	Ground
2	V_{SS}	-	Ground
47	VSYNC	Output	Vertical synchronization pulse
71	WE0	Output	WE enable of MAP 0 (active low)
72	WE1	Output	WE enable of MAP 1 (active low)
73	WE2	Output	WE enable of MAP 2 (active low)
74	WE3	Output	WE enable of MAP 3 (active low)

NOTES:

1. Supports 16-bit bus architecture.

T-52-33-45

Absolute Maximum Ratings (V_{SS} = 0 V)

Symbol	Parameter	Value MIN	Value MAX	Units
I_{IN}	input current	-10	10	uA
I_{OUT}	output current	-10	10	mA
PD	power dissipation		1	W
T_A	ambient temperature under bias	0°	70°	C
T_{STG}	storage temperature	-65°	150°	C
V_{DD}	power supply voltage	V_{SS} -0.5	6.0	V
V_{IN}	input voltage	V_{SS} -0.5	V_{DD} +0.5	V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

POACH 51 DC Characterisitics (V_{CC} = 5V +/- 5%, T_A = 0 to 70°C)

Recommended Operating Conditions (V_{SS} = 0 V)

Symbol	Parameter	Condition	Value MIN	Value MAX	Units
V_{IN}	input voltage		V_{SS}	V_{DD}	V
T_{OPR}	operating temperature		0°	70°	C
V_{DD}	power supply voltage		4.75	5.25	V

Electrical Characteristics (V_{SS} = 0 V)

Symbol	Parameter	Condition	Value MIN	Value MAX	Units	Notes
I_{CC}	power supply current	f_{MAX} = 50 MHz		150	mA	no DC loads
I_{DDS}	standby current	V_{DD} = MAX		10	uA	
I_I	input leakage		-1	+1	uA	
I_{IH}	input high current	$V_{IN} = V_{CC}$		10	uA	
I_{IL1}	input low current	V_{IN} = 0V	-100		uA	pull-up
I_{IL2}	special input low current	V_{IN} = 0V		-10	uA	no pull-up
V_{IH}	input voltage high	V_{DD} = 5.25	2.0		V	
V_{IL}	input voltage low			0.8	V	
V_{OH}	output voltage high	I_{OH} = 2,4,8 mA	2.4		V	
V_{OL}	output voltage low	I_{OL} = 4,6,8 mA V_{DD} = 4.75		V_{SS} +0.4	V	
V_{SK}	input voltage skew			2	V/ns	

POACH 51 AC Characteristics (V_{cc} = 5V +/- 5%, T_A = 0 to 70°C)

AC timings are referenced to 1.5V

T-52-33-45

Symbol	Parameter	Value MIN	TYP	MAX	Units	Notes
1	Address setup time to -CMD	15	-	-	ns	7
2	-CMD pulse width	-	180	-	ns	7
3	Read data valid from -CMD	-	-	135	ns	7
4	Write data setup time from READY	-	120	-	ns	7
5	Read data hold time	-	0	-	ns	7
6	Write data hold time	5	-	-	ns	7
7	-ADDEN hold time to -CMD active	9	15	20	ns	
8	-DATAEN active from -CMD	10	15	23	ns	
9	-DS16 active from address valid	10	17	24	ns	8
10	BDIR valid from Read CMD active	8	13	19	ns	
11	READY active from -CMD active	12	18	30	ns	
12	-ADDEN active from -CMD inactive	10	16	20	ns	
13	-DATAEN hold time from -CMD	10	16	22	ns	
14	-DS16 hold time from address invalid	8	17	24	ns	
15	BDIR hold time to -CMD inactive	10	14	20	ns	
16	Address AD0~15 setup to -CMD active	5	-	-	ns	1
17	Address AD0~15 hold to -CMD active	5	-	-	ns	
*18	ENHB, A16~19 setup to -CMD active	5	-	-	ns	
19	Address AD0~15 hold from -ADDEN	5	-	-	ns	
20	Read Data (AD0~15) delay from -CMD	35	-	-	ns	2b
21	Read Data (AD0~15) hold from -CMD	-	-	0	ns	2b
22	Write Data (AD0~15) setup from -CMD	15	-	-	ns	2a
23	Write Data (AD0~15) hold from -CMD	2	-	-	ns	2a
24	-DACWR delay from -IOW/write cmd active	10	14	40	ns	
25	-DACWR delay from -IOW/write cmd active	10	16	22	ns	
26	-DACRD delay from -IOR/read cmd active	11	14	20	ns	
27	-DACRD delay from -IOR/read cmd active	10	16	22	ns	
28	P0~P7 pixel word setup to PCLK	3	-	-	ns	6
29	P0~P7 pixel word hold from PCLK	t6+t62-4	-	-	ns	6
30	Blank setup to PCLK	1	-	-	ns	
31	Blank hold from PCLK	3	-	-	ns	
32	Sync setup to PCLK	6	-	-	ns	
33	Sync hold from PCLK	10	-	-	ns	
*34	Reset pulse width	128tc	-	-	ns	
35	MEMEN setup to -MEMR	10	-	-	ns	
36	MEMEN hold from -MEMR inactive	10	-	-	ns	
37	-ENIO setup to -IOCMD	15	-	-	ns	
38	-ENIO hold from -IOCMD inactive	10	-	-	ns	
*39	MONITOR setup to -IOR/read command	50	-	-	ns	
*40	MONITOR hold to -IOR/read cmd active	10	-	-	ns	
*41	Video vertical blank period					4
*42	Active vertical video period					4
*43	Video display end to VSYNC					4
*44	VSYNC internval					4
*45	Video Sync pulse width					4
46	IREQ active from VSYNC	10	-	25	ns	
*47	IREQ inactive from -IOW/write command	30	-	40	ns	
*48	NMI active from -IOW/write command	-	14	20	ns	
*49	NMI inactive from -IOW/write command	-	16	22	ns	

T-52-33-45

POACH 51 AC Characterisitics *(cont.)*

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
50	-ROMCS active from -MEMR	10	-	19	ns	
*51	Video horizontal blank period					5
*52	Active horizontal video period					5
*53	Horizontal display end to HSYNC					5
*54	HSYNC end to active video period					5
*55	-HSYNC interval					5
*56	HSYNC period					5
*57	+HSYNC interval					5
58	PCLK slew from VCLK	4	-	20	ns	
59	-DS16 from IOW	6	17	22	ns	9
60	-ROMCS from address valid	12	22	30	ns	
*61	PCLK high time	tch-4	-	-	ns	
*62	PCLK low time	tcl-1	-	-	ns	
*63	-CMD active period	3tc	-	-	ns	3
*64	READY pulse width	4tc	-	128tc	ns	
*65	Read data setup to READY	25	-	-	ns	
*66	Read data delay time	-	-	3tc+30	ns	
fc	VCLK 0-3 input clock frequency			50	MHz	
tc	VCLK 0-3 input clock period	20			ns	
tch	VCLK 0-3 high time		tc/2+/-5%		ns	
tcl	VCLK 0-3 low time		tc/2+/-5%		ns	

Notes:

1. Address A0~A15 must be valid 10 ns before -CMD goes active.
2a. -WRCMD can be either -IOW or valid S0, S1, MIO lines indicating -IOW.
2b. -RDCMD can be either -IOW or valid S0, S1, MIO lines indicating -IOR.
3. The -CMD pulse width indicated is a recommended minimum, the VGA controller may work with a lesser pulse period.
4. See VSYNC timings below.
5. See HSYNC timings below.
6. PCLK can be inverted externally to improve t_{28} and t_{29} timings. t_{28} (improved) = t_{28} + t_{81} - t_{delay} (inverter); t_{29} (improved) = t_{82} - t_{delay} (inverter) - t_{29}.
7. These timing numbers are meant only as a general reference; timing numbers t_1 to t_8 may vary depending upon system implementations. Do not use these numbers to design systems aound the POACH 51 VGA.
8. -DS16 is active only during CPU memory cycles and is inactive during CPU I/O cycles.
9. -DS16 active time when I/O register is written to enable -DS16.

*: Timing numbers guaranteed by design, not tested.

VSYNC	350 lines	400 lines	480 lines	600 lines
t_{41}	2.768 mS	1.112 mS	0.922 mS	0.72 mS
t_{42}	11.504 mS	13.156 mS	15.762 mS	17.07 mS
t_{43}	0.985 mS	0.159 mS	0.064 mS	0.030 mS
t_{44}	14.258 mS	14.258 mS	15.583 mS	17.78 mS
t_{45}	0.064 mS	0.064 mS	0.064 mS	0.06 mS

HSYNC	40/80 no border	80 with border	800-pixel graphics
t_{51}	6.356 uS	5.720 uS	6.23 uS
t_{52}	24.422 uS	26.058 uS	22.22 uS
t_{53}	0.636 uS	0.318 uS	0.67 uS
t_{54}	1.907 uS	1.589 uS	3.56 uS
t_{55}	3.813 uS	3.813 uS	2.00 uS
t_{56}	31.778 uS	31.778 uS	28.44 uS
t_{57}	3.813 uS	3.813 uS	2.00 uS

POACH 51 Timing Waveforms

T-52-33-45

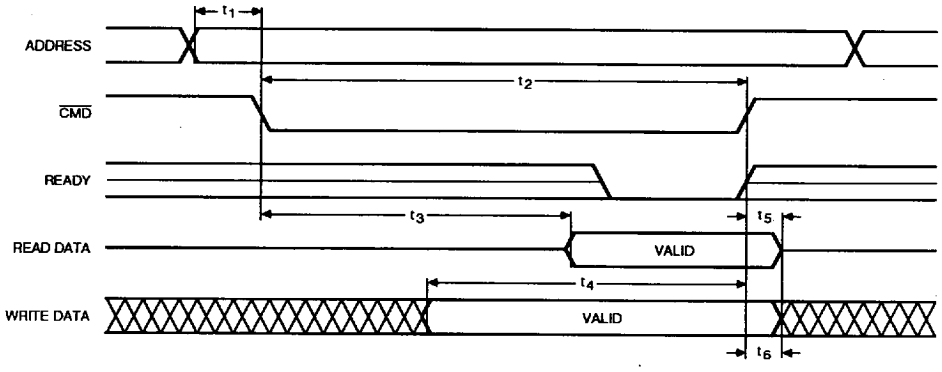


Diagram 1. PC XT/AT Bus Cycle Timing

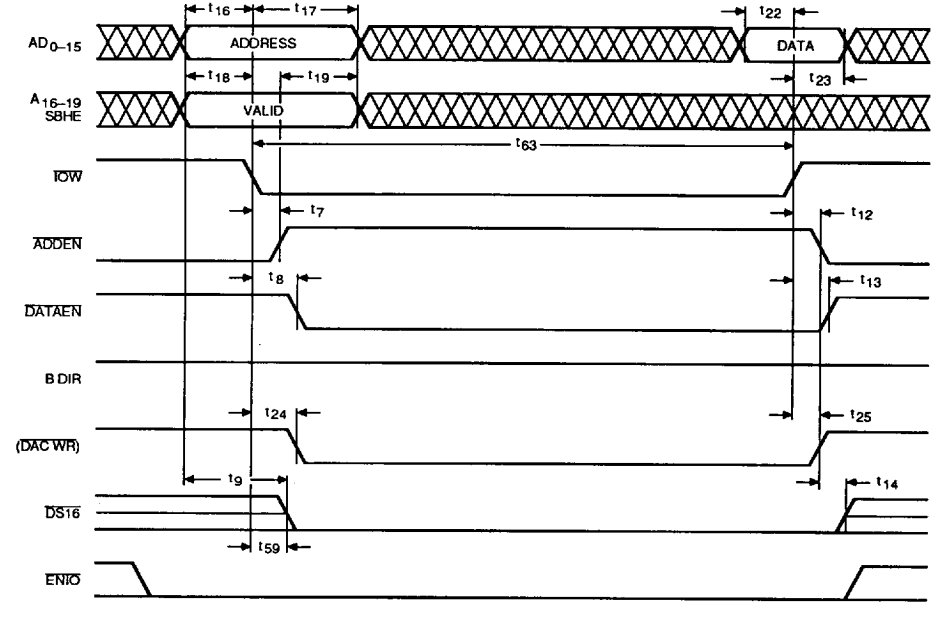


Diagram 2. AT Mode I/O Write Timing

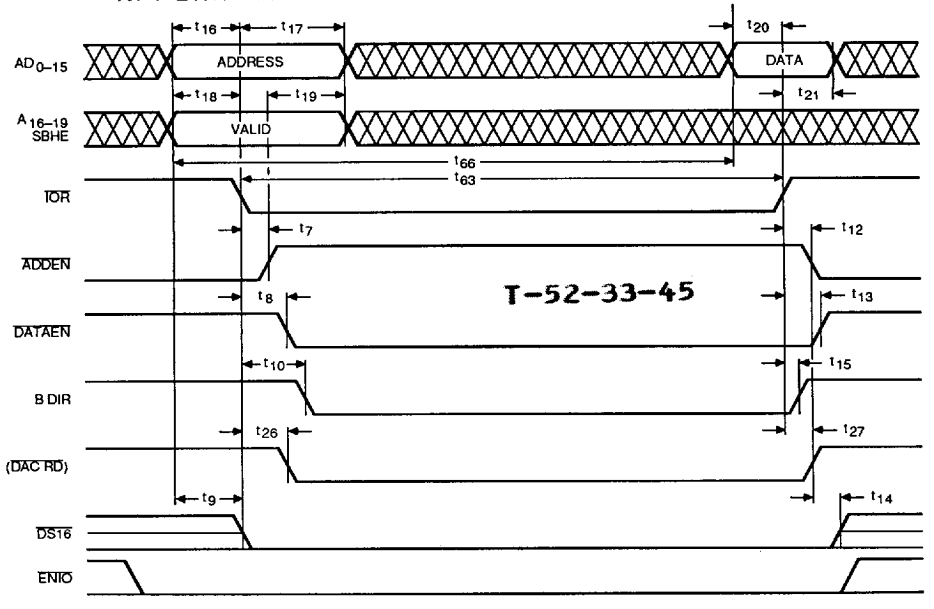


Diagram 3. AT Mode I/O Read Timing

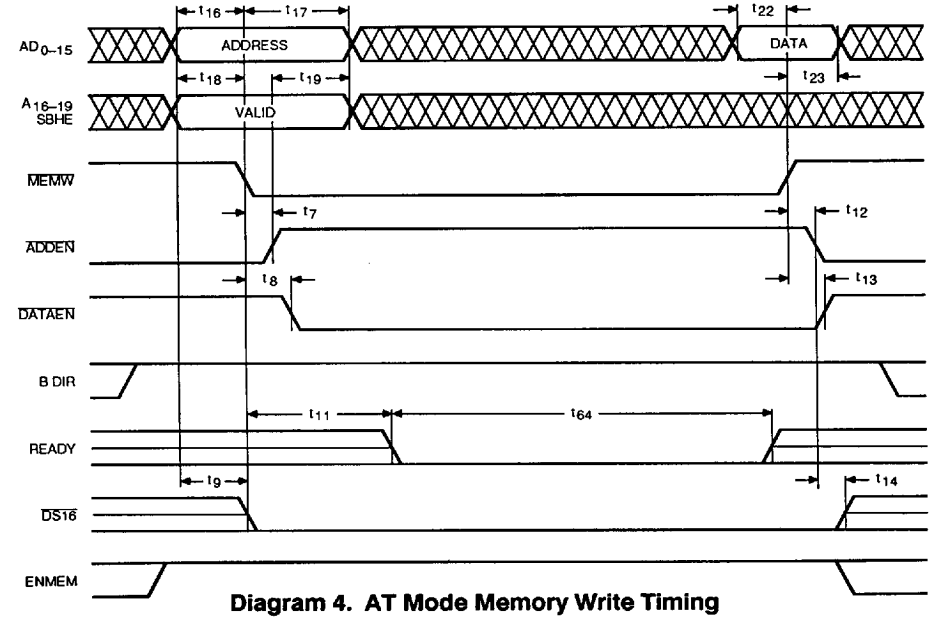


Diagram 4. AT Mode Memory Write Timing

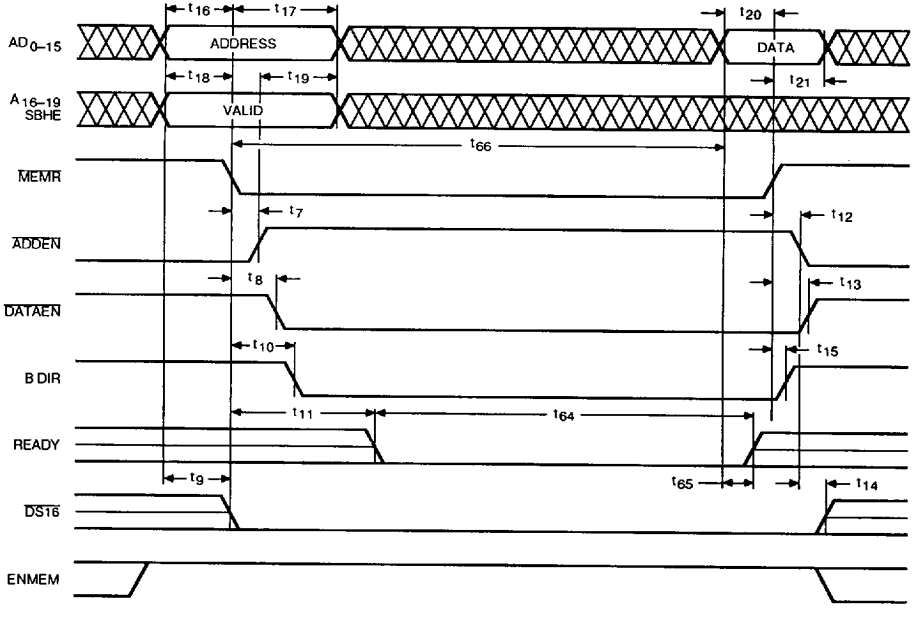


Diagram 5. AT Mode Memory Read Timing

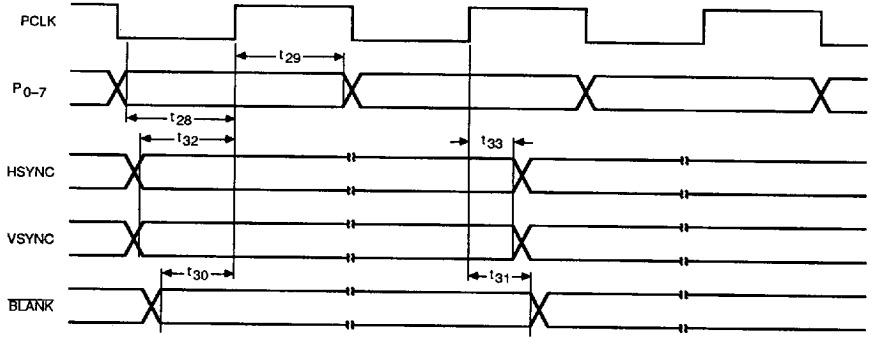


Diagram 6. DAC Interface Timings

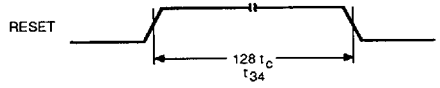


Diagram 7. Reset Timing

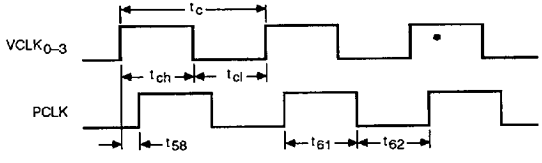


Diagram 8. Clock/PCLK Timing

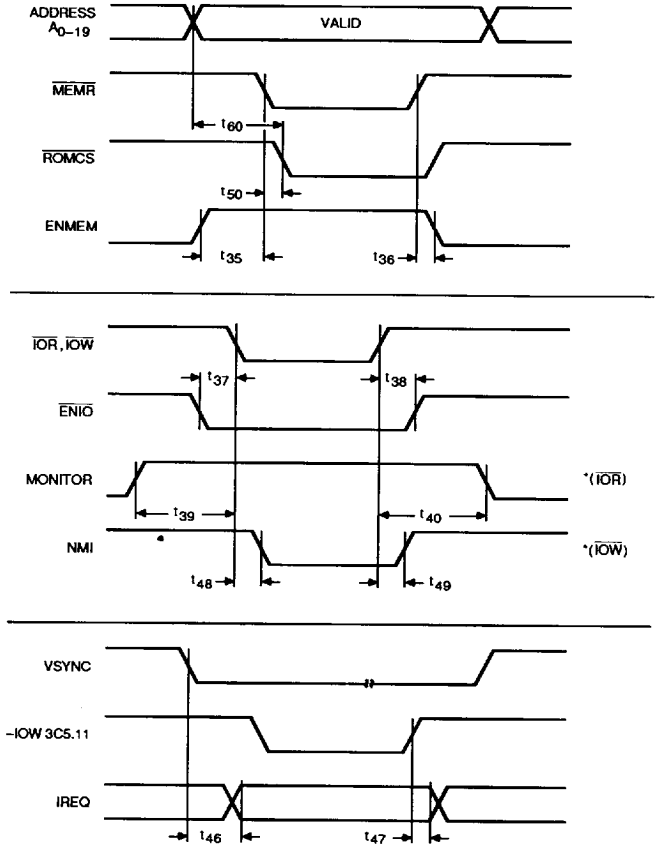
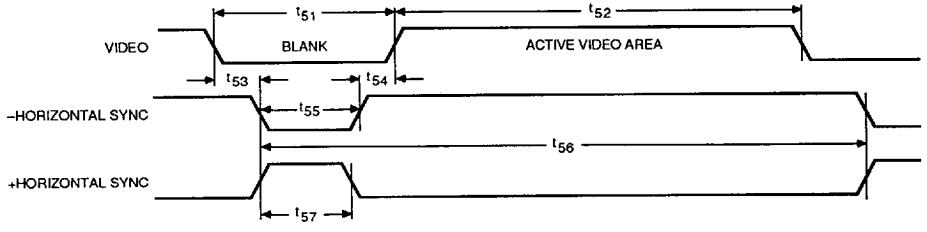
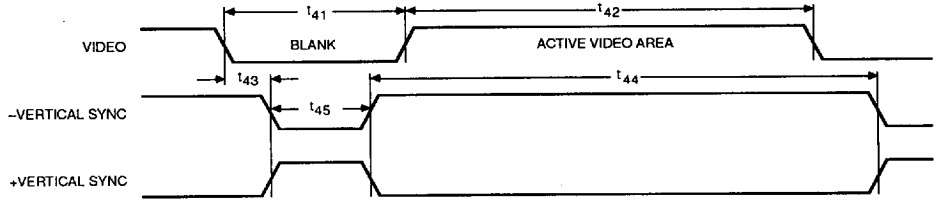


Diagram 9. Miscellaneous Interface Timings



Horizontal Timing



Vertical Timing

Diagram 10. Horizontal and Vertical Timing

ZyVGA DRAM Timing

T-52-33-45

Symbol	Parameter	8-dot mode MIN		9-dot mode MIN	
t_{rc}	Read/Write cycle time	6tc	-	7tc	-
t_{ras}	RAS pulse width	3.5tc-2tt	-	4tc-2tt	-
*t_{ar}	Column address hold from RAS	2tc	-	2tc	-
t_{rp}	RAS precharge	2.5tc	-	3.5tc	-
t_{crp}	CAS-to-RAS precharge	2.5tc	-	3.5tc	-
t_{csh}	CAS hold from RAS	3.5tc	-	3.5tc	-
t_{rcd}	RAS-to-CAS delay	1.5tc	-	1.5tc	-
t_{rsh}	RAS hold from CAS	2tc-2tt	-	2tc-2tt	-
t_{cpn}	CAS precharge	4tc-tt	-	5tc-tt	-
t_{cas}	CAS pulse width	2tc-2tt	-	2tc-2tt	-
t_{asr}	Row address setup to RAS	0.5tc	-	0.5tc	-
t_{asc}	Column address setup to CAS	0.5tc	-	0.5tc	-
t_{rs}	Row address hold from RAS	0.5tc	-	0.5tc	-
t_{cs}	Column address hold from CAS	0.5tc	-	0.5tc	-
t_{dsc}	Read data setup to CAS inactive	7ns	-	7ns	-
t_{off}	Read data hold to CAS inactive	0ns	-	0ns	
t_{wp}	WE pulse width	2.5tc	-	2.5tc	-
t_{ds}	Write data setup to CAS	tc-10	-	tc-10	-
t_{dh}	Write data hold from CAS	1.5tc	-	1.5tc	-
t_{dhr}	Write data hold from RAS	3tc	-	3tc	-
t_{wcr}	WE hold from RAS	3.5tc	-	1tc	-
t_{wcs}	Write command setup time	0.5tc-tt	-	0.5tc-tt	-
t_{wch}	Write command setup time	2tc	-	2tc	-

Notes:

t_c = 1/input clock frequency

All DRAM timings are listed at a maximum clock rate of 20 MHz during production.

*: Timing numbers guaranteed by design, not tested.

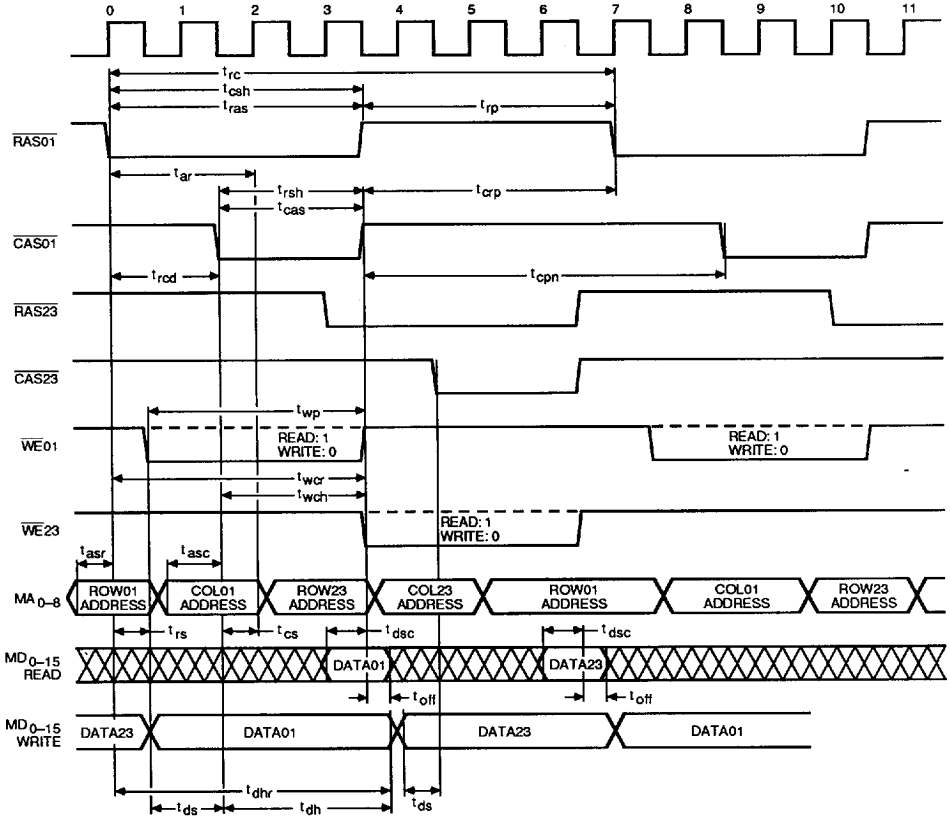


Diagram 11. Nine-dot DRAM Cycle Timing

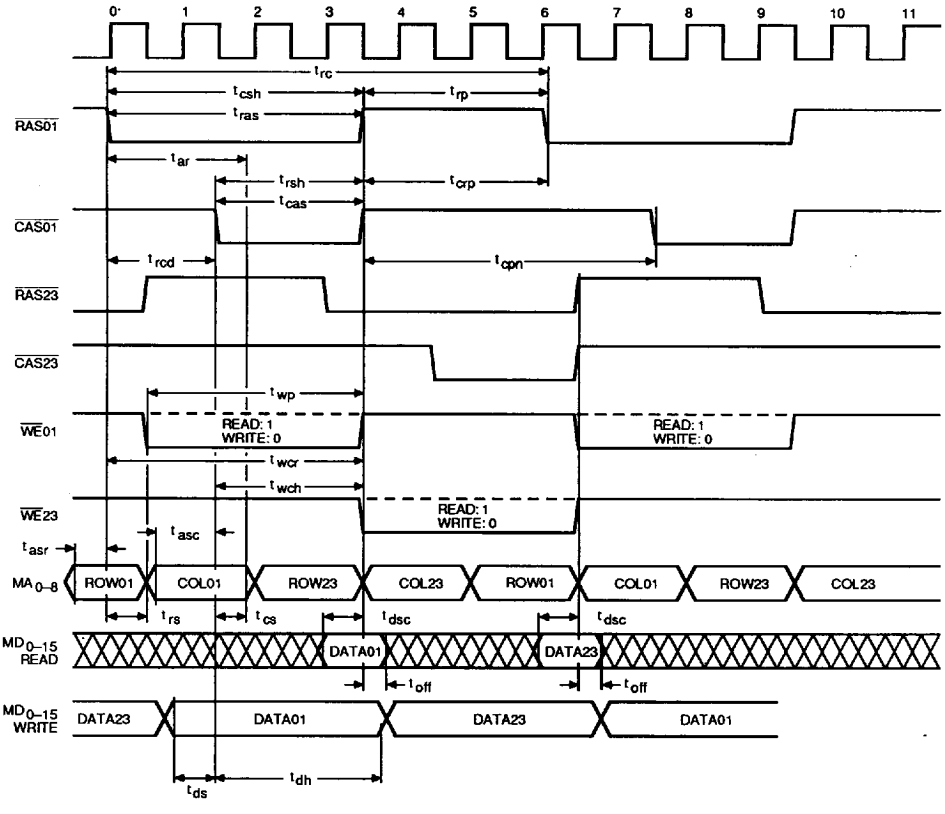


Diagram 12. Eight-dot DRAM Cycle Timing

T-52-33-45

ZyVGA DRAM Timing *(high bandwidth mode)*

Symbol	Parameter	Value MIN	MAX	Units	Notes
t_{rc}	Read/Write cycle time	6tc	19tc	ns	1
t_{ras}	RAS pulse width	17tc-2tt	-	ns	
*t_{ar}	Column address hold from RAS	2tc	-	ns	2
t_{rp}	RAS precharge	2.5tc	-	ns	2
t_{crp}	CAS-to-RAS precharge	2.5tc	-	ns	2
t_{csh}	CAS hold from RAS	3.5tc	-	ns	2
t_{rcd}	RAS-to-CAS delay	1.5tc	-	ns	
t_{rsh}	RAS hold from CAS	2tc-2tt	-	ns	2
t_{cpn}	CAS precharge	2tc-2tt	-	ns	2
t_{cas}	CAS pulse width	2tc-2tt	-	ns	
t_{asr}	Row address setup to RAS	0.5tc-tt	-	ns	2
t_{asc}	Column address setup to CAS	tc-tt	-	ns	
t_{rs}	Row address hold from RAS	0.5tc-tt	-	ns	2
t_{cs}	Column address hold from CAS	0.5tc-tt	-	ns	*
t_{dsc}	Read data setup to CAS inactive	7ns	-	ns	3
t_{off}	Read data hold to CAS inactive	0ns	-	ns	3
t_{wp}	WE pulse width	2.5tc	-	ns	4
t_{ds}	Write data setup to CAS	tc-10	-	ns	4
t_{dh}	Write data hold from CAS	1.5tc	-	ns	4
t_{dhr}	Write data hold from RAS	3tc	-	ns	4
t_{wcs}	Write command setup time to CAS	0.5tc-tt	-	ns	4
t_{wch}	Write command hold time from CAS	2tc	-	ns	4
t_{wcr}	WE hold from RAS	3.5tc	-	ns	4

ZyVGA DRAM Timing *(RAS-only REFRESH)*

t_{ref}	Horizontal display enable inactive to RAS-only refresh delay	16/18tc	-	ns {8-dot/9-dot}
t_{ras}	RAS pulse width	3.5tc	-	ns
t_{rp}	RAS precharge	2.5tc	-	ns
t_{asr}	Row address setup time	0.5tc	-	ns
t_{rs}	Row address hold time	tc	-	ns

t_t = minimum (3 ns) transition time
t_c = clock period

Notes:

1. Minimum time indicated is for non-page mode, 8-dot cycle.
   Maximum time indicated is for page mode cycle [CRT read cycle].
2. These timings are more relaxed in page mode operation and minimum times are controlled by 8-dot cycle timings.
3. Read cycle timings are similar to 8-dot cycle timings.
4. Write cycle is not a page mode cycle, hence timings indicated are 8-dot cycle timings.
5. All DRAM timings are listed at a maximum clock rate of 20 MHz during production.

* : Timings numbers are guaranteed by design, and are not tested.

T-52-33-45

ZyVGA DRAM Timing Waveforms *(high bandwidth mode and RAS-only REFRESH)*

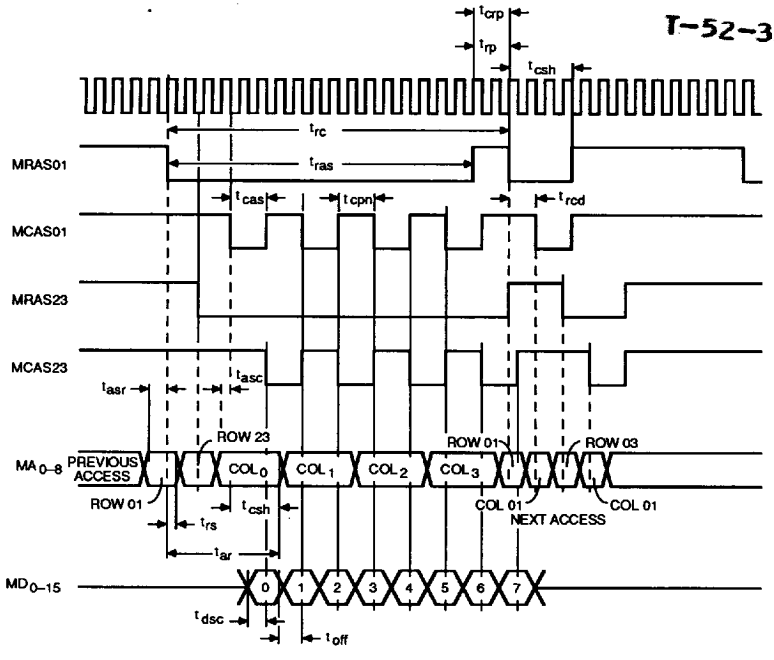


Diagram 13. Page Mode Timing

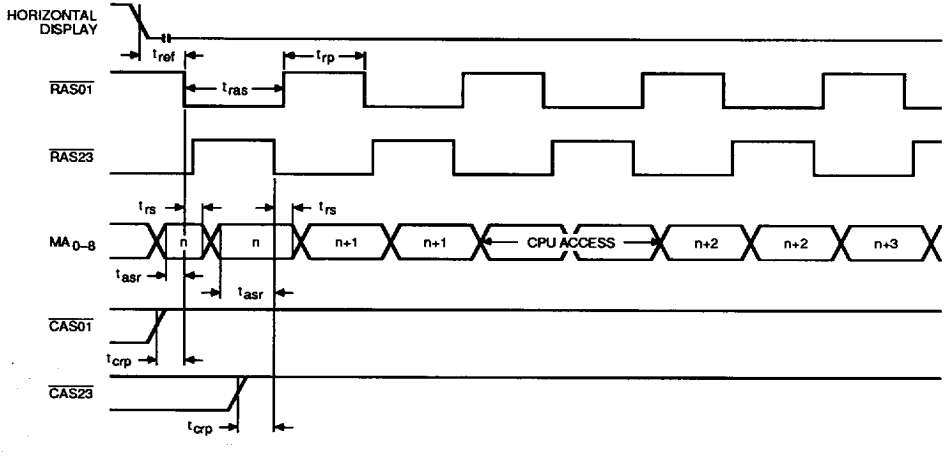
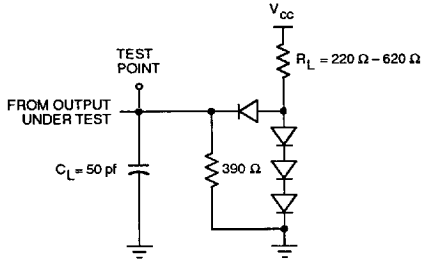


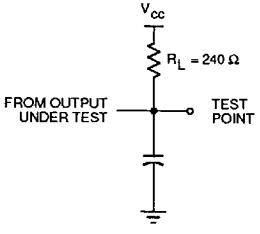
Diagram 14. RAS-only REFRESH Timing

Output Test Load Network

Standard Outputs



Open Collector Outputs



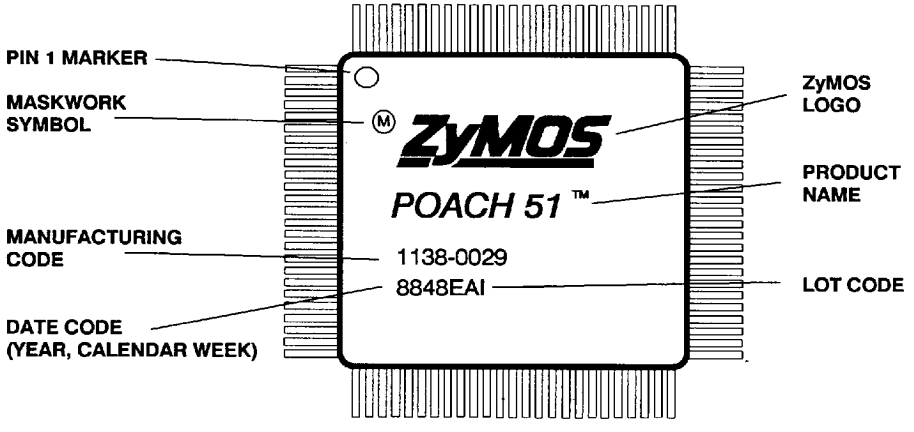


Figure 5. POACH 51 Flatpack Package Marking Detail

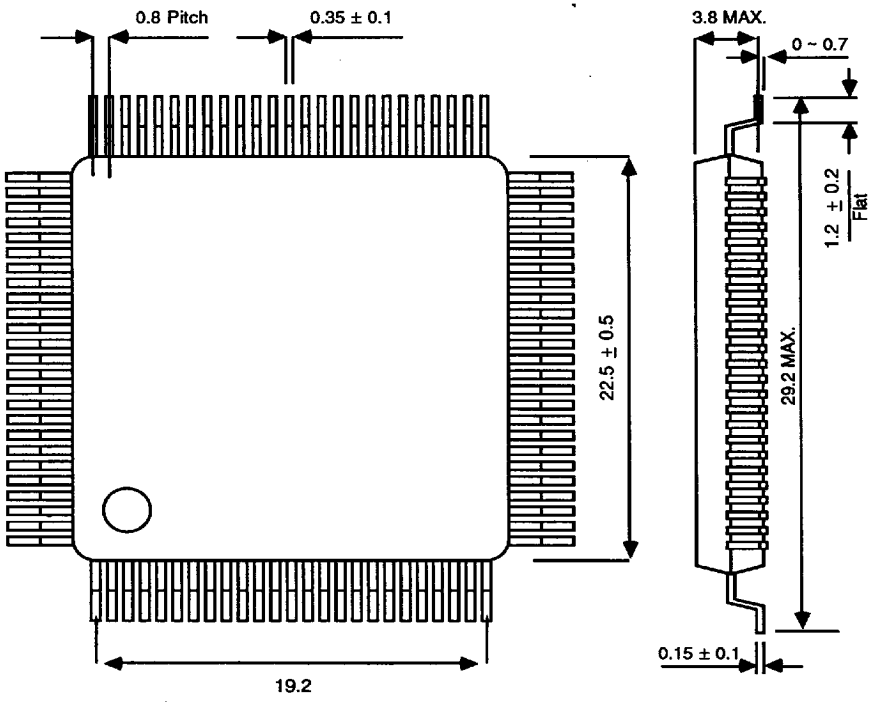


Figure 6. POACH 51 100-pin Flatpack Package Dimensions *(in millimeters)*