LINEAR INTEGRATED CIRCUIT

TIMER

The NE555 series are a monolithic integrated circuit and high stable device for generating accurate time delay or oscillation.

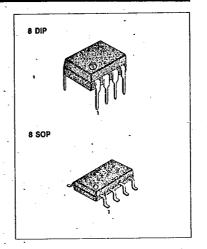
FEATURES

- Turn off time less than $2\mu s$
- Maximum operating frequency greater than 500KHz
- Timing from microseconds to hours
 Operates in both astable and monostable modes
- · High output current
- Adjustable duty cycle
- Temperature stability of 0.005% per °C

APPLICATIONS

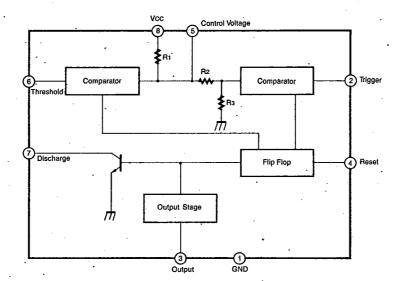
- Precision timing
- Time delay generationPulse generation
- Pulse position modulation
- Sequential timing
 Missing pulse detector

BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
NE555IN	8 DIP	- 40 ~ + 85°C
NE555ID	8 SOP	-40~+650
NE555CN	8 DIP	0 ~ + 70°C
NE555CD	8 SOP	1 0~+70 C



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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit	
Supply Voltage	V _{cc}	16	٧	
Lead Temperature (soldering 10 sec)	T _{lead}	300	°C	
Power Dissipation	P _D	600	mW	
Operating Temperature NE555I	Topr	-40~+85	°C	
NE555C		0~+70	°C	
Storage Temperature	. T _{stg}	-65 ~ + 150	°C	

ELECTRICAL CHARACTERISTICS

 $(T_a=25^{\circ}C, V_{CC}=5\sim15V, \text{ unless otherwise specified})$

Characteristic ·	Symbol	Test Conditions	Min	Тур	Max	Unit
Supply Voltage	V _{cc}		4.5		. 16	٧
Supply Current	Icc	V _{cc} = 5V, R _L =∞		3	6	mA
* ₁ (low stable)		V _{CC} = 15V, R _L =∞		10	15	mA
⁴ Timing Error (Monsotable) ² Initial Accurary Drift with Temperature Drift with Supply Voltage	MT ₁	$R_A = 1K\Omega \text{ to} \cdot$ $100K\Omega$ $C = 0.1\mu\text{F}$		1.0 50 0.1	3.0 0.5	% ppm/°C %/V
*Timing Error (astable) ² Initial Accurary Drift with Temperature Drift with Supply Voltage	MT ₂	$R_A = 1K$ to $100K\Omega$ $C = 0.1\mu F$	•	2.25 150 0.3		% ppm/°C %/V
		V _{cc} = 15V	9.0	10.0	11.0	V
Control Voltage	Vc	V _{cc} = 5V	2.6	3.33	4.0	V
		V _{cc} = 15V		10.0	0 3.0 0 0.5 1 0.5 25 00 3 3 4.0 .0 11.0 33 4.0 .0 33 1 0.25 67 2.2 6 5.6 5 2.0 7 1.0	٧
Threshold Voltage	V _{TH}	V _{CC} = 5V		. 3.33		٧
*3Threshold Current	I _{TH}			0.1	0.25	μΑ
Trigger Voltage	V _{TR}	V _{cc} = 5	1.1	1.67	2.2	V
Trigger Voltage	V _{TR}	V _{cc} = 15V	4.5	5	5.6	V
Trigger Current	I _{TR}	$V_T = 0V$		0.5	2.0	μΑ
Reset Voltage	V _{RE}		0.4	0.7	1.0	٧
Reset Current	IRE			0.1	0.4	mA

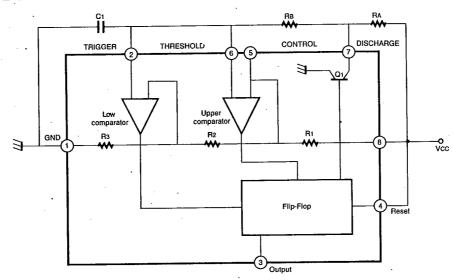
LINEAR INTEGRATED CIRCUIT

ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{∞} =5~15V, unless otherwise specified) .

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
Output Voltage (low)	V _{OL}	V _{CC} = 15V I _{sink} = 10mA I _{sink} = 50mA		0.1 0.4	0.25 0.75	V
		$V_{CC} = 5V$ $I_{sink} = 5mA$		0.25	0.35	v
Output Voltage (high)	V _{OH}	V _{CC} = 15V I _{source} = 200mA I _{source} = 100mA	12.75	12.5 13.3		. V
		V _{CC} = 5V I _{source} = 100mA	2.75	3.3		- V
Rise Time of Output	Tr			100		nsec
Fall Time of Output	T _f			100		nsec
Discharge Leakage Current	l _D			20	100	nA

APPLICATION CIRCUIT



- 1. Supply current when output is high is typically 1mA less at V_{CC} =5V.
- 2. Tested at Vcc = 5.0V and Vcc = 15V
- 2. This will determine the maximum value of $R_A + R_B$ for 15V operation, the max total $R = 20M\Omega$, and for 5V operation the max total R=6.7M Ω .





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APPLICATION NOTE

The application circuit shows a table mode.

The pin 6 (threshold) tied to the pin 2 (trigger) and pin 4 (reset) tied to Vcc (pin 8).

The external capacitor C₁ of pin 6 and pin 2 charges through R_A, R_B and discharges through R_B only.

In the internal circuit of the NE555 one input of upper comparator is the $2/3 \text{ V}_{CC}(^*R_1 = R_2 = \tilde{R}_3)$, another input of it connected pin 6.

As soon as charging C_1 is higher than 2/3 V_{CC} , discharge transistor Q_1 turn on and C_1 discharges to collector of transistor Q_1 . Therefore flip-flop circuit is reset and output is low.

One input of lower comparator is the 1/3 V_{CC} , discharge transistor Q_1 turn off and C_1 charges through R_A and R_B . Therefore filip-flop circuit is set and output is high.

So to say, when C_1 charges through H_A and H_B output is high and when C_1 discharges through H_B output is low The charge time (output is high) T_1 is 0.693 ($H_A + H_B$) C_1 and the discharge time (output is low) T_2 is 0.693 ($H_B + H_B$) C_1).

$$(I_n \frac{V_{CC}-1/3V_{CC}}{V_{CC}-2/3V_{CC}} = 0.693)$$

Thus the total period time T is given by $T=T_1+T_2=0.693$ (R_A+2R_B). C_1 . Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_1}$$

The duty cycle is given by

$$D.C = \frac{T_2}{T} = \frac{R_B}{R_A + 2R_B}$$

If you make use of the NE556 you can make two astable mode.

If you want another application note, request information on our timer IC application circuit designer.