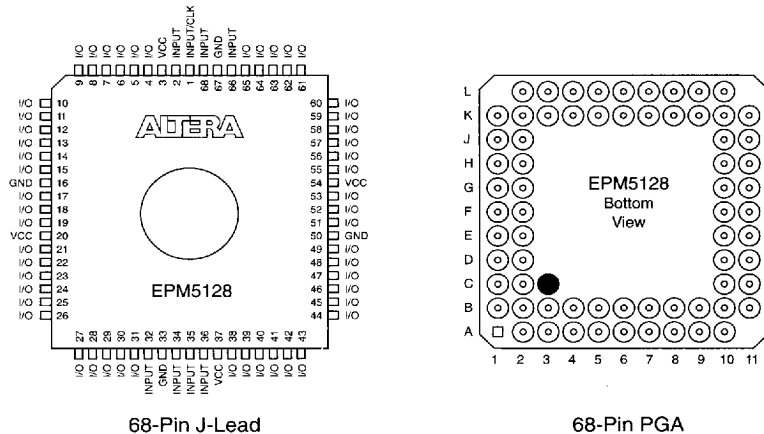


Features

- High-density, 128-macrocell, general-purpose MAX 5000 EPLD
- High-speed multi-LAB architecture
 - t_{PD} as fast as 15 ns
 - Counter frequencies up to 83.3 MHz
 - Pipelined data rates up to 100 MHz
- 256 shareable expander product terms (“expanders”) allowing over 32 product terms in a single macrocell
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- Available in windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 14):
 - 68-pin J-lead chip carrier (JLCC and PLCC)
 - 68-pin grid array (ceramic PGA only)
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 14. EPM5128 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 4 and 5 in this data sheet for pin-out information. Windows in ceramic packages only.



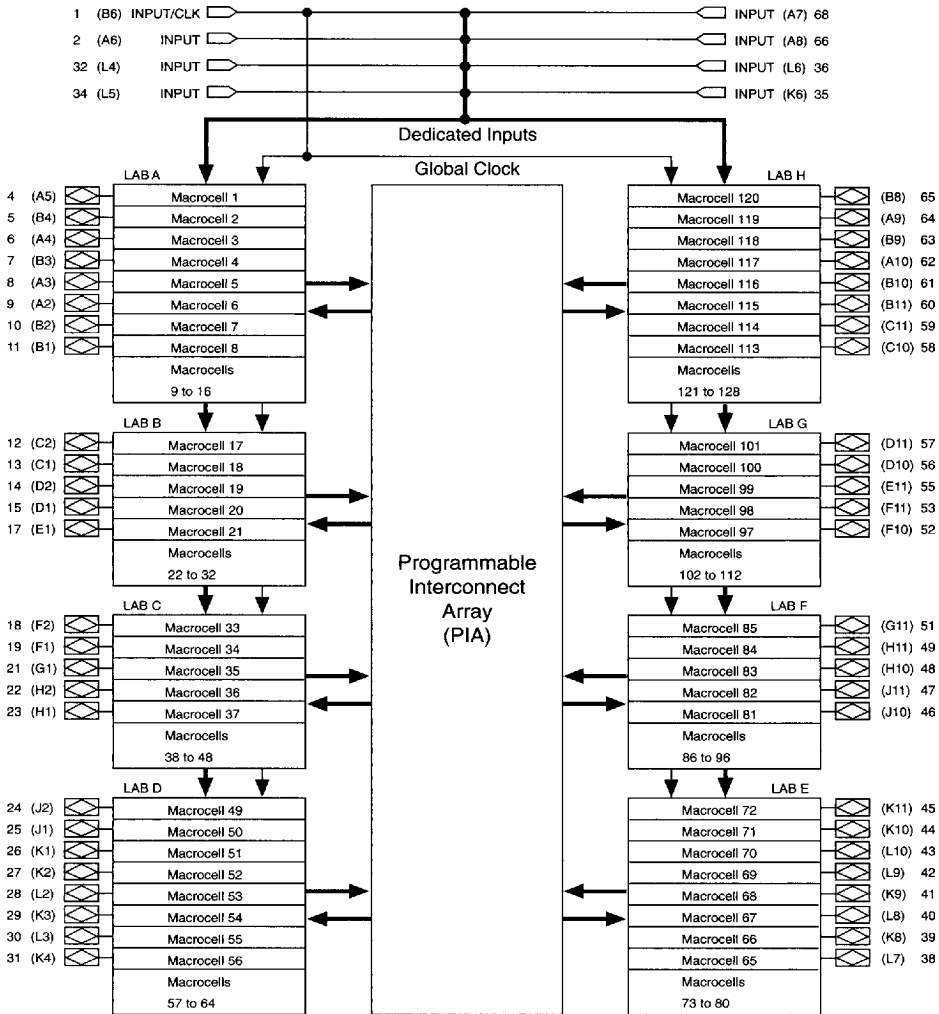
General Description

Altera EPM5128 EPLDs are user-configurable, high-performance MAX 5000 EPLDs that provide high-density replacements for 74-series SSI, MSI TTL, and CMOS logic. For example, a 74161 counter uses only 3% of the EPM5128 EPLD. These devices can replace over 60 TTL MSI and SSI components and integrate multiple 20- and 24-pin low-density PLDs.

The EPM5128 consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs) of 16 macrocells. Each LAB also contains 32 expander product terms. They each have 8 dedicated input pins, one of which can be used as a global system Clock. These devices contain 52 I/O pins that can be configured for input, output, or bidirectional operation. Four of the LABs have 8 I/O pins; the other 4 have 5 I/O pins. See Figure 15.

Figure 15. EPM5128 Block Diagram

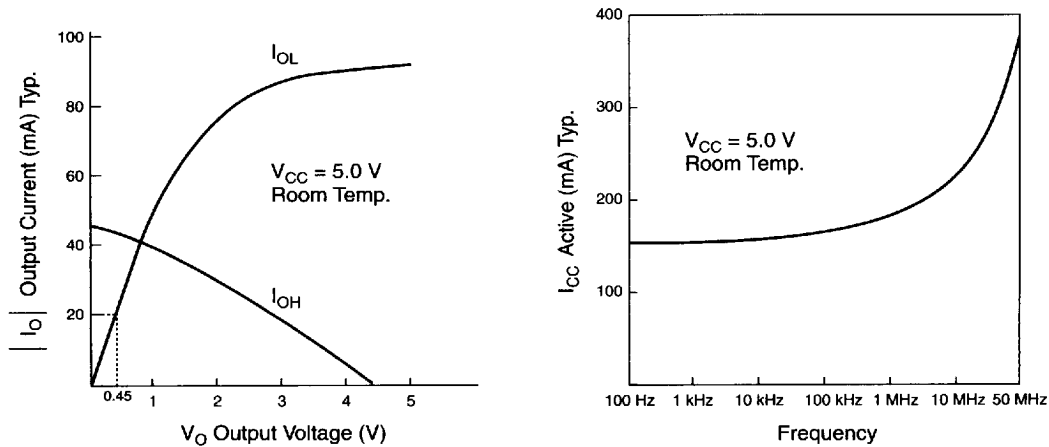
Numbers without parentheses are for J-lead packages. Numbers in parentheses are for PGA packages



7
MAX 5000

Figure 16 shows the output drive characteristics of EPM5128 I/O pins and typical supply current (I_{CC}) versus frequency.

Figure 16. Typical Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	With respect to GND	-2.0	7.0	V
V _I	DC input voltage	Note (1)	-2.0	7.0	V
I _{MAX}	DC V _{CC} or GND current			500	mA
I _{OUT}	DC output current, per pin		-25	25	mA
P _D	Power dissipation			2500	mW
T _{STG}	Storage temperature	No bias	-65	150	°C
T _{AMB}	Ambient temperature	Under bias, Note (2)	-65 [-55]	135 [125]	°C
T _J	Junction temperature	Under bias, Note (2)		150 [175]	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	Notes (3), (4)	4.75 (4.5)	5.25 (5.5)	V
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
T _A	Operating temperature	For commercial use	0	70	°C
T _A	Operating temperature	For industrial use	-40	85	°C
T _C	Case temperature	For military use	-55	125	°C
t _R	Input rise time			100	ns
t _F	Input fall time			100	ns

DC Operating Conditions Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	High-level input voltage	Note (2)	2.0 [2.2]		V _{CC} + 0.3	V
V _{IL}	Low-level input voltage		-0.3		0.8	V
V _{OH}	High-level TTL output voltage	I _{OH} = -4 mA DC	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA DC			0.45	V
I _I	Input leakage current	V _I = V _{CC} or GND	-10		10	μA
I _{OZ}	Tri-state output off-state current	V _O = V _{CC} or GND	-40		40	μA
I _{CC1}	V _{CC} supply current (standby)	V _I = V _{CC} or GND, Notes (3), (7)		150	225 (300)	mA
I _{CC3}	V _{CC} supply current (active)	V _I = V _{CC} or GND, No load, f = 1.0 MHz, Notes (3), (7)		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C _{IN}	Input pin capacitance	V _{IN} = 0 V, f = 1.0 MHz		10	pF
C _{IO}	I/O pin capacitance	V _{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions Note (6)

External Timing Parameters			EPM5128A-15		EPM5128A-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		25		33	ns
t_{SU}	Global clock setup time		10		13		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		9	ns
t_{CH}	Global clock high time		5		7		ns
t_{CL}	Global clock low time		5		7		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		20	ns
t_{ACH}	Array clock high time		5		7		ns
t_{ACL}	Array clock low time		5		7		ns
t_{CNT}	Minimum global clock period			12		15	ns
f_{CNT}	Max. internal global clock frequency	Note (7)	83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			12		15	ns
f_{ACNT}	Max. internal array clock frequency	Note (7)	83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	Note (9)	100.0		71.4		MHz

Internal Timing Parameters Note (10)			EPM5128A-15		EPM5128A-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Expander array delay			8		10	ns
t_{LAD}	Logic array delay			8		12	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		1		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{H}	Register hold time		7		10		ns
t_{IC}	Array clock delay			6		8	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	Prog. Interconnect Array delay			10		13	ns

AC Operating Conditions Note (6)

External Timing Parameters			EPM5128-1		EPM5128-2		EPM5128		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_H	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	Note (8)	11		14		16		ns
t_{ACL}	Array clock low time	Note (8)	9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	Note (7)	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	Note (7)	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	Note (9)	62.5		50		40		MHz

Internal Timing Parameters Note (10)			EPM5128-1		EPM5128-2		EPM5128		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_H	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

- (1) Minimum DC input is -0.3 V . During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
- (2) Numbers in brackets are for MIL-STD-883-compliant versions.
- (3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
- (4) Maximum V_{CC} rise time for the EPM5128/EPM5128A is 200 ms .
- (5) Typical values are for $T_A = 25^\circ\text{ C}$ and $V_{CC} = 5\text{ V}$.
- (6) Operating conditions: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{ C}$ to 70° C for commercial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{ C}$ to 85° C for industrial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_C = -55^\circ\text{ C}$ to 125° C for military use.
- (7) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C .
- (8) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
- (9) The f_{MAX} values represent the maximum frequency for pipelined data.
- (10) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

Pin-Out Information

Tables 4 and 5 provide pin-out information for the EPM5128.

Table 4. EPM5128 Dedicated Pin-Outs		
Dedicated Pin	68-Pin J-Lead	68-Pin PGA
INPUT/CLK	1	B6
INPUT	2, 32, 34, 35, 36, 66, 68	A6, L4, L5, L6, K6, A8, A7
GND	16, 33, 50, 67	B7, E2, G10, K5
VCC	3, 20, 37, 54	B5, E10, G2, K7

Table 5. EPM5128 I/O Pin-Outs (Part 1 of 2)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
1	A	4	A5	17	B	12	C2
2	A	5	B4	18	B	13	C1
3	A	6	A4	19	B	14	D2
4	A	7	B3	20	B	15	D1
5	A	8	A3	21	B	17	E1
6	A	9	A2	22	B	-	-
7	A	10	B2	23	B	-	-
8	A	11	B1	24	B	-	-
9	A	-	-	25	B	-	-
10	A	-	-	26	B	-	-
11	A	-	-	27	B	-	-
12	A	-	-	28	B	-	-
13	A	-	-	29	B	-	-
14	A	-	-	30	B	-	-
15	A	-	-	31	B	-	-
16	A	-	-	32	B	-	-
33	C	18	F2	49	D	24	J2
34	C	19	F1	50	D	25	J1
35	C	21	G1	51	D	26	K1
36	C	22	H2	52	D	27	K2
37	C	23	H1	53	D	28	L2
38	C	-	-	54	D	29	K3
39	C	-	-	55	D	30	L3
40	C	-	-	56	D	31	K4
41	C	-	-	57	D	-	-
42	C	-	-	58	D	-	-
43	C	-	-	59	D	-	-
44	C	-	-	60	D	-	-
45	C	-	-	61	D	-	-
46	C	-	-	62	D	-	-
47	C	-	-	63	D	-	-
48	C	-	-	64	D	-	-

7

MAX 5000

Table 5. EPM5128 I/O Pin-Outs (Part 2 of 2)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
65	E	38	L7	81	F	46	J10
66	E	39	K8	82	F	47	J11
67	E	40	L8	83	F	48	H10
68	E	41	K9	84	F	49	H11
69	E	42	L9	85	F	51	G11
70	E	43	L10	86	F	-	-
71	E	44	K10	87	F	-	-
72	E	45	K11	88	F	-	-
73	E	-	-	89	F	-	-
74	E	-	-	90	F	-	-
75	E	-	-	91	F	-	-
76	E	-	-	92	F	-	-
77	E	-	-	93	F	-	-
78	E	-	-	94	F	-	-
79	E	-	-	95	F	-	-
80	E	-	-	96	F	-	-
97	G	52	F10	113	H	58	C10
98	G	53	F11	114	H	59	C11
99	G	55	E11	115	H	60	B11
100	G	56	D10	116	H	61	B10
101	G	57	D11	117	H	62	A10
102	G	-	-	118	H	63	B9
103	G	-	-	119	H	64	A9
104	G	-	-	120	H	65	B8
105	G	-	-	121	H	-	-
106	G	-	-	122	H	-	-
107	G	-	-	123	H	-	-
108	G	-	-	124	H	-	-
109	G	-	-	125	H	-	-
110	G	-	-	126	H	-	-
111	G	-	-	127	H	-	-
112	G	-	-	128	H	-	-