The Atmel ATF1500
44-pin Complex PLD

Introduction

The ATF1500 is Atmel's newest Complex PLD. It is a 44-pin device built on an advanced Flash technology. It has maximum pin-to-pin delay of 7.5 ns. With 32 I/O macrocells, each containing a flip-flop, the ATF1500 can easily integrate several TTL, SSI, MSI and simple PLDs. In terms of logic density, the ATF1500 provides an intermediate solution between Atmel's 24-pin ATV750B (20 flip-flops) and the high-density 44-pin ATV2500B (48 flip-flops).

The ATF1500 has several power and speed management options. The ATF1500L device offers Atmel's unique low-power standby mode. When there are no input transitions, the "L" device will automatically power-down to a low-power mode. In addition, the ATF1500 has an optional pin-controlled power-down mode. In this mode, one of the pins is configured as a power-down pin. A high signal on this pin will put the device into a zero-power mode (typically in the (A range).

For software support, Atmel developed an ATF1500 fitter that interfaces with industry-standard PLD tools such as ABEL, CUPL and Synario. Atmel offers its own versions of these tools at a reduced cost. For converting existing designs, Atmel provides a POF2JED utility that reads a POF programming file and creates an ATF1500 JEDEC file.

Architecture Overview

The ATF1500 has 32 I/O pins and 4 input-only pins. Each I/O pin is associated with a logic macrocell containing a flip-flop. Each flip-flop is configurable as a D- or T-type register, or transparent latch. Each macrocell also has a buried feedback, allowing the macrocell logic to be used even if the I/O pin is used as an input. All the macrocells are connected by a global bus that routes all inputs, I/Os and macrocell feedbacks signals to every macrocell in the device.

Each ATF1500 macrocell contains five product terms. Additional logic requiring more product terms can be implemented using either Cascade or Foldback Logic. The Cascade Logic allows logic product terms to be borrowed from an adjacent macrocell. Up to eight macrocells can be cascaded together to create a sum term of up to 40 product terms. The Foldback Logic term implements a NAND function. There is a Foldback Logic term in each macrocell, providing up to 32 NAND functions in the device. Both logic expansion methods are automatically implemented by the ATF1500 fitter, and each incurs a small propagation delay.

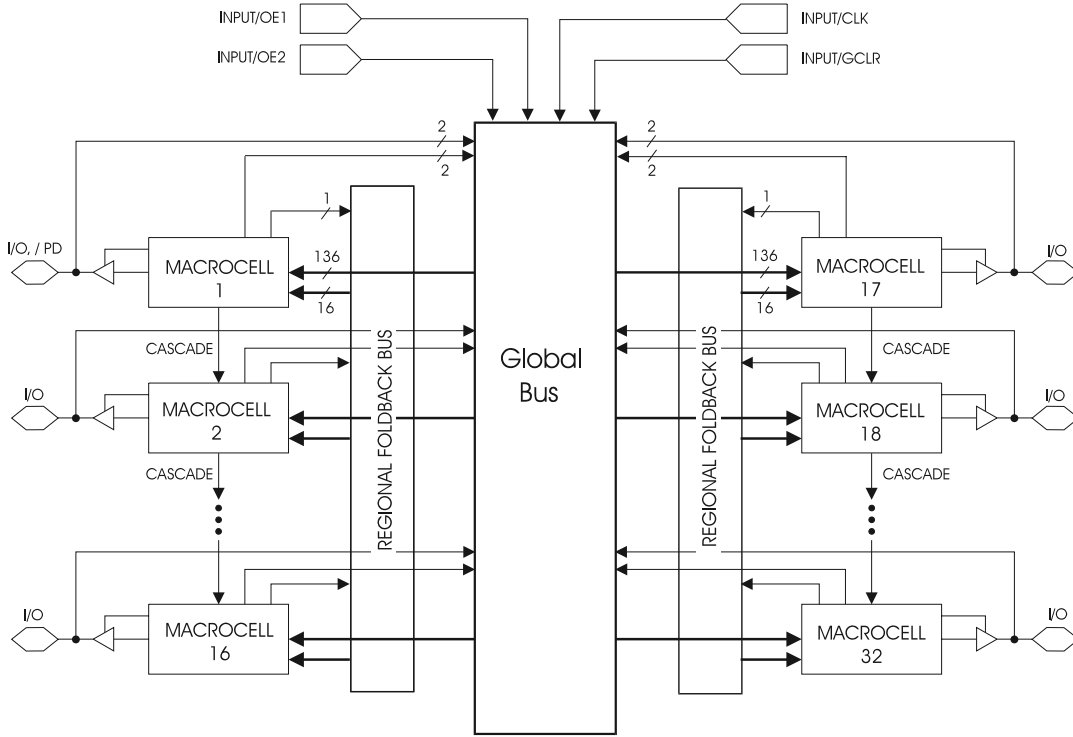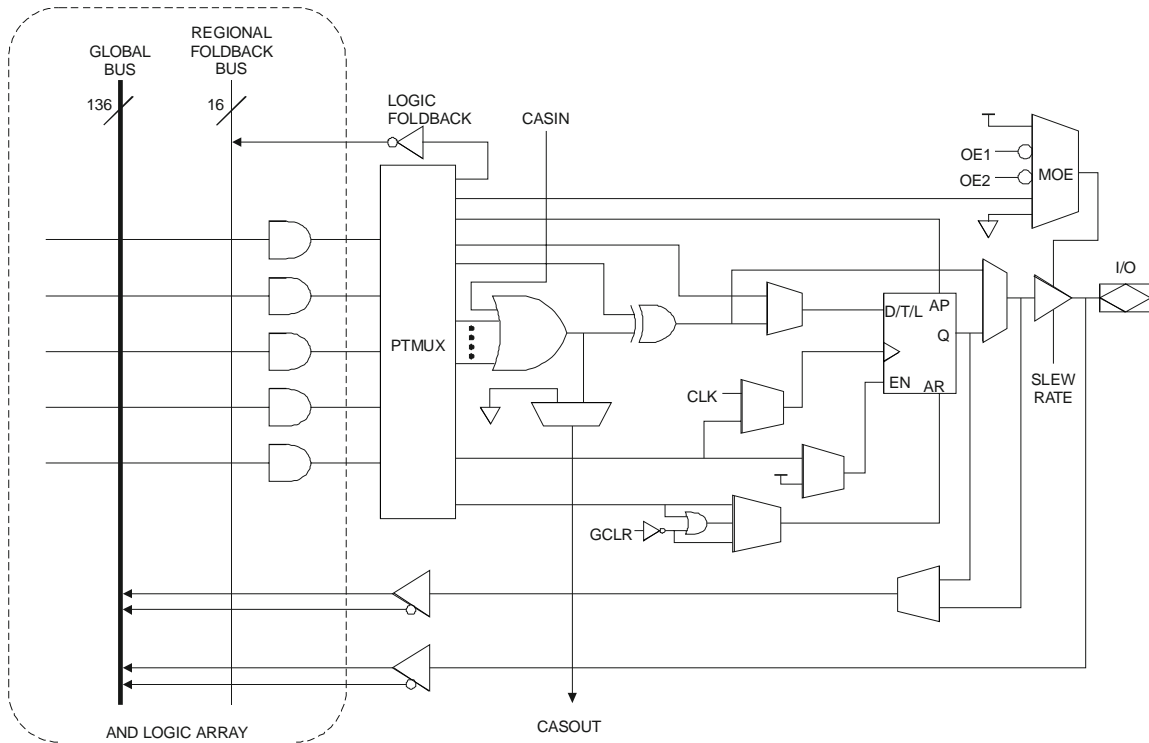**Figure 1.** ATF1500 Logic Block Diagram

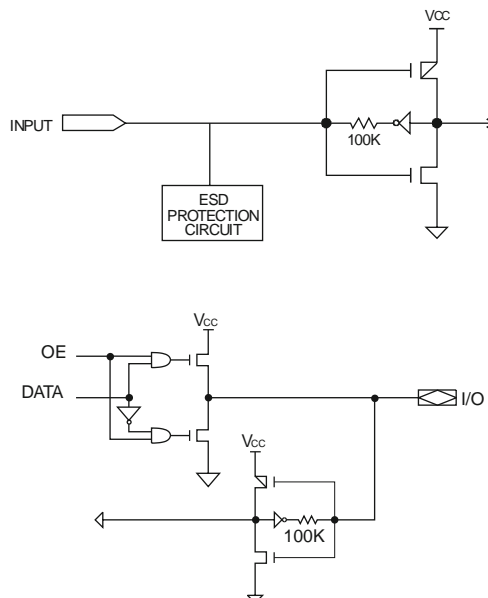**Figure 2.** ATF1500 Macrocell Diagram

ATF1500 Key Features

Some of the ATF1500 key functional features are summarized below:

• Global Bus connected to every macrocell to eliminate routing bottlenecks, to increase logic utilization and enable design changes with fixed pin placements.

• Independent configurable D- or T-type flip-flop, or transparent Latch.

• Global pin or product term controlled Output Enable for each I/O.

• Global pin or product term controlled Clock or Reset for each flip-flop in the macrocell.

• Macrocell configuration providing a Combinatorial output along with a buried register feedback.

• Pin-controlled or automatic power-down options to reduce overall system power consumption.

• Slew rate control for each output to reduce overall system noise.

• Programming time of less than 10 seconds.

ATF1500 Bus-friendly Pin-keeper Inputs and I/Os

All Input and I/O pins on the ATF1500 have bus-friendly "data-keeper" circuits. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This prevents the inputs or I/Os from floating to an intermediate voltage, and hence reduces power consumption, system noise and eliminating the need for external pull-up resistors.
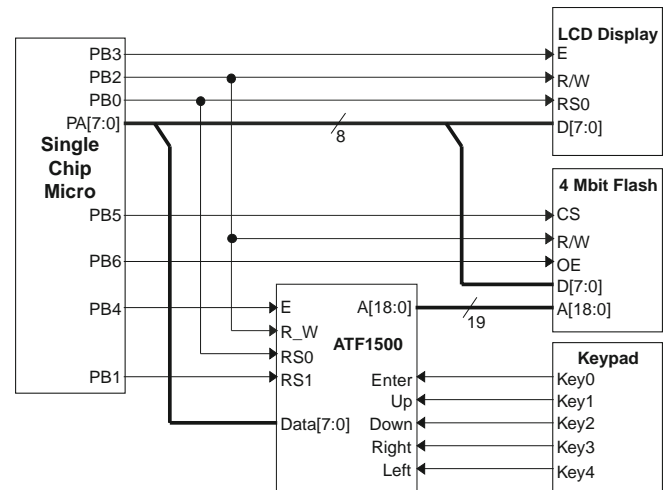
Figure 3. ATF1500 Input and I/O Circuitry

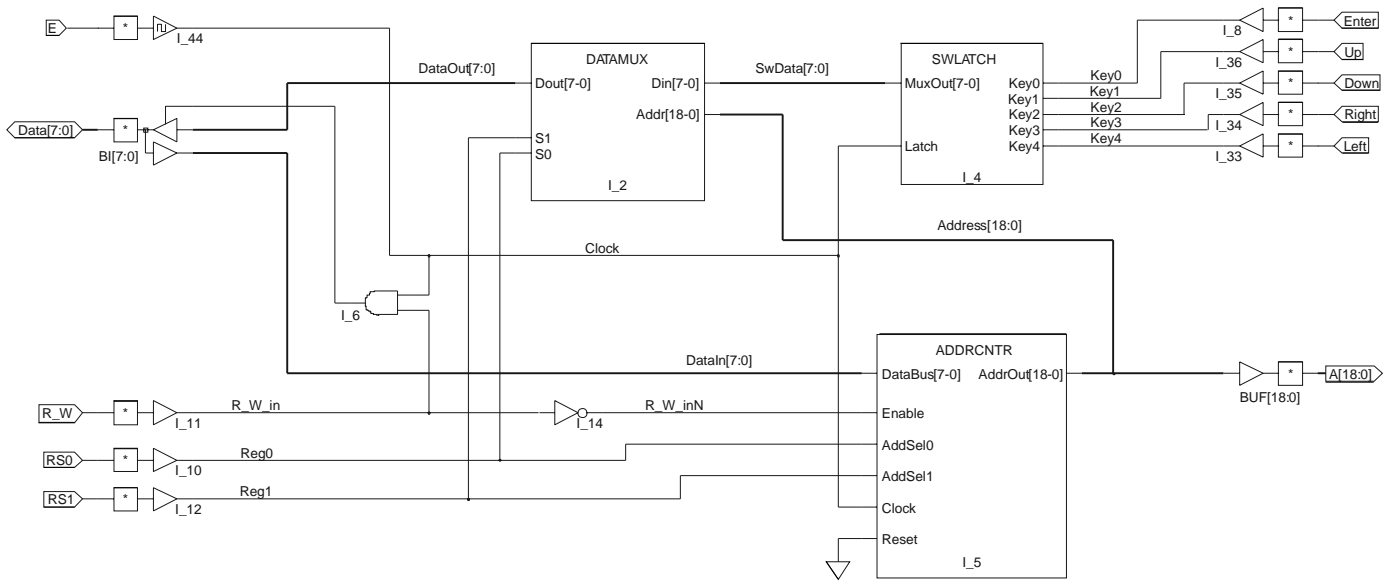## ATF1500 Design Example – Memory and I/O Interface to a Single-chip Microprocessor

This is a microprocessor based design to display large volumes of text on a 2 line by 16 character LCD display using a simple keypad. The design was implemented using a single microprocessor chip that interfaced to the LCD display, a 5-key keypad, a 4 MB Flash memory and an ATF1500 CPLD (see Figure 4). The Flash memory stores the text. Since the single microprocessor chip does not have an external address or data bus, these signals must be generated by the ATF1500 device via control signals from the I/O ports on the CPU.

Figure 4. System Block Diagram

The customer implemented the design using the Data I/O Synario Development tool. Figure 5 shows the block diagram of the interface design for the logic in the ATF1500. The design consists of three logic blocks: Address Counter (ADDRCNTR); Data Multiplexer (DATAMUX) and Switch Latch (SWLATCH) blocks. Since all the data in the Flash memory is in the form of text strings, the address of the first character of a string can be loaded into the 19-bit counter. The counter is then clocked each time a byte is read by the CPU, making the next character available immediately. The SWLATCH block contains latches to hold the keypad data. The DATAMUX block enables the CPU to read not just the keypad data, but also the condition of the counter.

Figure 5. Memory and I/O Interface Design in the ATF1500

Key Device Features Utilized in the Memory and I/O Interface Design

The following lists the key device features that allowed this Memory and I/O Interface design example to fit efficiently in an ATF1500 device.

1. Global Connectivity of the ATF1500: The capability of the ATF1500 to provide 100% connectivity between all macrocells allows both the 19-bit and 8-bit Address and Data busses to be routed throughout the device. This feature eliminates any routing bottlenecks and efficiently utilizes all device resources for logic implementation. Due to the high interconnectivity between the three logic blocks (ADDRCNTR, DATAMUX and SWLATCH blocks), this design would not fit if global connectivity were not available.

2. Output Enable Product Term for each I/O: As shown in Figure 5, the design required an output enable product term for the OE control of the bi-directional DATA pins. If output enable product terms are not available, then two pins (an input and an I/O pin) will be needed to generate the output enable control logic, i.e. externally wiring the output pin to the input pin. The two additional pins would have prevented the design from fitting into the ATF1500 because all 36 input and I/O pins were used in the design.

3. Latch Configuration for the Macrocell Register: Each register of the ATF1500 macrocell can be configured as a transparent latch. In the Memory and I/O Interface design, five latches were needed to latch the keypad data.

4. Buried Feedback Path from each Macrocell: The buried feedback paths of the ATF1500 macrocells allowed the macrocell logic to be used even when the I/O pins associated with these macrocells are configured as inputs for the Keypad signals.

5. Bus Friendly Pin-keeper Circuits: The bus-friendly "pin-keeper" circuits on the ATF1500 Input and I/O pins eliminated the need of external pull-up resistors on the bi-directional DATA pins (connected to the 8-bit Data bus).

Acknowledgment: This Memory and I/O Interface design was contributed by Jim Millener of JCM II, Inc.

Summary

The ATF1500 is a high-performance, high-density Flash-based Complex PLD. It has flexible macrocells that are globally connected, and a variety of speed and power management features. It is available in a 44-lead PLCC or TQFP package. For software support, Atmel provides a fitter that interfaces with ABEL, CUPL and Synario tools. For converting existing designs, Atmel provides the POF2JED utility that reads a POF programming file and creates an ATF1500 JEDEC file.

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High-performance Flash PLD

Application Note

Rev. 0731B–09/99

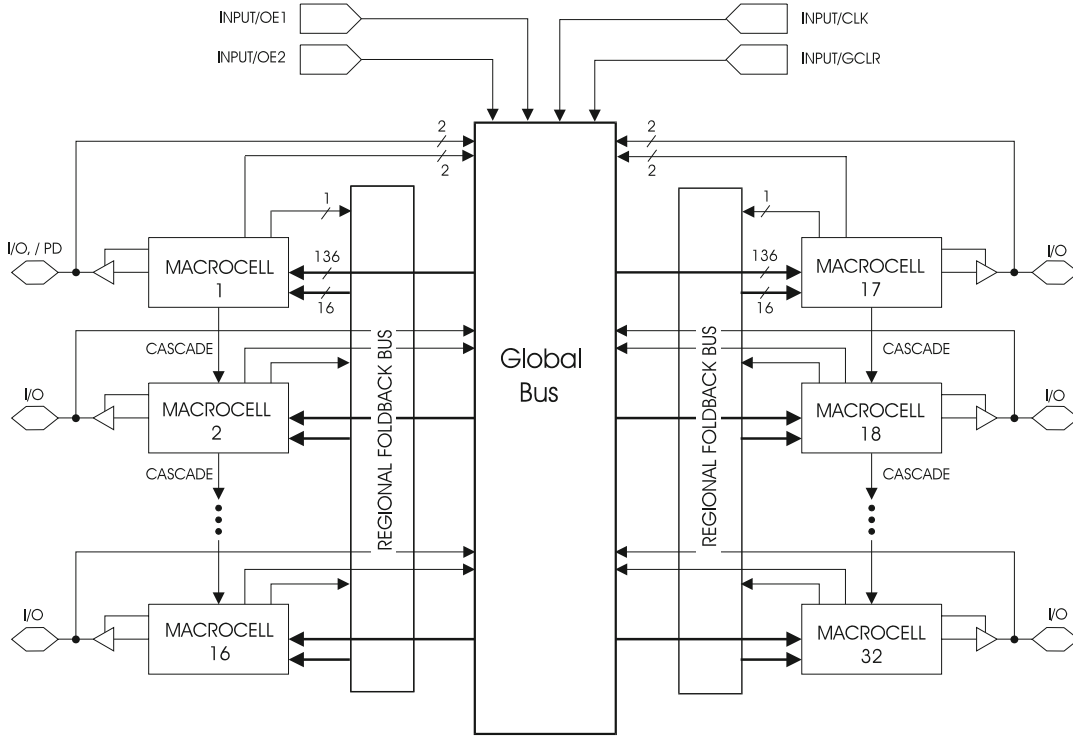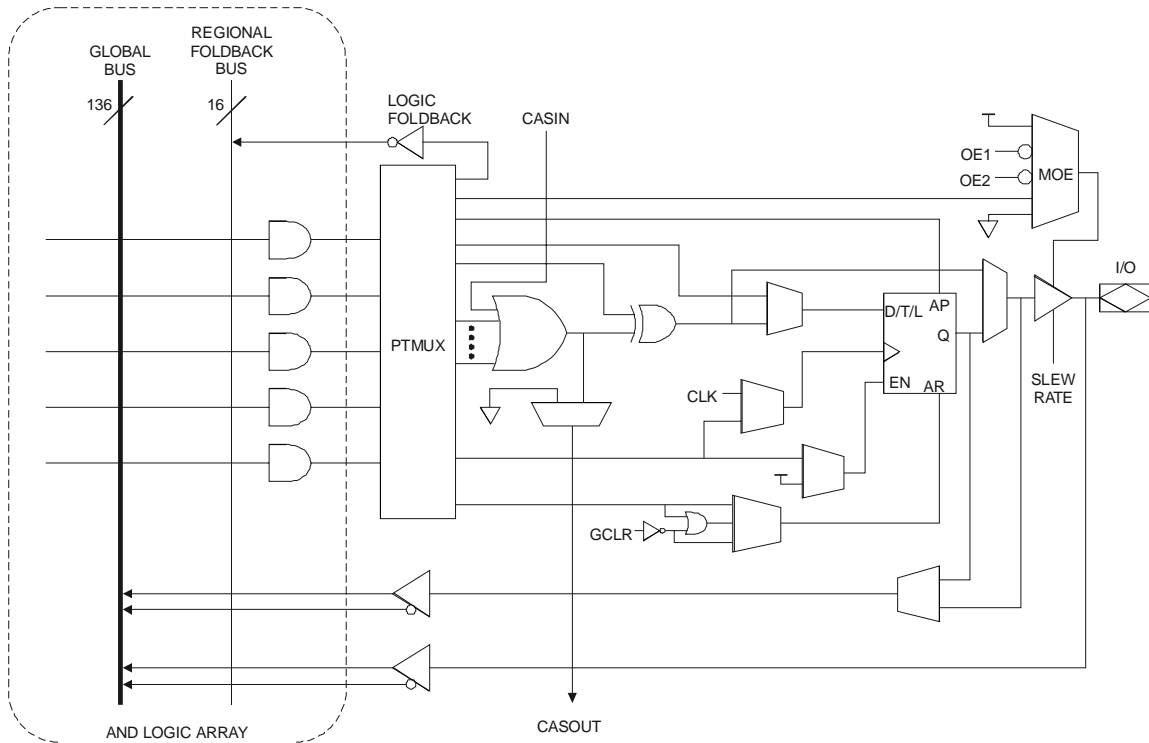**Figure 1.** ATF1500 Logic Block Diagram

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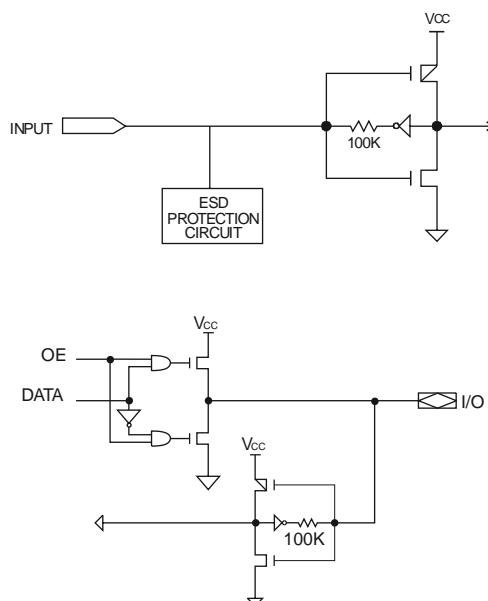
Flash PLD

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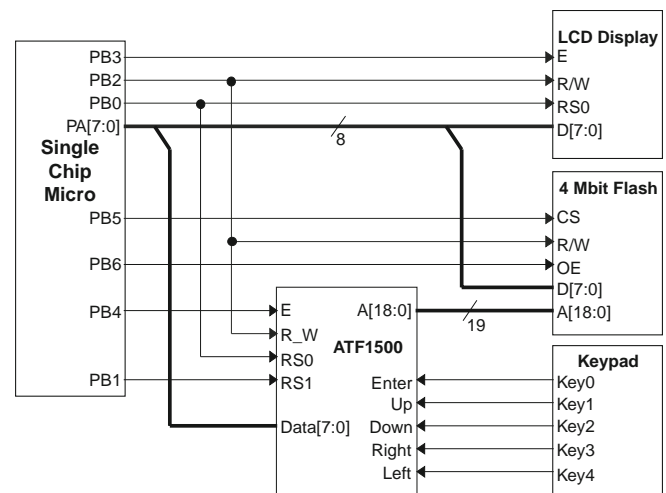
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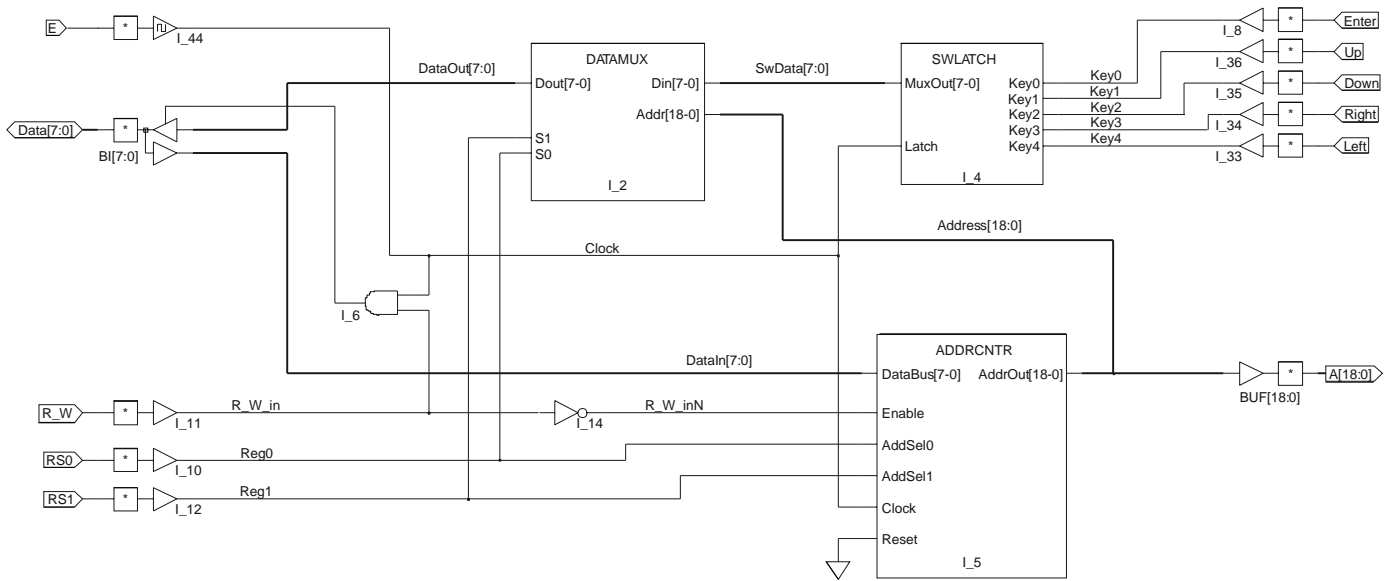
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