

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 1 M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μ PD42S16160L, 4216160L, 42S18160L, 4218160L are 1,048, 576 words by 16 bits CMOS dynamic RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the μ PD42S16160L, 42S18160L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

Features

- 1,048,576 words by 16 bits organization
- Single +3.3 V ± 0.3 V power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μ PD42S16160L-A50, 4216160L-A50	396 mW	50 ns	90 ns	35 ns
μ PD42S18160L-A50, 4218160L-A50	612 mW			
μ PD42S16160L-A60, 4216160L-A60	324 mW	60 ns	110 ns	40 ns
μ PD42S18160L-A60, 4218160L-A60	540 mW			
μ PD42S16160L-A70, 4216160L-A70	288 mW	70 ns	130 ns	45 ns
μ PD42S18160L-A70, 4218160L-A70	504 mW			

- The μ PD42S16160L, 42S18160L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μ PD42S16160L	4,096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μ PD42S18160L	1,024 cycles/128 ms		
μ PD4216160L	4,096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)
μ PD4218160L	1,024 cycles/16 ms		

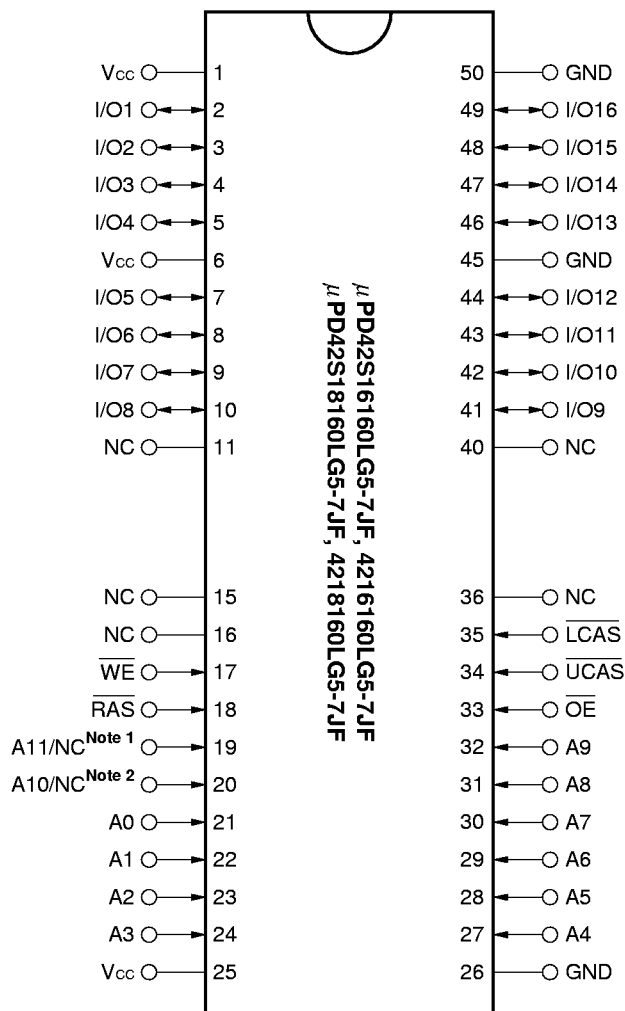
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★ Ordering Information

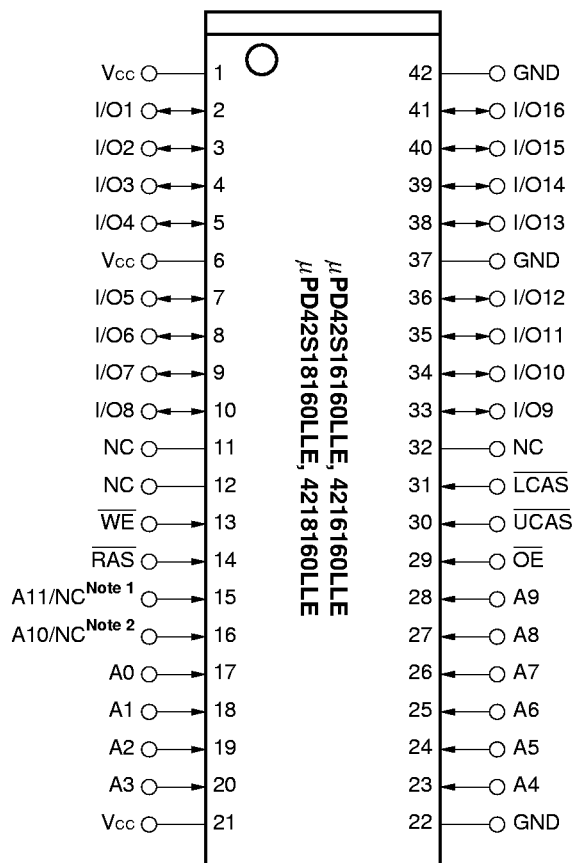
Part number	Access time (MAX.)	Package	Refresh
μPD42S16160LG5-A50-7JF	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S18160LG5-A50-7JF			
μPD42S16160LG5-A60-7JF	60 ns		
μPD42S18160LG5-A60-7JF			
μPD42S16160LG5-A70-7JF	70 ns		
μPD42S18160LG5-A70-7JF			
μPD42S16160LLE-A50	50 ns	42-pin plastic SOJ (400 mil)	
μPD42S18160LLE-A50			
μPD42S16160LLE-A60	60 ns		
μPD42S18160LLE-A60			
μPD42S16160LLE-A70	70 ns		
μPD42S18160LLE-A70			
μPD4216160LG5-A50-7JF	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD4218160LG5-A50-7JF			
μPD4216160LG5-A60-7JF	60 ns		
μPD4218160LG5-A60-7JF			
μPD4216160LG5-A70-7JF	70 ns		
μPD4218160LG5-A70-7JF			
μPD4216160LLE-A50	50 ns	42-pin plastic SOJ (400 mil)	
μPD4218160LLE-A50			
μPD4216160LLE-A60	60 ns		
μPD4218160LLE-A60			
μPD4216160LLE-A70	70 ns		
μPD4218160LLE-A70			

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)



42-pin Plastic SOJ (400 mil)



Notes 1. A11 ... μ PD42S16160L, 4216160L NC ... μ PD42S18160L, 4218160L

2. A10 ... μ PD42S16160L, 4216160L NC ... μ PD42S18160L, 4218160L

A0 to A11 : Address Inputs

I/O1 to I/O16 : Data Inputs/Outputs

$\overline{\text{RAS}}$: Row Address Strobe

$\overline{\text{UCAS}}$: Column Address Strobe (upper)

$\overline{\text{LCAS}}$: Column Address Strobe (lower)

$\overline{\text{WE}}$: Write Enable

$\overline{\text{OE}}$: Output Enable

Vcc : Power Supply

GND : Ground

NC : No Connection

Input/Output Pin Functions

The μ PD42S16160L, 4216160L, 42S18160L, 4218160L have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ^{Note 1}, $\overline{\text{WE}}$, $\overline{\text{OE}}$, Address^{Note 2} and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
$\overline{\text{CAS}}$ (Column address strobe)	Input	$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A _x ^{Note 2} (Address input)	Input	Address bus. Input total 20-bit of address signal, upper bits and lower bits ^{Note 2} in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data input/ output)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Notes 1. $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.

2.

Part number	Address inputs	Upper bits	Lower bits
μ PD42S16160L, 4216160L	A0 - A11	12 bits	8 bits
μ PD42S18160L, 4218160L	A0 - A9	10 bits	10 bits

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than $100 \mu\text{s}$ ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ inactive) and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	$^{\circ}\text{C}$

Capacitance ($T_A = 25^{\circ}\text{C}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

★ DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[μ PD42S16160L, 4216160L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		110	mA	1, 2, 3
				$t_{\text{RAC}} = 60 \text{ ns}$		90		
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
Standby current	$\mu\text{PD42S16160L}$	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$			0.5	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$			0.15		
	$\mu\text{PD4216160L}$		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$			2.0		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$			0.5		
$\overline{\text{RAS}}$ only refresh current		I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}$ $t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		110	mA	1, 2, 3, 4
				$t_{\text{RAC}} = 60 \text{ ns}$		90		
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL (MAX.)}}, \overline{\text{CAS}}$ cycling $t_{\text{PC}} = t_{\text{PC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		100	mA	1, 2, 5
				$t_{\text{RAC}} = 60 \text{ ns}$		90		
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current		I _{CC5}	$\overline{\text{RAS}}$ cycling $t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$		110	mA	1, 2
				$t_{\text{RAC}} = 60 \text{ ns}$		90		
				$t_{\text{RAC}} = 70 \text{ ns}$		80		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (4,096 cycles / 128 ms, only for the $\mu\text{PD42S16160L}$)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $t_{\text{RC}} = 31.3 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}:$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH (MAX.)}}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address: V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ $I_{\text{O}} = 0 \text{ mA}$	$t_{\text{RAS}} \leq 300 \text{ ns}$		400	μA	1, 2
				$t_{\text{RAS}} \leq 1 \mu\text{s}$		500	μA	1, 2
Self refresh current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for the $\mu\text{PD42S16160L}$)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}:$ $t_{\text{RAS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH (MAX.)}}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_{\text{O}} = 0 \text{ mA}$			200	μA	2
Input leakage current		I _{I (L)}	$V_{\text{I}} = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V		-5	+5	μA	
Output leakage current		I _{O (L)}	$V_{\text{O}} = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)		-5	+5	μA	
High level output voltage		V _{OH}	$I_{\text{O}} = -2.0 \text{ mA}$		2.4		V	
Low level output voltage		V _{OL}	$I_{\text{O}} = +2.0 \text{ mA}$			0.4	V	

[μ PD42S18160L, 4218160L]

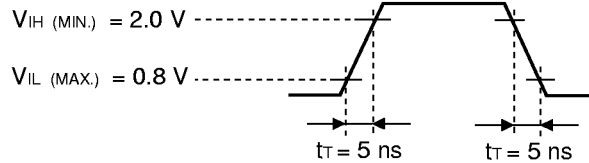
Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	170	mA	1, 2, 3
				$t_{\text{RAC}} = 60 \text{ ns}$	150		
				$t_{\text{RAC}} = 70 \text{ ns}$	140		
Standby current	μ PD42S18160L	I _{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}, I_o = 0 \text{ mA}$		0.5	mA	
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_o = 0 \text{ mA}$		0.15		
	μ PD4218160L		$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}, I_o = 0 \text{ mA}$		2.0		
			$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_o = 0 \text{ mA}$		0.5		
RAS only refresh current		I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}$ $t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	170	mA	1, 2, 3, 4
				$t_{\text{RAC}} = 60 \text{ ns}$	150		
				$t_{\text{RAC}} = 70 \text{ ns}$	140		
Operating current (Fast page mode)		I _{CC4}	$\overline{\text{RAS}} \leq V_{\text{IL (MAX.)}}, \overline{\text{CAS}}$ cycling $t_{\text{PC}} = t_{\text{PC (MIN.)}}, I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	100	mA	1, 2, 5
				$t_{\text{RAC}} = 60 \text{ ns}$	90		
				$t_{\text{RAC}} = 70 \text{ ns}$	80		
CAS before RAS refresh current		I _{CC5}	$\overline{\text{RAS}}$ cycling $t_{\text{RC}} = t_{\text{RC (MIN.)}}, I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 50 \text{ ns}$	170	mA	1, 2
				$t_{\text{RAC}} = 60 \text{ ns}$	150		
				$t_{\text{RAC}} = 70 \text{ ns}$	140		
CAS before RAS long refresh current (1,024 cycles / 128 ms, only for the μ PD42S18160L)		I _{CC6}	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh: $t_{\text{RC}} = 125.0 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}:$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH (MAX.)}}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby: $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address: V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ $I_o = 0 \text{ mA}$	$t_{\text{RAS}} \leq 300 \text{ ns}$	300	μA	1, 2
				$t_{\text{RAS}} \leq 1 \mu\text{s}$	400	μA	1, 2
Self refresh current (CAS before RAS self refresh, only for the μ PD42S18160L)		I _{CC7}	$\overline{\text{RAS}}, \overline{\text{CAS}}:$ $t_{\text{RASS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH (MAX.)}}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$		200	μA	2
Input leakage current		I _{I (L)}	$V_i = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	-5	+5	μA	
Output leakage current		I _{O (L)}	$V_o = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage		V _{OH}	$I_o = -2.0 \text{ mA}$	2.4		V	
Low level output voltage		V _{OL}	$I_o = +2.0 \text{ mA}$		0.4	V	

- Notes**
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{\text{RAS}} \leq V_{\text{IL (MAX.)}}$ and $\overline{\text{CAS}} \geq V_{\text{IH (MIN.)}}$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

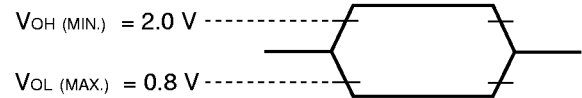
★ AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

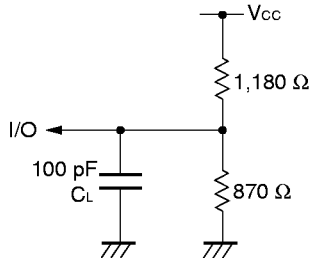
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		t _{RC}	90	—	110	—	130	—	ns	
RAS precharge time		t _{RP}	30	—	40	—	50	—	ns	
CAS precharge time		t _{CPN}	8	—	10	—	10	—	ns	
RAS pulse width		t _{RAS}	50	10,000	60	10,000	70	10,000	ns	1
CAS pulse width		t _{CAS}	13	10,000	15	10,000	20	10,000	ns	
RAS hold time		t _{RSH}	13	—	15	—	18	—	ns	
CAS hold time		t _{CSH}	50	—	60	—	70	—	ns	
RAS to CAS delay time		t _{RCD}	18	35	20	45	20	50	ns	2
RAS to column address delay time		t _{RAD}	13	25	15	30	15	35	ns	2
CAS to RAS precharge time		t _{CRP}	5	—	5	—	5	—	ns	3
Row address setup time		t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time		t _{RAH}	8	—	10	—	10	—	ns	
Column address setup time		t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time		t _{CAH}	10	—	10	—	15	—	ns	
OE lead time referenced to RAS		t _{OES}	0	—	0	—	0	—	ns	
CAS to data setup time		t _{CLZ}	0	—	0	—	0	—	ns	
OE to data setup time		t _{OLZ}	0	—	0	—	0	—	ns	
OE to data delay time		t _{OED}	10	—	13	—	15	—	ns	
Masked byte write hold time referenced to RAS		t _{MRH}	0	—	0	—	0	—	ns	
Transition time (rise and fall)		t _T	3	50	3	50	3	50	ns	
Refresh time	μPD42S16160L, 42S18160L	t _{REF}	—	128	—	128	—	128	ms	4
	μPD4216160L		—	64	—	64	—	64	ms	
	μPD4218160L		—	16	—	16	—	16	ms	

- Notes 1.** In $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, $t_{\text{RAS}}(\text{MAX.})$ is 100 μs .
 If 10 μs < t_{RAS} < 100 μs , $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied.
- 2.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}}(\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

- 3.** $t_{\text{CRP}}(\text{MIN.})$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
- 4.** This specification is applied only to the μ PD42S16160L, 42S18160L.

Read Cycle

Parameter	Symbol	$t_{\text{RAC}} = 50 \text{ ns}$		$t_{\text{RAC}} = 60 \text{ ns}$		$t_{\text{RAC}} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	1
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	20	ns	1
Access time from column address	t_{AA}	—	25	—	30	—	35	ns	1
Access time from $\overline{\text{OE}}$	t_{OEA}	—	13	—	15	—	20	ns	
Column address lead time referenced to $\overline{\text{RAS}}$	t_{RAL}	25	—	30	—	35	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	2
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	2
Output buffer turn-off delay time from $\overline{\text{OE}}$	t_{OEZ}	0	10	0	13	0	15	ns	3
Output buffer turn-off delay time from $\overline{\text{CAS}}$	t_{OFF}	0	10	0	13	0	15	ns	3

- Notes 1.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}}(\text{MAX.})$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$ will not cause any operation problems.

- 2.** Either $t_{\text{RCH}}(\text{MIN.})$ or $t_{\text{RRH}}(\text{MIN.})$ should be met in read cycles.
- 3.** $t_{\text{OFF}}(\text{MAX.})$ and $t_{\text{OEZ}}(\text{MAX.})$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ hold time referenced to $\overline{\text{CAS}}$	t _{WCH}	8	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ pulse width	t _{WP}	8	–	10	–	10	–	ns	1
$\overline{\text{WE}}$ lead time referenced to $\overline{\text{RAS}}$	t _{RWL}	18	–	20	–	20	–	ns	
$\overline{\text{WE}}$ lead time referenced to $\overline{\text{CAS}}$	t _{CWL}	13	–	15	–	15	–	ns	
$\overline{\text{WE}}$ setup time	t _{WCS}	0	–	0	–	0	–	ns	2
$\overline{\text{OE}}$ hold time	t _{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t _{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t _{DH}	10	–	10	–	15	–	ns	3

- Notes**
1. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t _{RWC}	133	–	158	–	180	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	70	–	83	–	95	–	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	33	–	38	–	40	–	ns	1
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	45	–	53	–	60	–	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS} (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN.), t_{CWD} ≥ t_{CWD} (MIN.), t_{AWD} ≥ t_{AWD} (MIN.) and t_{CPWD} ≥ t_{CPWD} (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t _{PC}	35	—	40	—	45	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	30	—	35	—	40	ns	
$\overline{\text{RAS}}$ pulse width	t _{RASP}	50	125,000	60	125,000	70	125,000	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	8	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	30	—	35	—	40	—	ns	
Read modify write cycle time	t _{PRWC}	73	—	83	—	90	—	9ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t _{CPWD}	50	—	58	—	65	—	ns	1

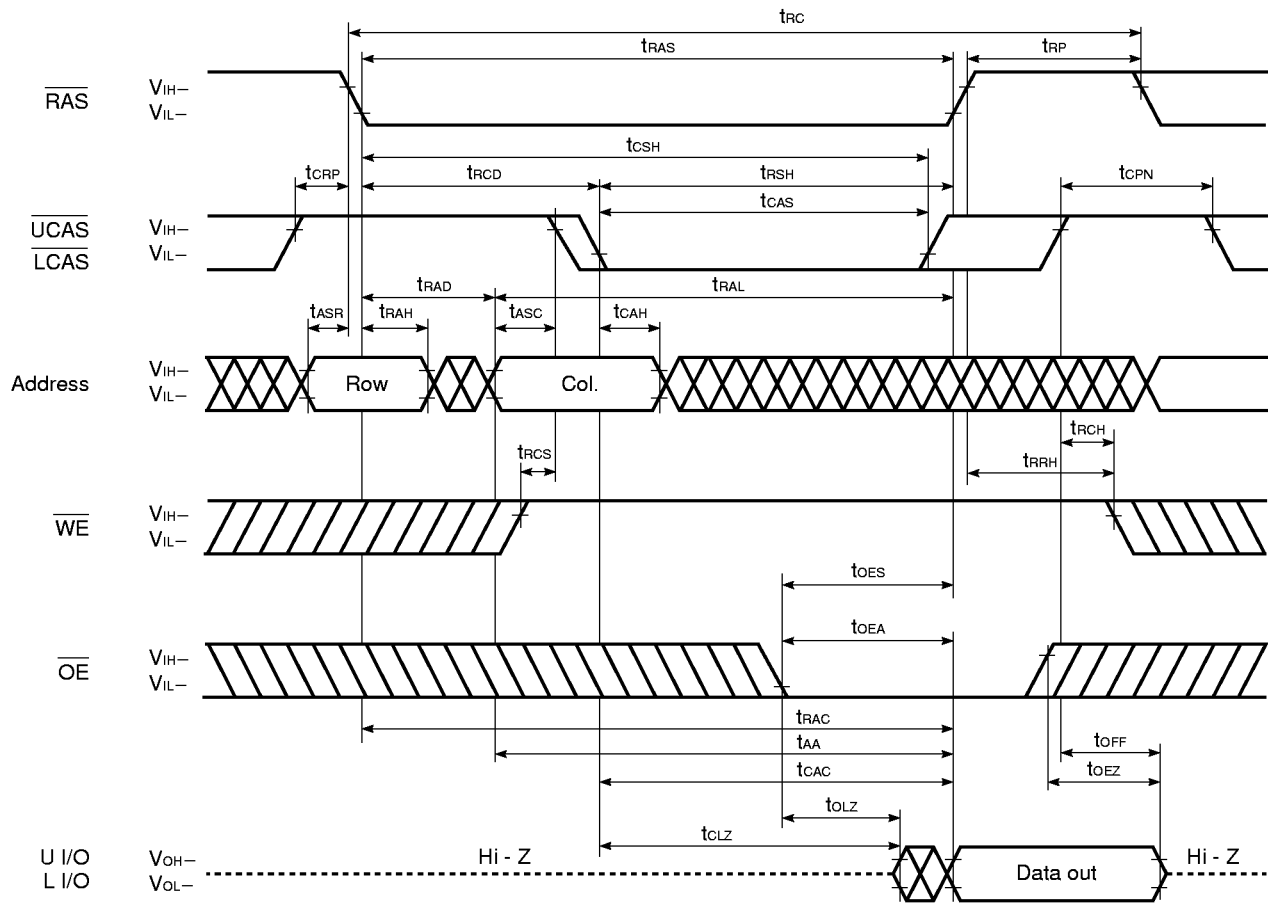
Note 1. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{MIN.})$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{MIN.})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{MIN.})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{MIN.})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{MIN.})$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

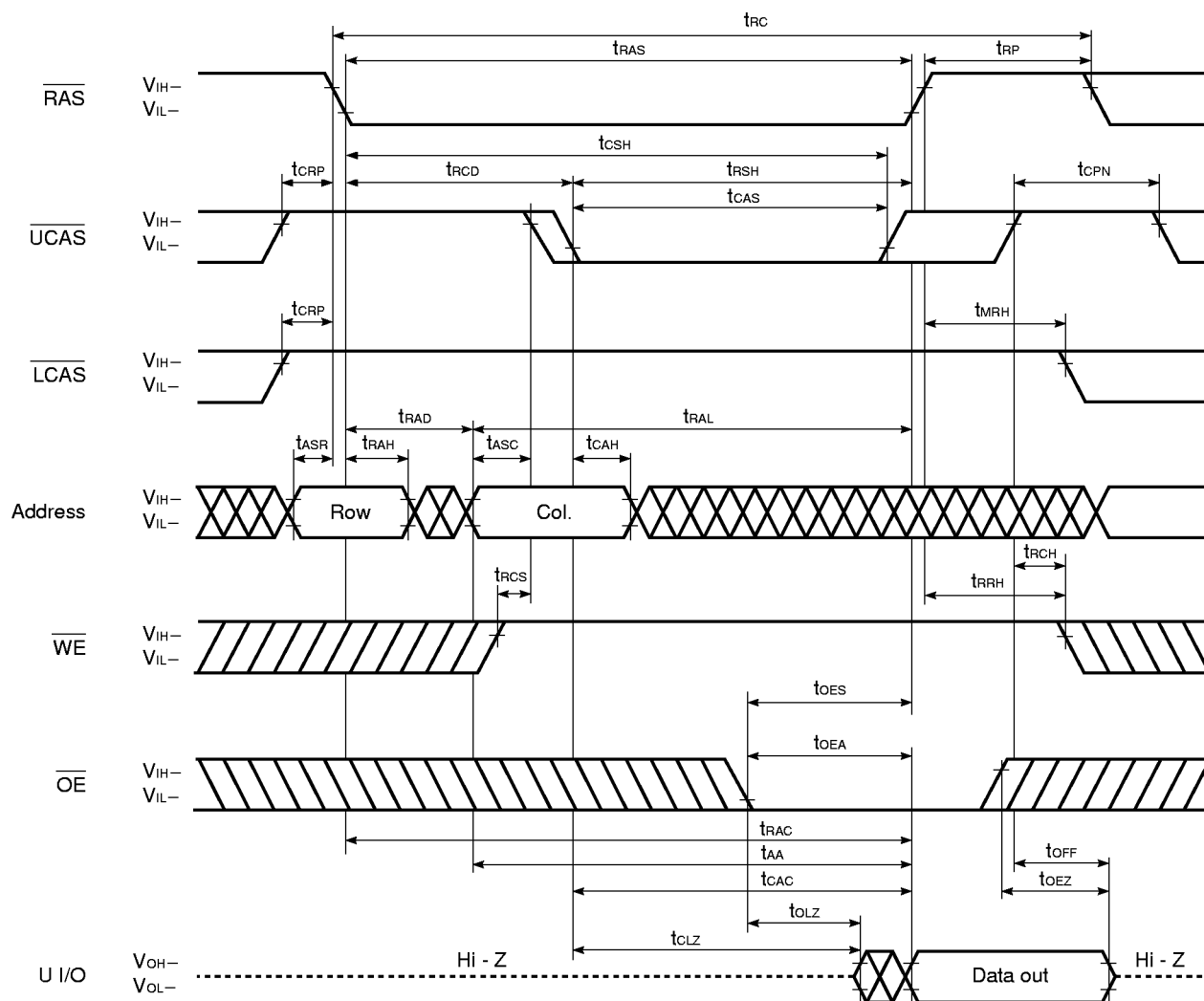
Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	t _{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t _{RPC}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RASS}	100	—	100	—	100	—	μ s	1
$\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{RPS}	90	—	110	—	130	—	ns	1
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t _{CHS}	–50	—	–50	—	–50	—	ns	1
$\overline{\text{WE}}$ hold time	t _{WHR}	15	—	15	—	15	—	ns	

Note 1. This specification is applied only to the μ PD42S16160L, 42S18160L.

Read Cycle

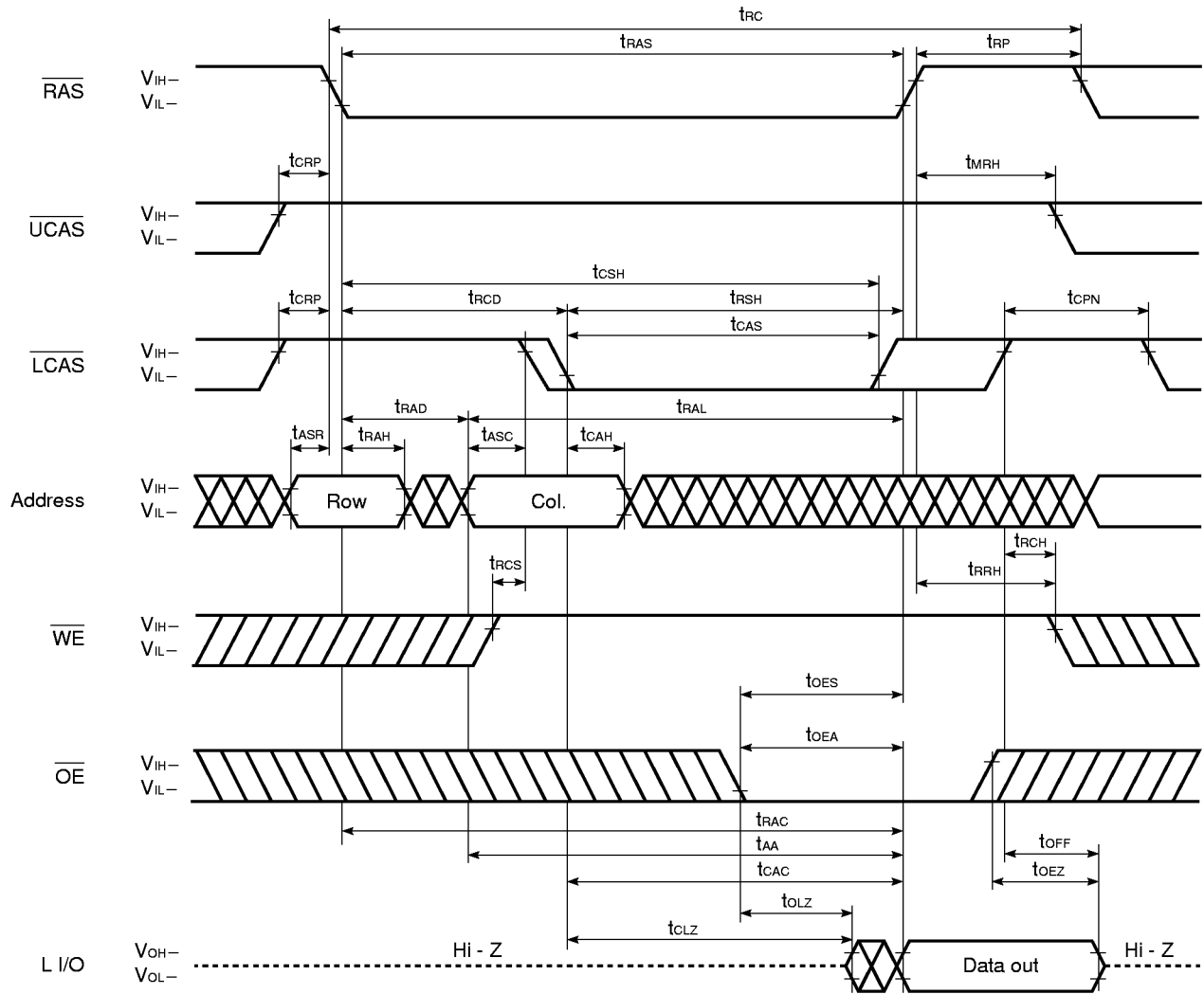


Upper Byte Read Cycle



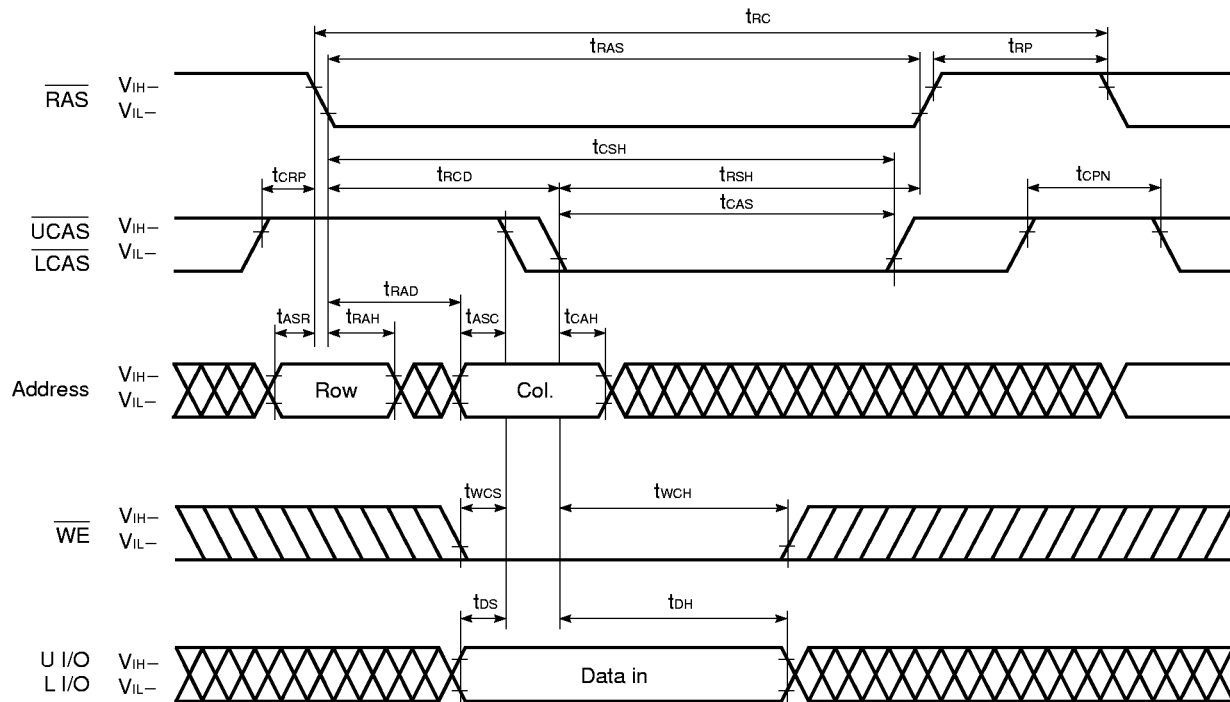
Remark L I/O: Hi-Z

Lower Byte Read Cycle



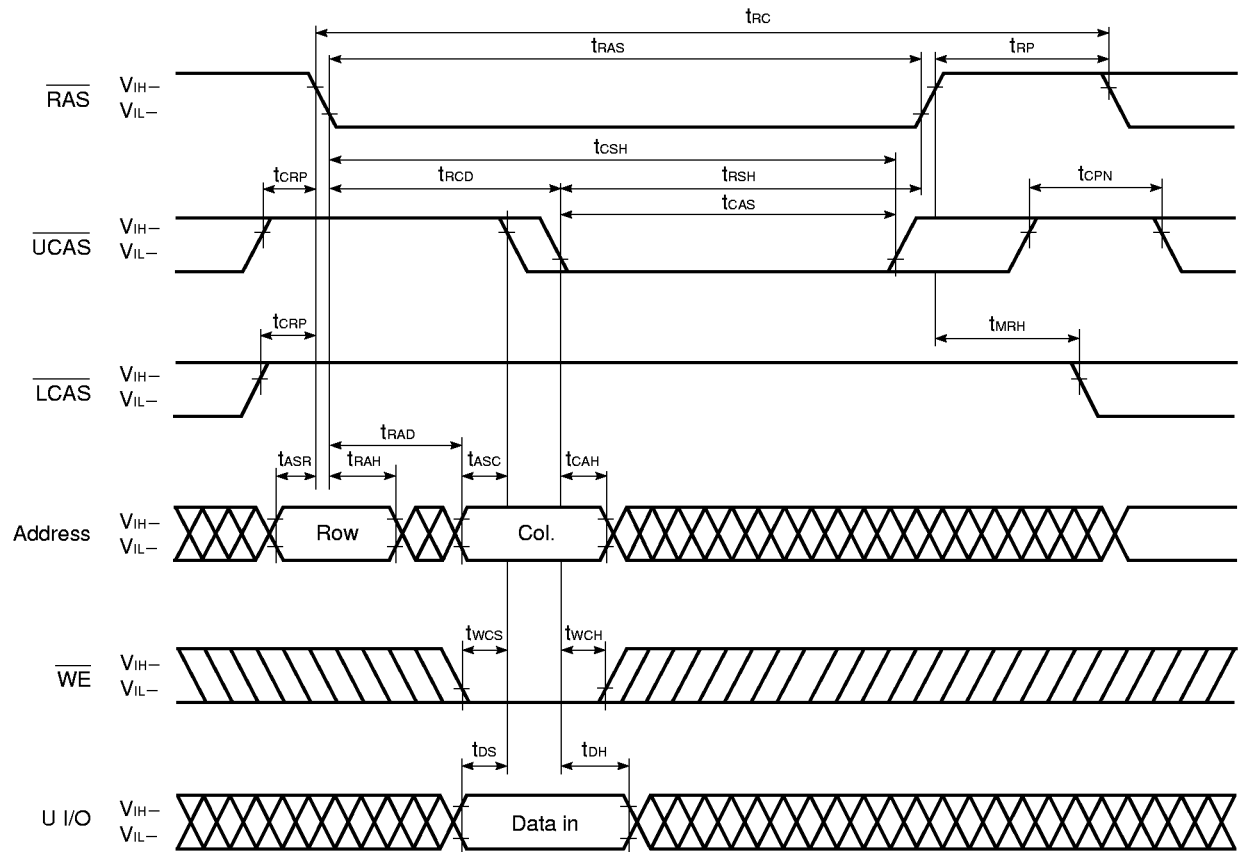
Remark U I/O: Hi-Z

Early Write Cycle



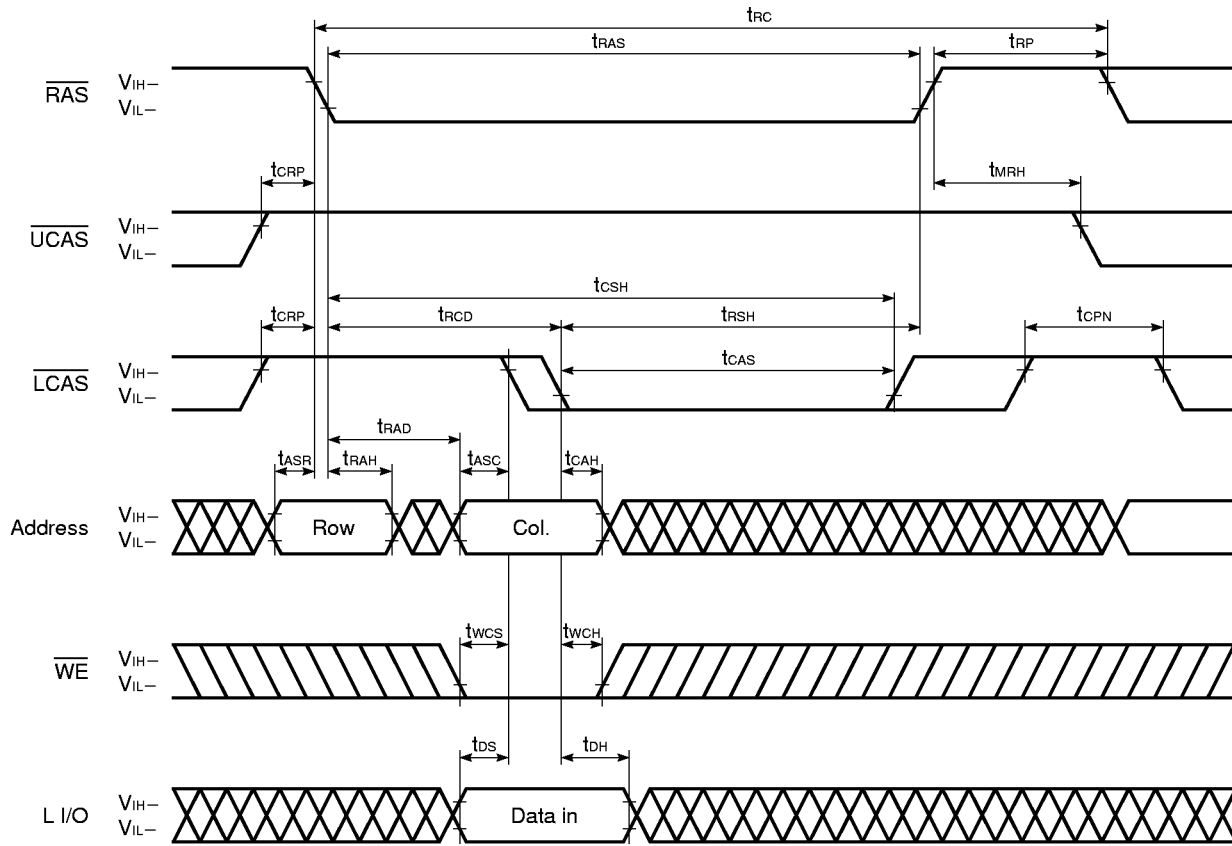
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



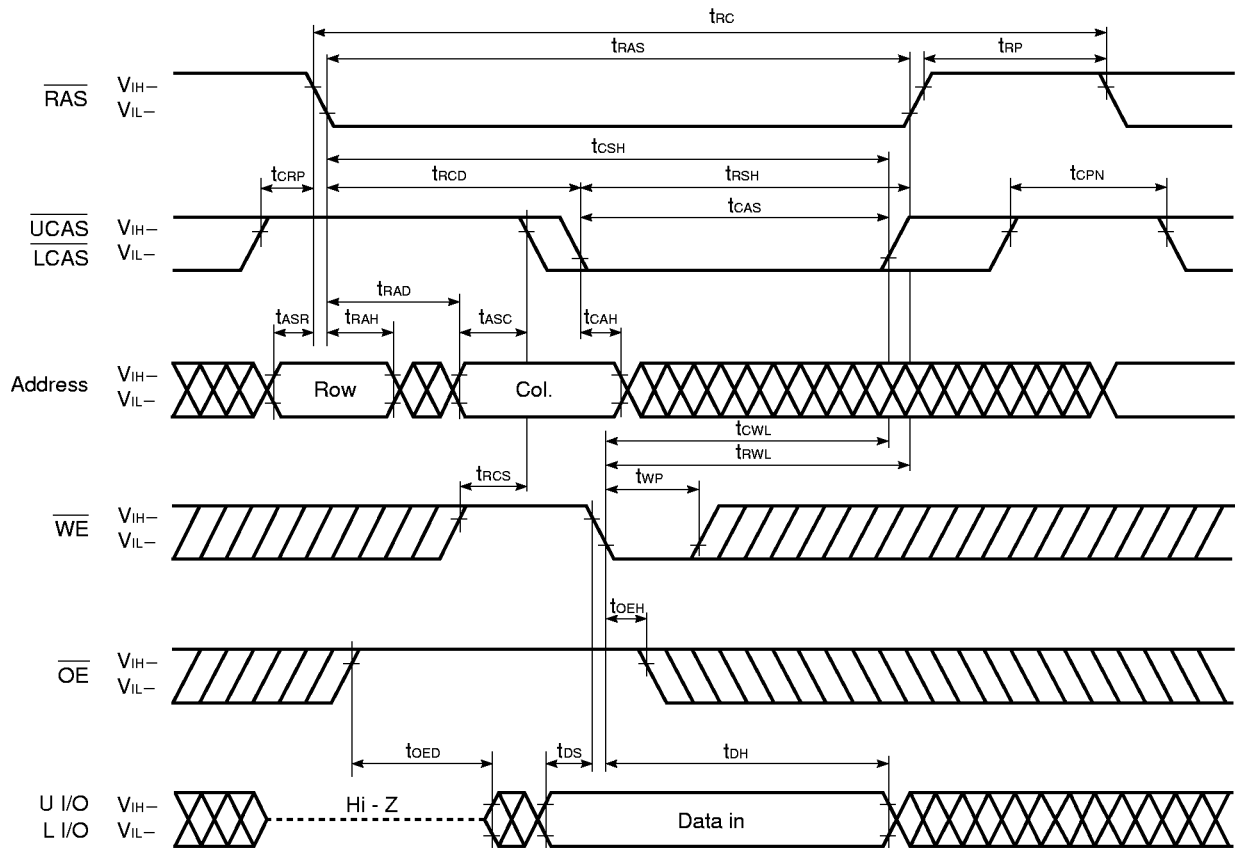
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

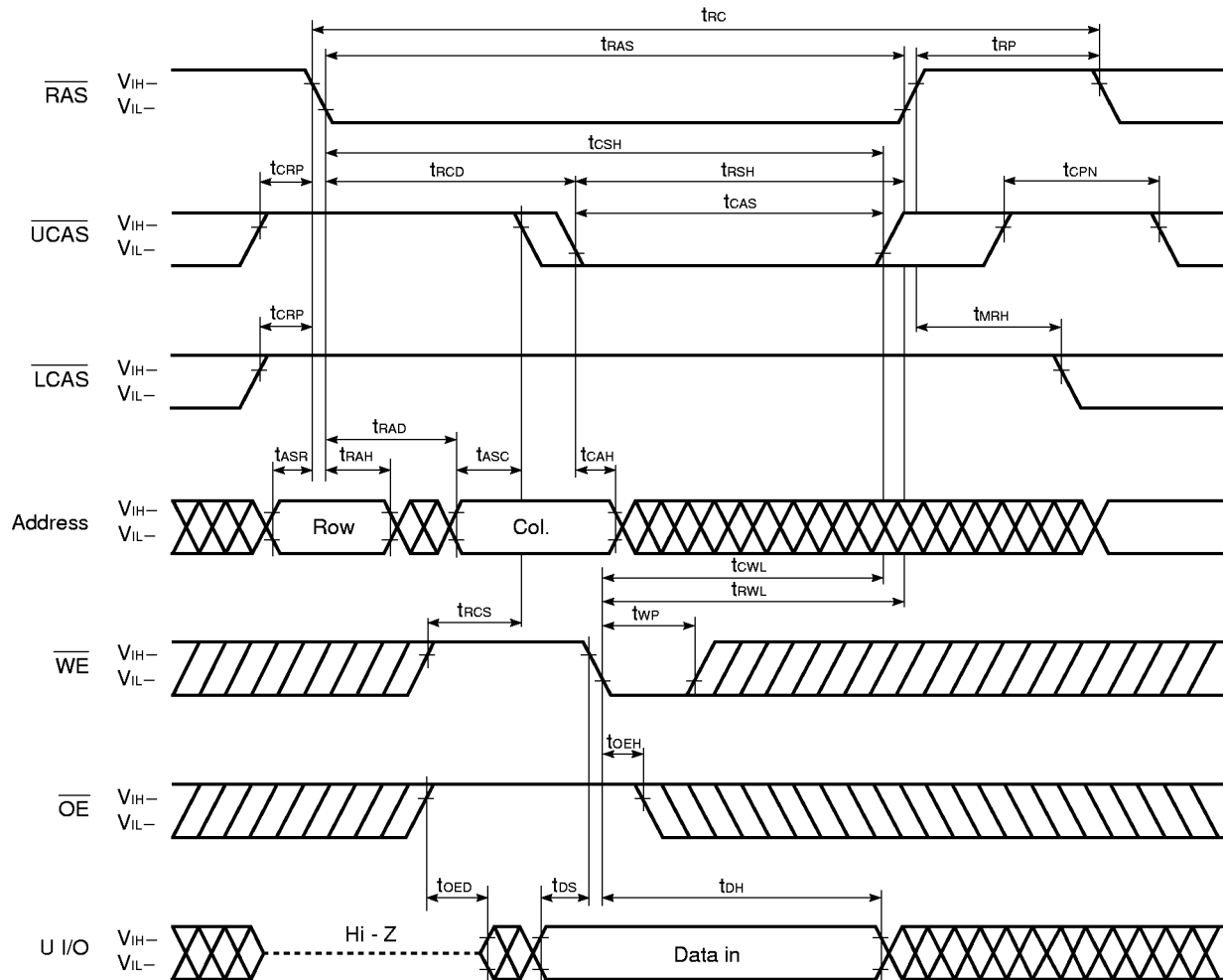


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

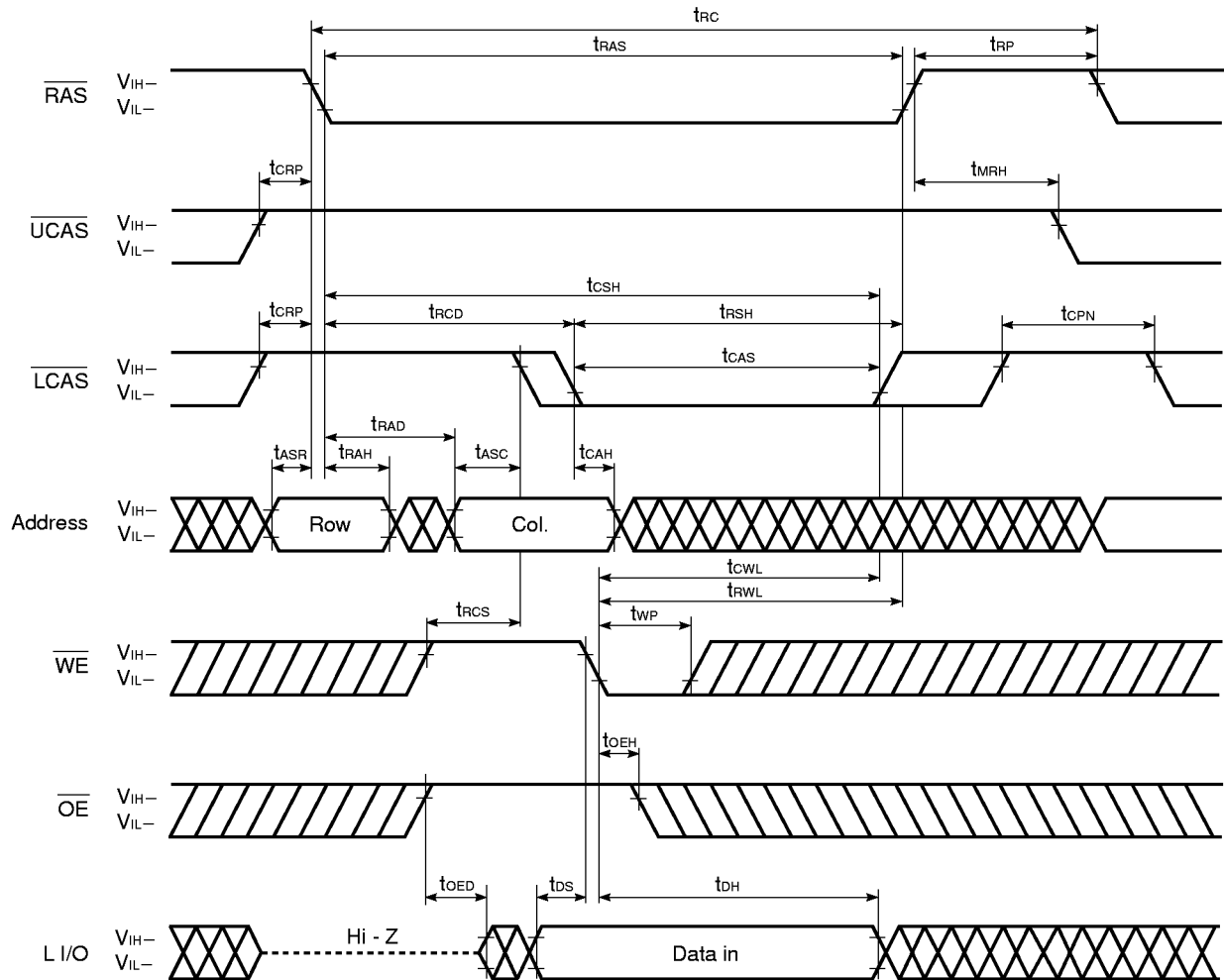


Upper Byte Late Write Cycle



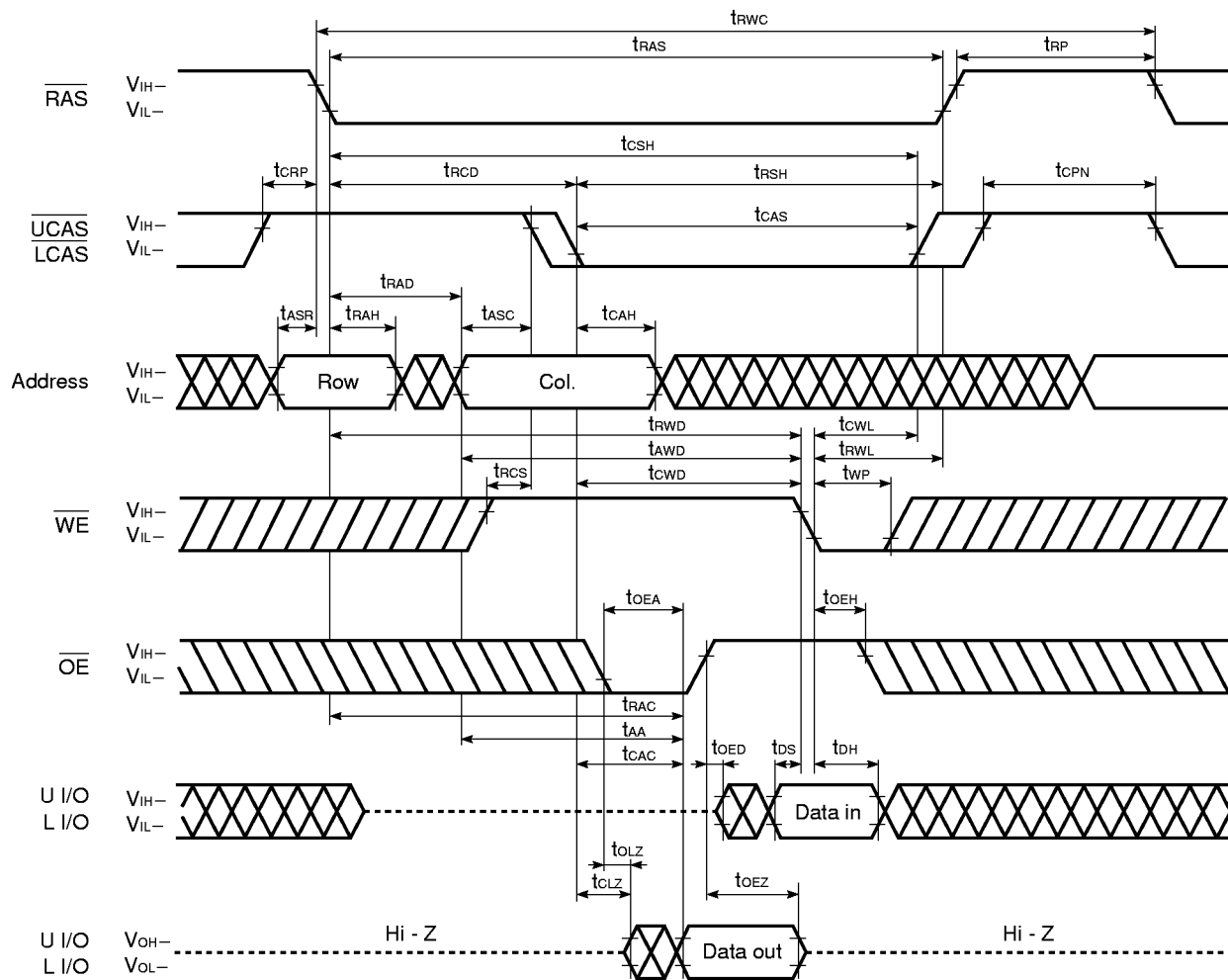
Remark L I/O: Don't care

Lower Byte Late Write Cycle

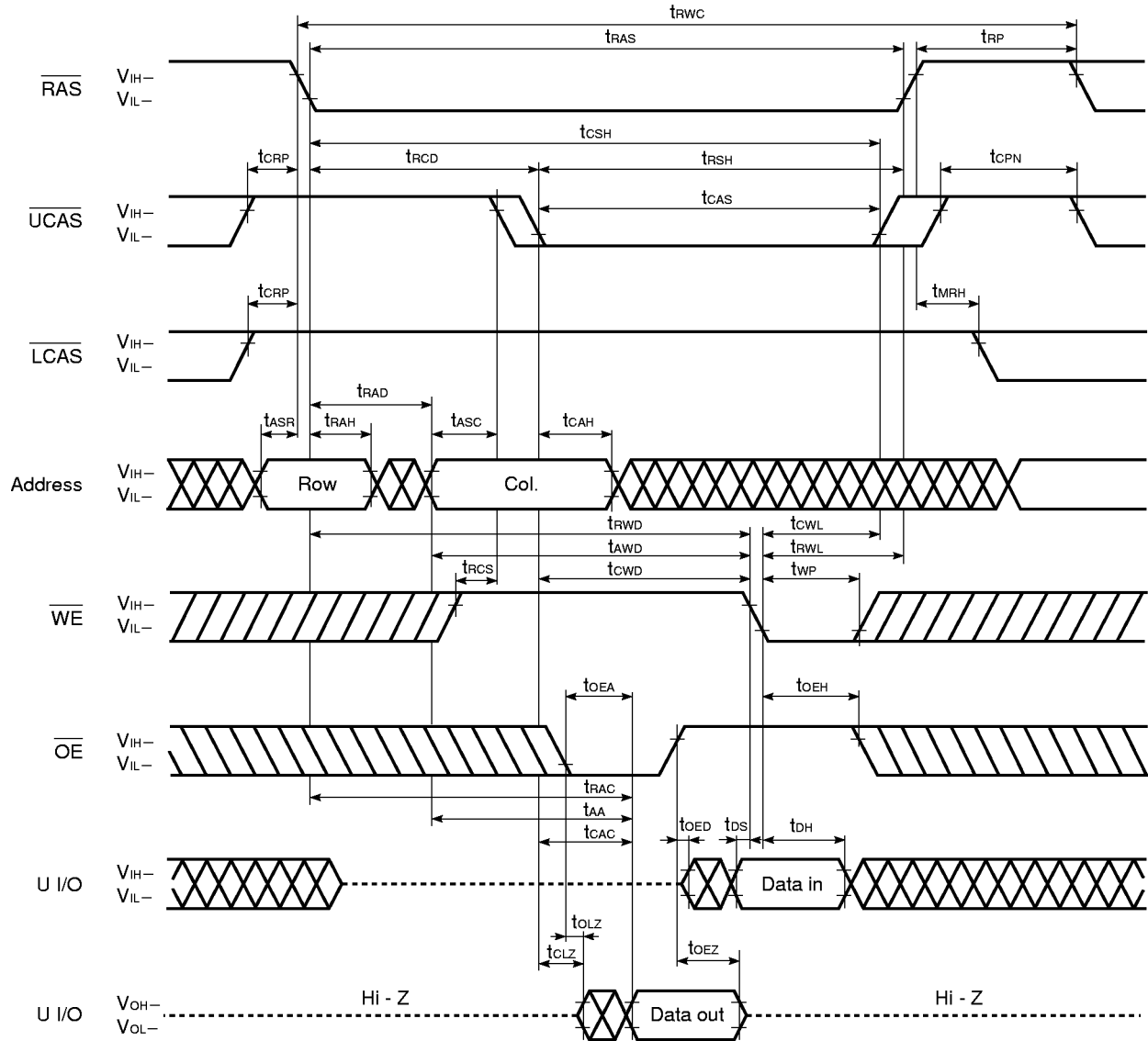


Remark U I/O: Don't care

Read Modify Write Cycle



Upper Byte Read Modify Write Cycle



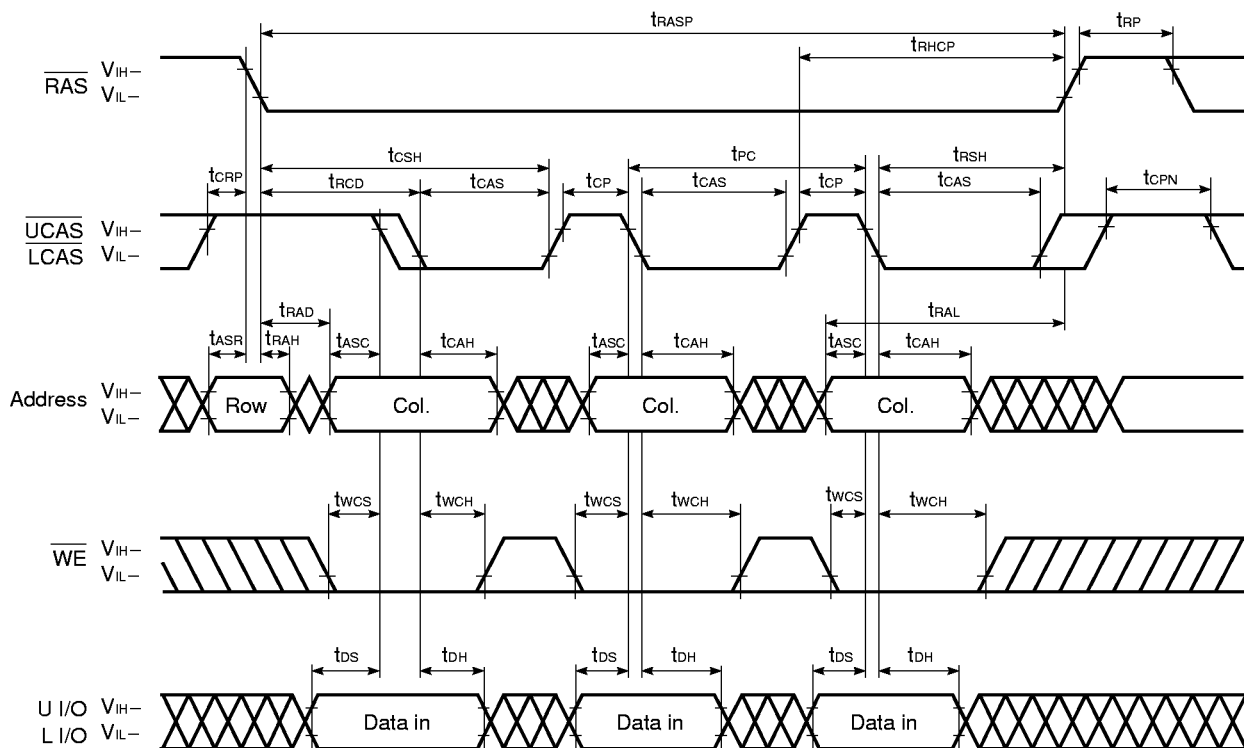
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

[illegible]

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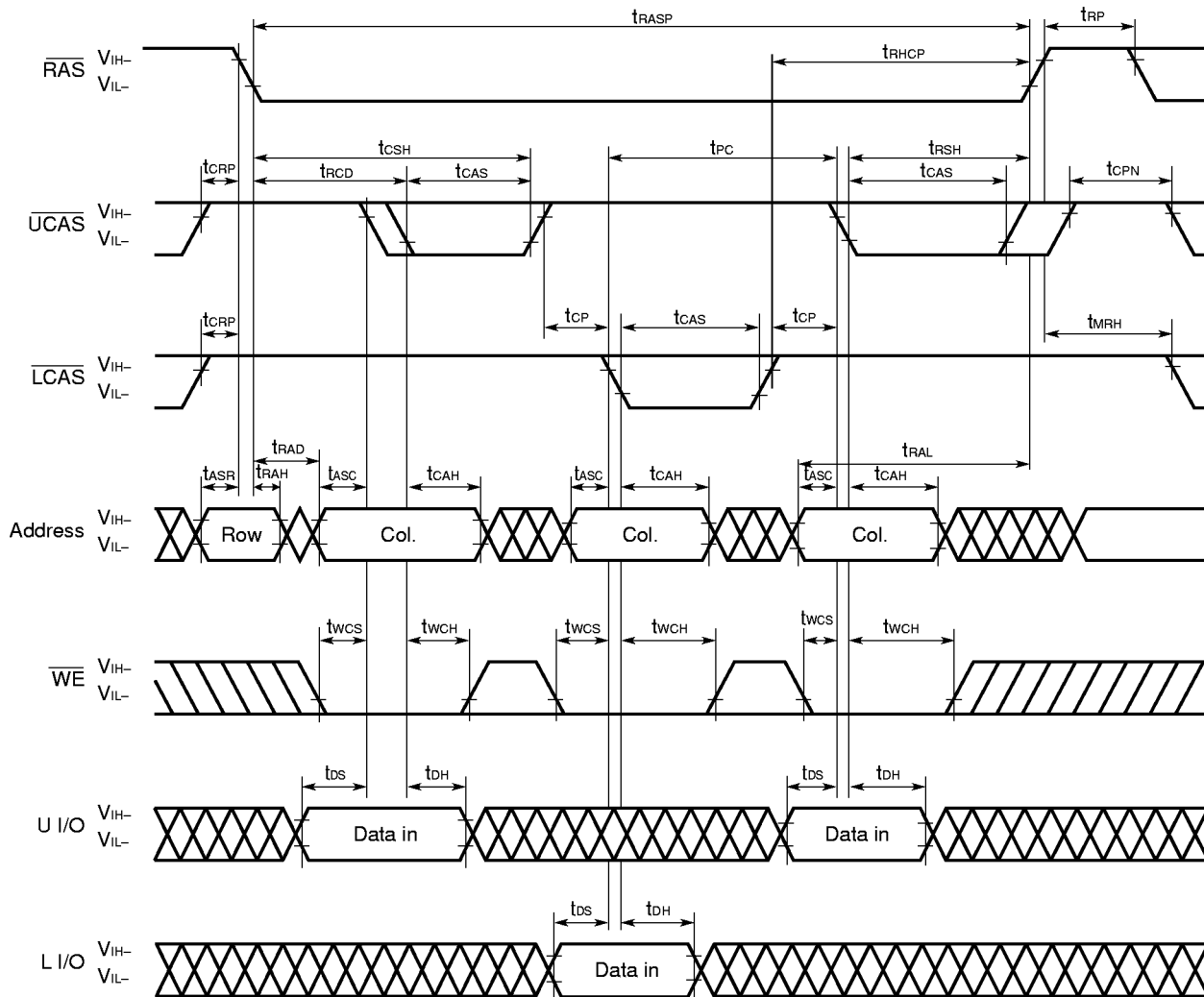
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Byte Early Write Cycle



Remarks

1. $\overline{\text{OE}}$: Don't care
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
3. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

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The diagram illustrates the timing relationships for a 256K16 DRAM. The signals and their timing parameters are as follows:

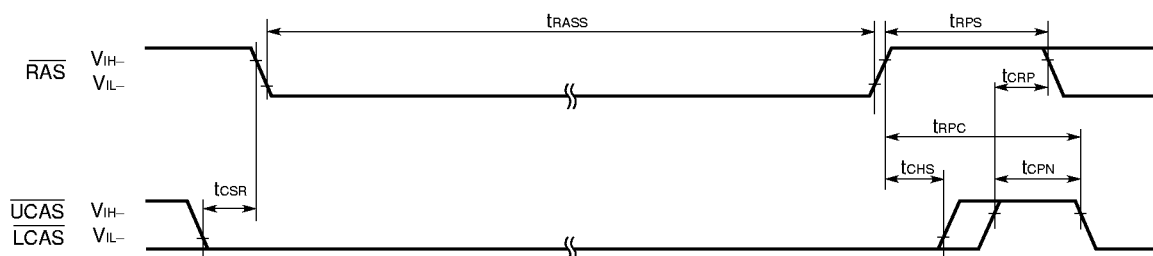
- RAS:** $\overline{\text{RAS}}$ signal with parameters t_{RASP} , t_{RHCP} , and t_{RP} .
- UCAS:** $\overline{\text{UCAS}}$ signal with parameters t_{CRP} , t_{RCD} , t_{CSH} , t_{CAS} , t_{PC} , t_{ASH} , t_{CAS} , and t_{CPN} .
- LCAS:** $\overline{\text{LCAS}}$ signal with parameters t_{CRP} , t_{CP} , t_{CAS} , t_{CP} , and t_{MRH} .
- Address:** Shows Row and Column address cycles with parameters t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , t_{ASC} , t_{CAH} , t_{ASC} , t_{CAH} , and t_{RAL} .
- WE:** $\overline{\text{WE}}$ signal with parameters t_{RCS} , t_{CWL} , t_{WP} , t_{RCS} , t_{CWL} , t_{WP} , t_{RCS} , t_{CWL} , t_{RWL} , and t_{WP} .
- OE:** $\overline{\text{OE}}$ signal with parameters t_{OEH} .
- U I/O:** Data input/output with parameters t_{OED} , t_{DS} , and t_{DH} .
- L I/O:** Data input/output with parameters t_{OED} , t_{DS} , and t_{DH} .

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[illegible]

- Remarks**
1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.
 2. This cycle can be used to control either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ only. Or, it can be used to control $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ simultaneously, or at random.

★ **CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16160L, 42S18160L)**



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16160L: 4,096 times within a 64 ms interval

μ PD42S18160L: 1,024 times within a 16 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16160L: 4,096 times within a 64 ms interval

μ PD42S18160L: 1,024 times within a 16 ms interval

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied.

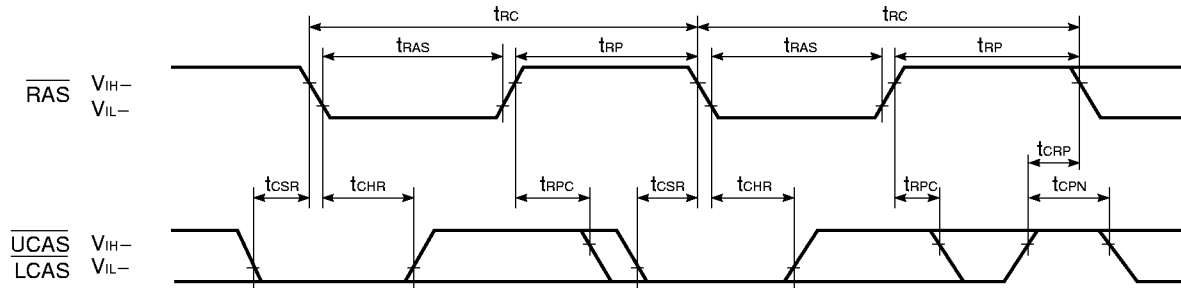
And refresh cycles as follows should be met.

μ PD42S16160L: 4,096 times within a 128 ms interval

μ PD42S18160L: 1,024 times within a 128 ms interval

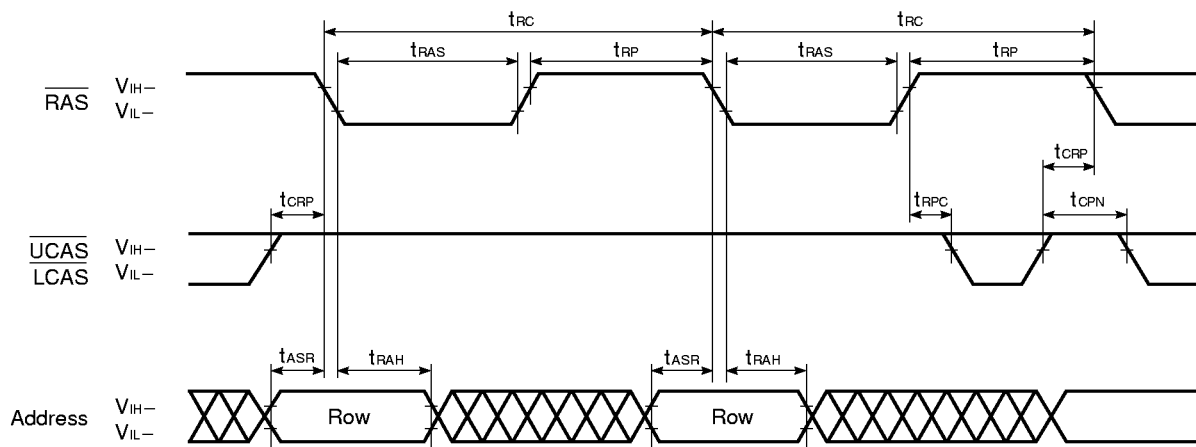
For details, please refer to **How to use DRAM** User's Manual.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



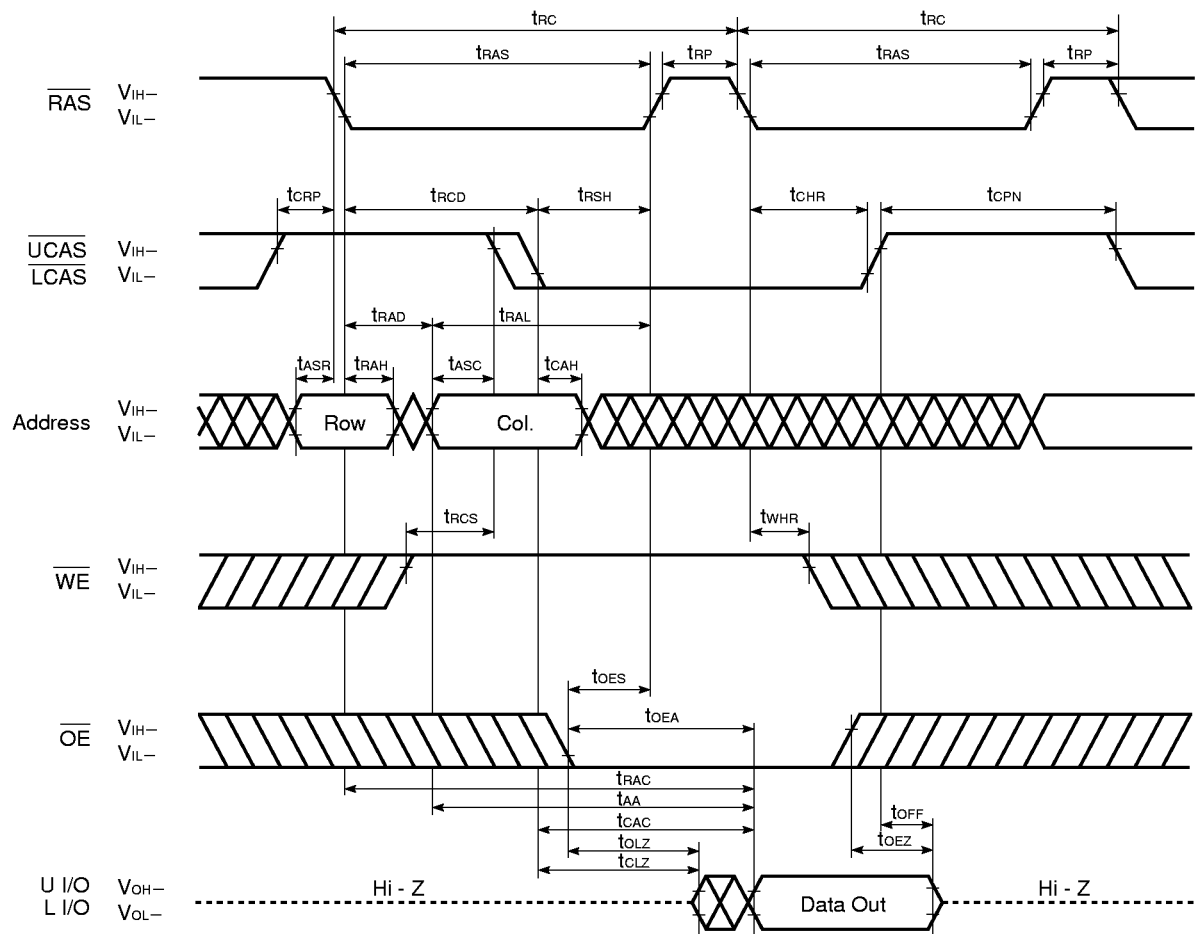
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

$\overline{\text{RAS}}$ Only Refresh Cycle

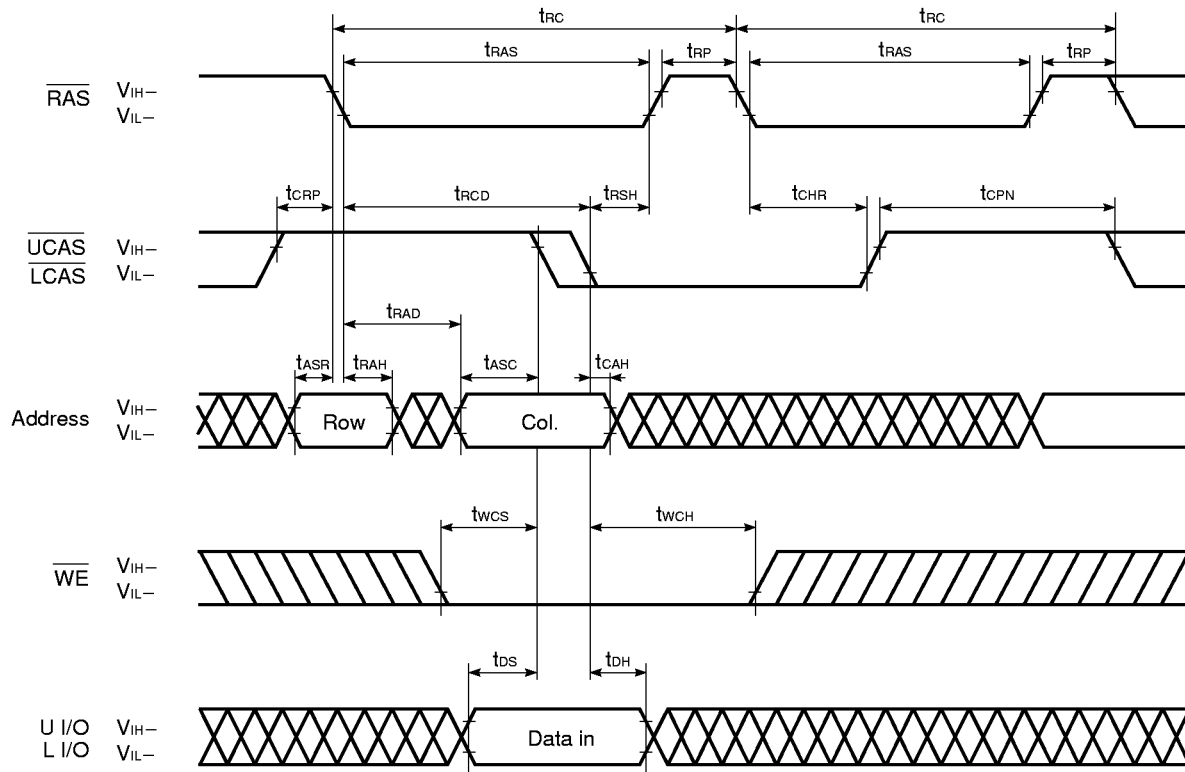


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



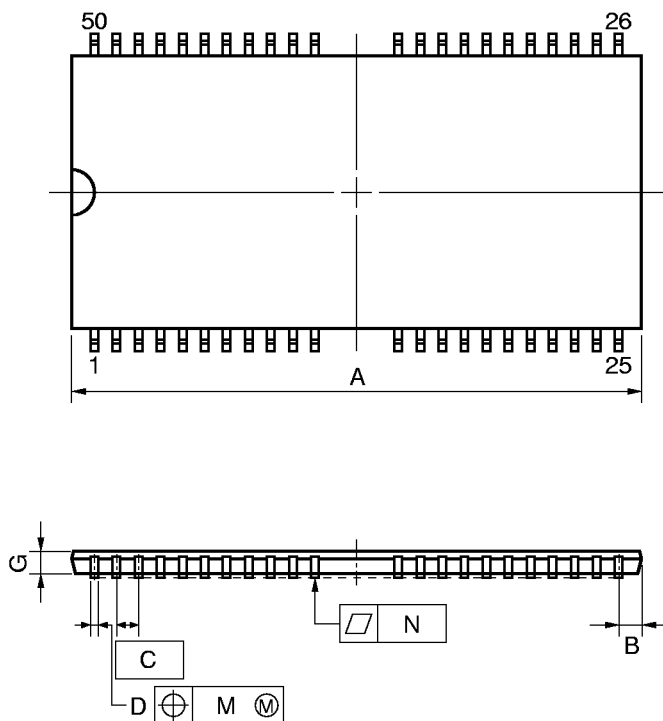
Hidden Refresh Cycle (Write)



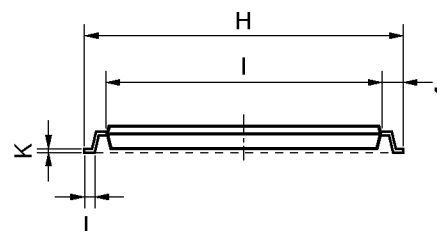
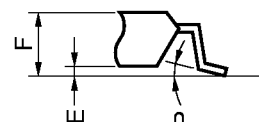
Remark $\overline{\text{OE}}$: Don't care

Package Drawings

50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end



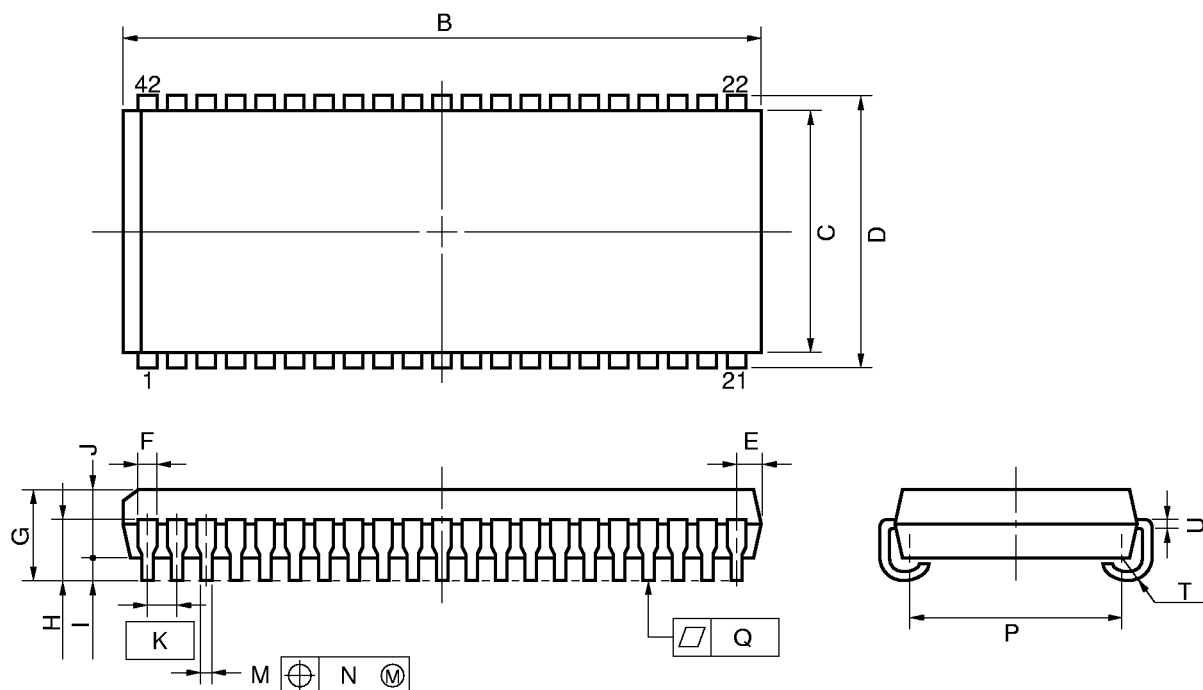
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.32 ^{+0.08} _{-0.07}	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145 ^{+0.025} _{-0.015}	0.006±0.001
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.13	0.005
N	0.10	0.004
P	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P42LE-400A

ITEM	MILLIMETERS	INCHES
B	27.56 ^{+0.2} _{-0.35}	1.085 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	0.043 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

★ Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μ PD42S16160L, 4216160L, 42S18160L, 4218160L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μ PD42S16160LG5-7JF, 4216160LG5-7JF, 42S18160LG5-7JF, 4218160LG5-7JF: 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	IR35-107-3
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards)	VP15-107-3
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μ PD42S16160LLE, 4216160LLE, 42S18160LLE, 4218160LLE: 42-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards)	IR35-207-3
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards)	VP15-207-3
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.