OXFORD SEMICONDUCTOR

Data Sheet

OXU210HP
USB2.0 High-Speed Host, Peripheral and OTG Controller

Features

- High-performance, high-speed USB dual-role (host/peripheral) controller
- Compatible with the *Universal Serial Bus Specification, Revision 2.0* for high-speed (480 Mb/s), full-speed (12 Mb/s), and low-speed (1.5 Mb/s) operations
- High-speed optimized host controller with transaction translator for complete backward compatibility with full-speed and low-speed products
- Two high-speed USB ports; one port remains host while the other can be configured as peripheral, host, or OTG (dual role)
- Simultaneous operation of both ports
- Processor interface is either 16 bits (BGA) or configurable 16 or 32 bits (LQFP)
- Fast microprocessor access cycle and double/multi buffering support for USB transfers
- Host interface contains support for common SoC DMA modes including bursting and slave request/acknowledge protocols
- Complete host, peripheral and OTG software solutions for popular microprocessors using many of the most popular operating systems
- Advanced power management controls chip clocking and PHY function for very low power consumption
- Integrated on-chip V_{BUS} voltage comparator and 100 mA charge pump
- 72 Kbytes of single-port SRAM provides space for data structures and buffer space for transfer data
- True transfer level operation, with transaction scheduling and handling (data sequence toggle, error retry, etc.), implemented in hardware
- Integrated PLL runs from a single 12-MHz crystal or an external 12-MHz clock source

- Packaging
  - 7×7 mm BGA, 84-ball, RoHS compliant
  - 14×14 mm LQFP, 128-pin, RoHS compliant
- Operating temperature range: -40° to 85° C

Device Overview

The Oxford Semiconductor OXU210HP is a single-chip, high-speed USB host and high-speed USB peripheral controller with integrated transceivers. It is the fourth controller in the family of integrated low-cost, high-performance, OTG controllers that have been specifically designed for embedded systems.

The OXU210HP operates at up to 480 Mb/s, using a compatible EHCI-based core. It also includes an integrated transaction translator that supports full-speed (12 Mb/s) and low-speed (1.5 Mb/s) USB peripherals.

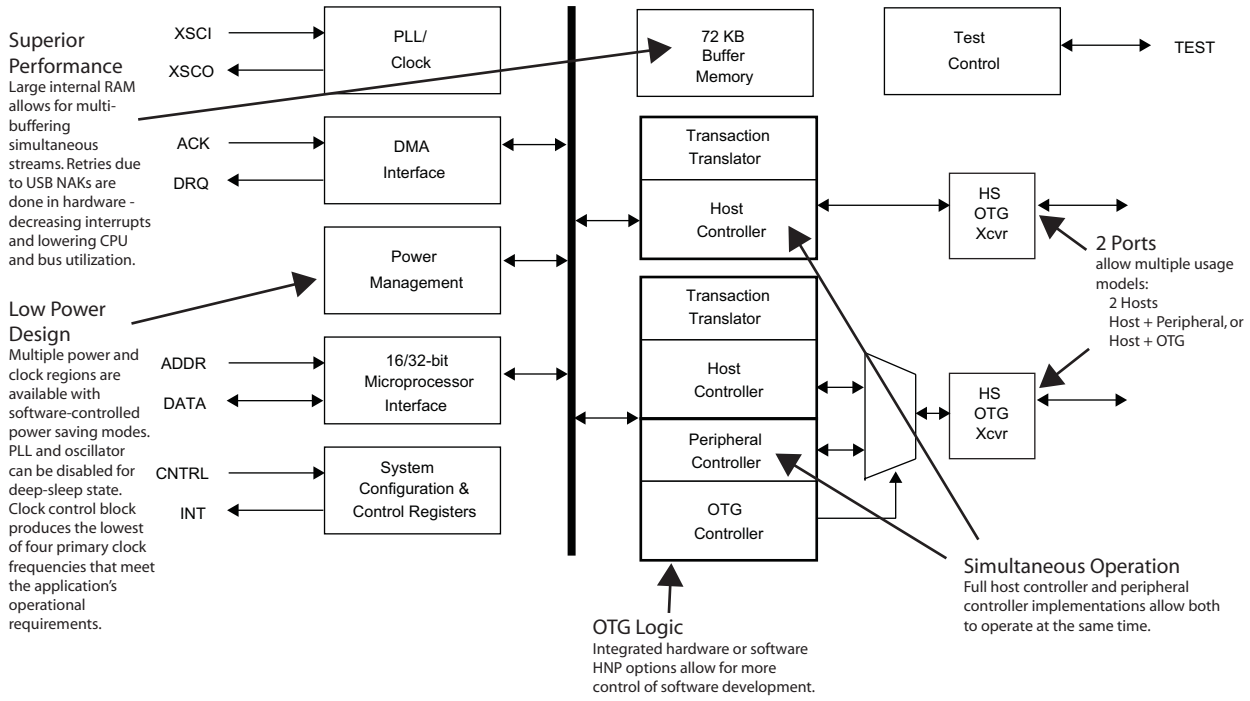
The selectable 16- and 32-bit processor interface is compatible with a variety of CPUs. A large 72-Kbyte buffer has also been integrated to reduce interrupts and minimize CPU overhead.

The OXU210HP supports all USB transfer modes (control, interrupt, bulk and isochronous) and is supported with USB device drivers and the Oxford Semiconductor USBLink product suite. The USBLink host, peripheral and OTG stacks have been ported to a wide variety of real time operating systems including VxWorks®, ThreadX®, and Nucleus®.

In addition, Oxford Semiconductor also makes available low-level controller drivers for other native USB stacks such as those included with Windows® CE and Linux® 2.6.x.

Figure 1 shows the OXU210HP block diagram.

Figure 1 OXU210HP Block Diagram



Sample Applications

- Digital televisions
- Home media centers
- Portable media centers
- Digital video cameras
- Digital still cameras
- Printers
- MP3 players
- External storage products
- Set-Top Boxes (STB)
- Personal Video Recorders (PVR)
- Personal Digital Assistants (PDA)
- 3G mobile phones
- DVD recorders

Development Support

The OXU210HP product suite includes the USB controller as well as the protocol stacks and the driver software that enable a wide variety of USB applications. This unique ability to deliver a total hardware and software solution sets Oxford Semiconductor apart from other semiconductor companies and benefits customers by:

- Shortening time to market
- Reducing risk
- Offering a single source for hardware and software, thereby reducing the number of suppliers the customer has to deal with

Oxford Semiconductor is a Microsoft® Windows® Embedded Partner and has developed host and peripheral controller drivers for Windows CE 5.0. Similar software support is also available for Linux® 2.6.x.

For customers using an RTOS such as VxWorks®, ThreadX®, Nucleus®, OSE, LynxOS®, and AMX™, among others, Oxford Semiconductor offers its USBLink™ host, peripheral and On-The-Go software solutions.

The USBLink Product Suite is a modularized approach to providing USB connectivity for a wide variety of embedded products. Due to its flexible architecture and broad based support for USB host, peripheral and OTG applications, Oxford Semiconductor can tailor the USBLink software deliverables to meet each customer's USB requirements.

The USBLink solutions are configurable and can support systems with:

- Big or little endian processors
- DMA or non-DMA USB controllers
- A wide variety of USB controllers, including the OXU210HP
- Complex to simple operating systems

Oxford Semiconductor has over eight years of experience developing embedded USB technology. Its USBLink software has been ported to twenty different operating systems and a wide variety of embedded architectures. USBLink is shipping in many millions of units.

Electrical Characteristics

Table 1 to Table 10 detail the required operating conditions for the device and the DC and AC electrical characteristics.

Table 1 Absolute Maximum Device Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{PWM3}, V_{DD3IO}	3.3 V digital power supply		-0.3	4.0	V
$V_{DD3.3A}$	3.3 V analog power supply		-0.3	4.0	V
$V_{DD1.8}$	1.8 V power supply		-0.3	2.16	V
V_{IO}	1.65 V to 3.3 V power supply		-0.3	4.0	V
V_I	DC input voltage		-0.3	4.0	V
T_S	Storage temperature		-40	+150	°C

Note: 1 Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the normal operating conditions specified in the following section. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
V_{PWM3}, V_{DD3IO}	3.3 V digital power supply		3.0	3.6	V
$V_{DD3.3A}$	3.3 V analog power supply		3.0	3.6	V
$V_{DD1.8}$	1.8 V power supply		1.62	1.98	V
V_{IO}	1.65 - 3.3 V wide-range I/O power supply		1.65	3.6	V
$V_{I3.3}$	DC input voltage of 3.3 V pins		0	3.6	V
V_{IW}	DC input voltage of wide-range pins		0	V_{IO} + 0.3	V
T_O	Operating temperature		-40	+85	°C

Table 3 DC Characteristics, Full-Speed USB I/O Signals: DP_HOST, DM_HOST, DP_OTG, DM_OTG

Symbol	Parameter	Condition	Min	Max	Unit
V_{DI}	Diff. input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	--	V
V_{CM}	Diff. comm. mode range		0.8	2.5	V
V_{OL}	Static output low		--	0.3	V
V_{OH}	Static output high		2.8	3.6	V
V_{CRS}	Output signal crossover		1.3	2.0	V
C_{IN}	Input capacitance			20	pF

Table 4 DC Characteristics, High-Speed USB I/O Signals: DP_HOST, DM_HOST, DP_OTG, DM_OTG					
Symbol	Parameter	Condition	Min	Max	Unit
V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	300	--	mV
V_{HSCM}	High-speed data signaling common mode range		-50	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch detected	--	100	mV
		No squelch detected	150	--	mV
V_{HSOI}	High-speed idle output voltage (differential)		-10	10	mV
V_{HSOL}	High speed low level output voltage (differential)		-10	10	mV
V_{HSOH}	High speed high level output voltage (differential)		-360	400	mV
V_{CHIRPJ}	Chirp-J output voltage (differential)		700	1100	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900	-500	mV

Table 5 DC Characteristics, Logic Signals					
Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Low level output voltage		--	0.4	V
V_{OH}	High level output voltage	V_{IO} = 3.3 V	2.4	--	V
		V_{IO} = 2.5 V	1.85	--	V
		V_{IO} = 1.8 V	0.75 * V_{IO}		
V_{IL}	Low level input voltage	V_{IO} = 3.3 V	--	0.8	V
		V_{IO} = 2.5 V	--	0.25 * V_{IO}	V
		V_{IO} = 1.8 V	0.3 * V_{IO}	--	
V_{IH}	High level input voltage	V_{IO} = 3.3 V	2.0	--	V
		V_{IO} = 2.5 V	0.625 * V_{IO}	--	V
		V_{IO} = 1.8 V	0.7 * V_{IO}	--	
C_{IN}	Input capacitance		2.2 (typical)		pF
C_{OUT}	Output capacitance		2.2 (typical)		pF
C_{BI}	Bi-directional capacitance		2.2 (typical)		pF
I_{IN}	Input leakage current	No pull up or pull down	-10	10	µA

Note: 1 The charge pump supply $V_{CPSUPPLY}$ supplies the external components of the charge pump circuit. This is not a pin on the chip.

Table 6 DC Characteristics, ID Resistance					
Symbol	Parameter	Condition	Min	Max	Unit
$R_{B-PLUG-ID}$	Resistance to ground on Mini-B plug		100 K	--	Ω
$R_{A-PLUG-ID}$	Resistance to ground on Mini-B plug		--	10	Ω

Table 7 DC Characteristics, Charge Pump					
Symbol	Parameter	Condition	Min	Max	Unit
CV_{out}	Output voltage	Driving current <= 100 mA	4.75	5.07	V
CI_{drive}	Driving current	$V_{CPSUPPLY}$ = 3.3 V Output voltage = 5 V	--	100	mA
Ct_{st}	Start-up time when enabled	$V_{CPSUPPLY}$ = 3.3 V RV_{out} = 4.5 V (90%)	400 (typical)		µs

Table 8 AC Characteristics, DP_HOST, DM_HOST, DP_OTG, DM_OTG Driver Characteristics (High Speed)					
Symbol	Parameter	Condition	Min	Max	Unit
t_{HSRt}	High speed differential rise time		500	--	ps
t_{HSF}	High speed differential fall time		500	--	ps
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip	40.5	49.5	Ω

Table 9 AC Characteristics, DP_HOST, DM_HOST, DP_OTG, DM_OTG Driver Characteristics (Full Speed)					
Symbol	Parameter	Condition	Min	Max	Unit
t_{FR}	Rise time	C_L = 50 pF	4	20	ns
t_{FF}	Fall time	C_L = 50 pF	4	20	ns
t_{FRFM}	T_R/T_F matching		90	110	%
Z_{DRV}	Driver output resistance	Steady state drive with external 33 Ω series resistor	3	9	Ω

Table 10 AC Characteristics, DP_HOST, DM_HOST, DP_OTG, DM_OTG Driver Characteristics (Low Speed)					
Symbol	Parameter	Condition	Min	Max	Unit
t_{LR}	Rise time	C_L = 200 - 600 pF	75	300	ns
t_{FF}	Fall time	C_L = 200 - 600 pF	75	300	ns
t_{FRFM}	T_R/T_F matching		80	125	%

Power Consumption

Table 11 gives the power consumption figures for the OXU210HP.

Table 11 OXU210HP Power Consumption

Mode	3.3 V (mA)	1.8 V (mA)	Power (mW)
Full-power down	0.06	0.2	0.56
Power down, remote wakeup enabled (PHY PLL enabled during power down)	0.66	0.24	2.61
Idle but clocking @ 120 MHz (port suspend)	23	56	177
FS bulk in/out transfers @ OTG port, peak current (120 MHz), SPH idle	33	60	217
FS transmit of test packet, both ports (60 MHz)	25	35	146
HS bulk in/out transfers @ OTG port, peak current (120 MHz), SPH idle	61	70	327
HS transmit of test packet, OTG port only (120 MHz)	56	59	291
HS transmit of test packet, both ports (120 MHz)	91	59	407

The above measurements are at typical process corner and room temperature and do not account for process and temperature variations. Bulk transfer current measurements are made at the peak of each transfer. Actual average current in customer application will be lower. Transmit of test packet measurements are taken in test mode and represent maximum switching on the bus.

Pin Layout

The device is supplied as a 128-pin LQFP package and as an 84-ball BGA package. Figure 2 shows the chip layout of the 128-pin LQFP package. Figure 3 shows the chip layout of the 84-ball BGA package.

Figure 2 OXU210HP 128-Pin LQFP Package (Top View)

Table 12 lists the LQFP pin allocations.

*Table 12 OXU210HP **128-Pin LQFP** Pin Allocations (Sheet 1 of 2)*

Pin	No. Bits	Type(1)	Name	Description
Processor Interface (61 pins)				
14, 15, 16, 17, 19, 20, 21, 22, 23, 24, 25, 26, 30, 31, 32, 33	16	MSBCT	D_0 - D_{15}	16-bit data bus
2, 3, 4, 5, 8, 9, 10, 11, 34, 35, 36, 37, 38, 39, 40, 41	16	MSBCT	D_{16} - D_{31}	Additional 16-bits of data bus for optional 32-bit mode. In 16-bit mode, these signals have an internal pull down
106, 107, 108, 109, 110, 111, 112, 113, 116, 117, 118, 119, 120, 123, 124, 125	16	MSI	A_1 - A_{16}	Address bus for direct address space of 72 Kbytes plus memory mapped registers
127	1	MSIU	/WR	Write strobe
1	1	MSIU	/RD	Read strobe
126	1	MSIU	/CS	Chip select
83	1	MOCT	/INT	Interrupt to the MCU.This pin can be software configured as a driven output or WO. WO is the default
84	1	I	/RESET	Hardware reset
90, 91	2	MOCT	DRQ_1, DRQ_0	DMA request outputs to support two channels
92, 93	2	SI	ACK_1, ACK_0	DMA acknowledge
42, 43	2	MSI	BE_0, BE_1	Byte enables
44, 45	2	MSID	BE_2, BE_3	Byte enables. These signals have an internal pull down.
General Purpose I/O (4 pins)				
96, 97, 98, 99	4	BC	$GPIO_0$ - $GPIO_3$	General purpose I/O
Power and Ground (38 pins)				
7, 13, 28, 29, 55, 56, 79, 82, 95, 105, 115, 122, 128	13		V_{SS}	Digital ground
46, 51, 60, 65, 68, 73	6		V_{SSA}	Analog ground
18, 53, 54, 81, 114	5		$V_{DD1.8}$	1.8 V core power. VREGOUT may be used for the supplies
47, 52, 59, 64, 72	5		$V_{DD3.3A}$	Analog +3.3 V power
6, 12, 27, 80, 94, 104, 121	7		V_{IO}	Wide-range I/O voltage. If using +1.8 V, VREGOUT may be used for the supplies
74	1		V_{DD3IO}	Digital +3.3 V power

*Table 12 OXU210HP **128-Pin LQFP** Pin Allocations (Sheet 2 of 2)*

Pin	No. Bits	Type[(1)]	Name	Description
67	1		V_{PWM3}	Analog 3.3 V power for the charge pump Pulse Width Modulator (PWM)
USB Interface (9 pins)				
48, 49	2	B	DP_HOST, DM_HOST	Data lines for host port. If not used, these pins should be left floating
62, 63	2	B	DP_OTG, DM_OTG	Data lines for OTG port. If not used, these pins should be left floating
71	1	5I	V_{BUS}	V_{BUS} input used by the voltage comparators of the OTG port for connection. This pin should be left floating in a host-only application
75	1	P5O	/EXVBO	Turn on/off the external V_{BUS} (5 V) for OTG operation (1:V_{BUS} off, 0: V_{BUS} on) when using the external V_{BUS} source
76	1	P5IU	/OC	Over current condition indicator for powered host ports
77	1	P5IU	ID	Connected to the ID pin of the mini-AB connector for OTG applications. With the help of an internal pull-up resistor, this pin determines the chip's responsibility in an OTG application (0: A-device, 1:B-device)
78	1	P5OT	/PO	Turn on/off gang power for all host ports
Clock Interface (2 pins)				
57	1	I	XSCI	Input. A 12 MHz passive crystal should be connected across the two pins (XSCI and XSCO). Optionally, a 12 MHz oscillator can be sourced through XSCI while keeping XSCO unconnected
58	1	O	XSCO	Output
Internal V_{BUS} Charge Pump (3 pins)				
69	1	O	PD_PMOS	Internal charge pump output for P-MOSFET (optional switch on the V_{OUT})
66	1	O	EXT	Internal charge pump output for N-MOSFET
70	1	I	V_{OUT}	Internal charge pump output voltage feedback pin
Test (9 pins)				
85, 86, 87, 88, 100, 101, 102, 103	8	OC	$DEBUG_0$ - $DEBUG_7$	Debug outputs
89	1	I	TEST	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation
Miscellaneous (2 pins)				
50	1	B	REF_HOST	Connect external reference resistor (12 KW +/- 1%) to V_{SSA}. One per port
61	1	B	REF_OTG	

Note to Table 12: 1 Type key: format is [(L)(W_)X(Y)(_Z(T))] where the following conventions apply:

L—Logic Level		W—Tolerance		X—Type		Y—Pull		Z—Drive	T—Tristate	
P[2]	OD 3.3 CMOS	5	5 V	I	Input	U	Pull up	C[4]	T	Tristate
M[3]	Multi-voltage: 3.3 V CMOS 2.5 V CMOS 1.8 V CMOS		3.3 V	O	Output	D	Pull down			Normal
S	Schmitt Trigger			B	Bidirectional		None			

2 Program to OD or 3.3 V CMOS via the ASO register (0x0068).
3 Program to 3.3, 2.5, or 1.8 V by setting the V_{IO} voltage level.
4 Program to 2 mA, 4 mA, 6 mA, or 8 mA via the I/O Control register (0x006C).

Figure 3 OXU210HP 84-Ball BGA Package (Top View)

	1	2	3	4	5	6	7	8	9	10
A	/CS	A_{15}	A_{13}	A_{11}	A_{10}	A_7	A_6	A_4	A_2	ACK_0
B	/RD	/WR	A_{14}	A_{12}	A_9	A_8	A_5	A_3	$GPIO_0$	DRQ_0
C	D_0	A_{16}	V_{SS}	V_{IO}	V_{SS}	$V_{DD1.8}$	V_{SS}	$V_{DD1.8}$	A_1	TEST
D	D_1	D_2	V_{SS}					V_{IO}	/INT	/RESET
E	D_3	D_4	$V_{DD1.8}$					V_{SS}	ID	/PO
F	D_6	D_5	D_7					V_{SSA}	/EXVBO	/OC
G	D_8	D_9	V_{SS}					$V_{DD3.3A}$	V_{BUS}	V_{OUT}
H	D_{11}	D_{10}	V_{SSA}	$V_{DD3.3A}$	$V_{DD3.3A}$	$V_{DD3.3A}$	V_{SSA}	V_{SSA}	V_{PWM3}	PD_PMOS
J	D_{13}	D_{12}	BE_1	BE_0	V_{SSA}	V_{DD3IO}	V_{IO}	$V_{DD3.3A}$	V_{SSA}	EXT
K	D_{15}	D_{14}	DM_HOST	DP_HOST	REF_HOST	XSCI	XSCO	DM_OTG	DP_OTG	REF_OTG

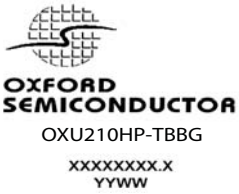


Table 13 lists the BGA pin allocations.

Table 13 OXU210HP 84-Ball BGA Pin Allocations (Sheet 1 of 2)

Pin	No. Bits	Type(1)	Name	Description
Processor Interface (41 pins)				
C1, D1, D2, E1, E2, F2, F1, F3, G1, G2, H2, H1, J2, J1, K2, K1	16	MSBCT	D_0 - D_{15}	16-bit data bus
C9, A9, B8, A8, B7, A7, A6, B6, B5, A5, A4, B4, A3, B3, A2, C2	16	MSI	A_1 - A_{16}	Address bus for direct address space of 72 Kbytes plus memory mapped registers
B2	1	MSIU	/WR	Write strobe
B1	1	MSIU	/RD	Read strobe
A1	1	MSIU	/CS	Chip select
D9	1	MOCT	/INT	Interrupt to the MCU.This pin can be software configured as a driven output or WO. WO is the default
D10	1	I	/RESET	Hardware reset
B10	1	MOT	DRQ_0	DMA request outputs to support two channels
A10	1	SI	ACK_0	DMA acknowledge
J4, J3	2	MSI	BE_0, BE_1	Byte enables
General Purpose I/O (1 pin)				
B9	1	B	$GPIO_0$	General purpose I/O
Power and Ground (25 pins)				
C3, C5, C7, D3, E8, G3	6		V_{SS}	Digital ground
F8, H3, H7, H8, J5, J9	6		V_{SSA}	Analog ground
C6, C8, E3	3		$V_{DD1.8}$	1.8 V core power. VREGOUT may be used for the supplies
G8, H4, H5, H6, J8	5		$V_{DD3.3A}$	Analog +3.3 V power
C4, D8, J7	3		V_{IO}	Wide-range I/O voltage. If using +1.8 V, VREGOUT may be used for the supplies
J6	1		V_{DD3IO}	Digital +3.3 V power
H9	1		V_{PWM3}	Analog 3.3 V power for the charge pump Pulse Width Modulator (PWM)
USB Interface (9 pins)				
K4, K3	2	B	DP_HOST, DM_HOST	Data lines for host port. If not used, these pins should be left floating
K8, K9	2	B	DM_OTG, DP_OTG	Data lines for OTG port. If not used, these pins should be left floating.
G9	1	5I	V_{BUS}	V_{BUS} input used by the voltage comparators of the OTG port for connection. This pin should be left floating in a host only application

Table 13 OXU210HP 84-Ball BGA Pin Allocations (Sheet 2 of 2)

Pin	No. Bits	Type(1)	Name	Description
F9	1	P5O	/EXVBO	Turn on/off the external V_{BUS} (5 V) for OTG operation (1:V_{BUS} off, 0:V_{BUS} on) when using the external charge pump
F10	1	P5IU	/OC	Over current condition indicator for powered host ports
E9	1	P5IU	ID	Connected to the ID pin of the mini-AB connector for OTG applications. With the help of an internal pull-up resistor, this pin determines the chip's responsibility in an OTG application (0: A-peripheral, 1:B-peripheral)
E10	1	P5O	/PO	Turn on/off the gang power for all host ports
Clock Interface (2 pins)				
K6	1	I	XSCI	Input. A 12 MHz passive crystal should be connected across the two pins (XSCI and XSCO). Optionally, a 12 MHz oscillator can be connected to XSCI while keeping XSCO unconnected
K7	1	O	XSCO	Output
Internal V_{BUS} Charge Pump (3 pins)				
H10	1	O	PD_PMOS	Internal charge pump output for P-MOSFET (optional switch on the V_{OUT})
J10	1	O	EXT	Internal charge pump output for N-MOSFET
G10	1	I	V_{OUT}	Internal charge pump output voltage feedback pin
Test (1 pin)				
C10	1	SIUC	TEST	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation
Miscellaneous (2 pins)				
K5	1	B	REF_HOST	Connect external reference resistor (12 KΩ +/- 1%) to V_{SSA}. One per port
K10	1	B	REF_OTG	

Note to Table 13:

1 Type key: format is [(L)(W_)X(Y)(_Z(T))] where the following conventions apply:

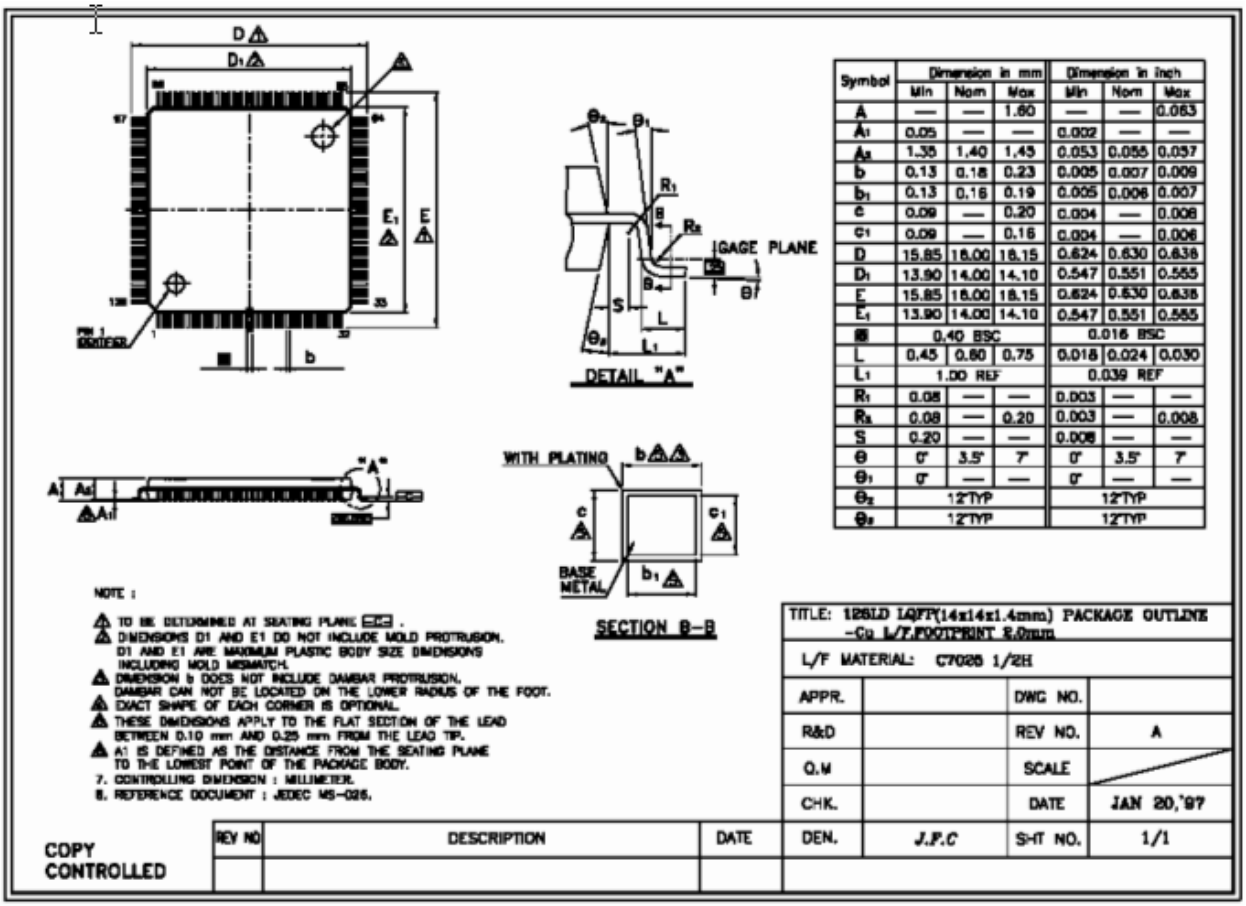
L—Logic Level		W—Tolerance		X—Type		Y—Pull		Z—Drive	T—Tristate	
P(2)	OD 3.3 CMOS	5	5 V	I	Input	U	Pull up	C(4)	T	Tristate
M(3)	Multi-voltage: 3.3 V CMOS 2.5 V CMOS 1.8 V CMOS		3.3 V	O	Output	D	Pull down			Normal
S	Schmitt Trigger			B	Bidirectional		None			

2 Program to OD or 3.3 V CMOS via the ASO register (0x0068).
3 Program to 3.3, 2.5, or 1.8 V by setting the V_{IO} voltage level.
4 Program to 2 mA, 4 mA, 6 mA, or 8 mA via the I/O Control register (0x006C).

Package Layout

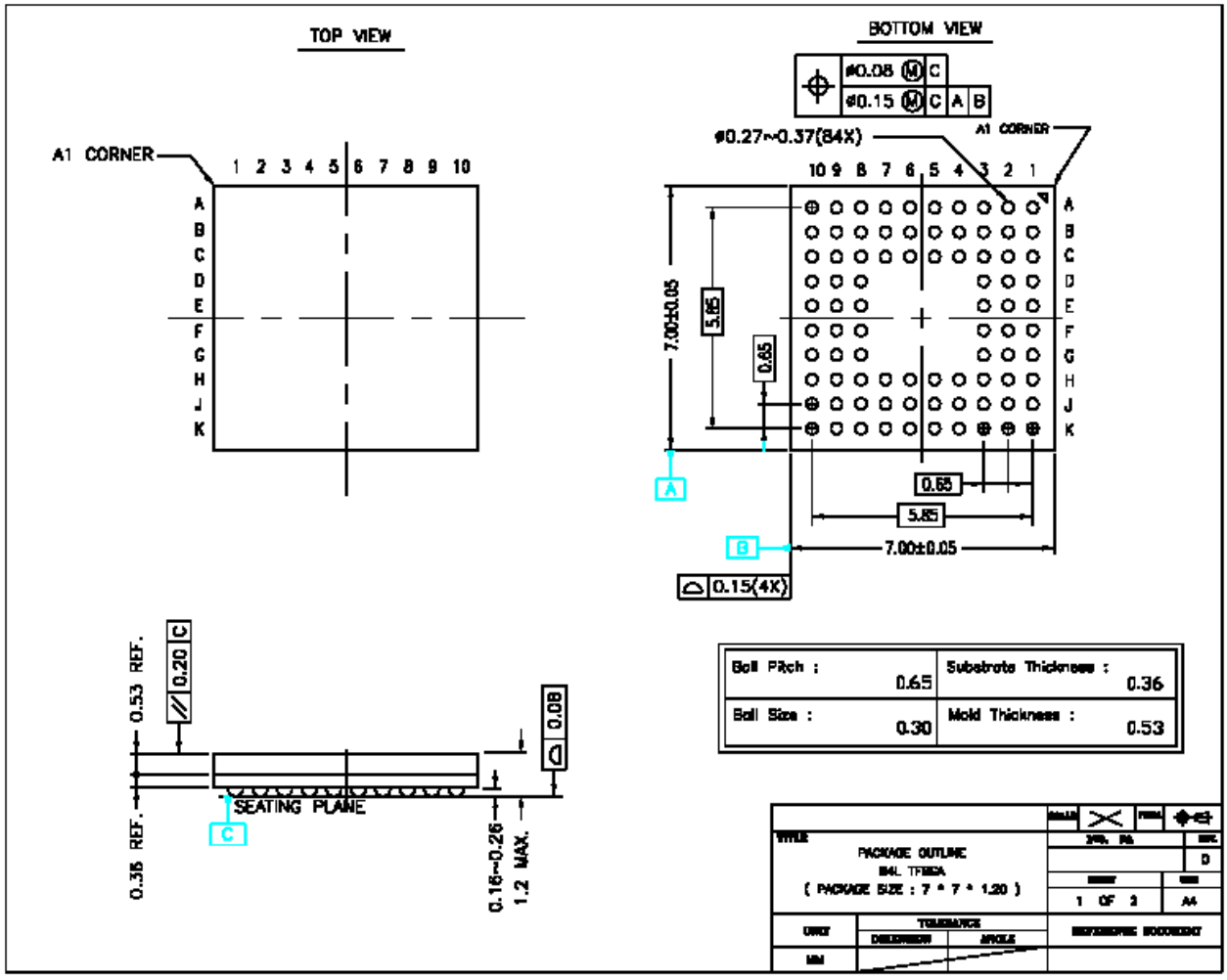
Figure 4 shows the package layout for the 128-pin LQFP package. Figure 5 on page 17 shows the layout for the 84-ball TFBGA.

Figure 4 128-Pin LQFP



Symbol	Dimension in mm			Dimension in Inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

Figure 5 84-Ball TFBGA Package



Ordering Information

The following conventions are used to identify Oxford Semiconductor products:

OXU210HP - LQBG

- Green (RoHS compliant)
- Revision
- Package Type: LQ 128-Pin LQFP
- Part Number

OXU210HP - TBBG

- Green (RoHS compliant)
- Revision
- Package Type: TB 84-Ball TF-BGA
- Part Number

Contacting Oxford Semiconductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further detail about Oxford Semiconductor devices, or email sales@oxsemi.com.

Revision Information

Table 14 documents the revisions of this data sheet.

Table 14 Revision Information

Revision	Modification
Jun 06	First publication
Dec 06	Miscellaneous editorial changes