NEC

User's Manual

IE-703107-MC-EM1

In-Circuit Emulator Option Board

Target Devices
V850E/MA1
V850E/MA2

Document No. U14481EJ2V0UM00 (2nd edition)
Date Published September 2003 N CP(K)

[MEMO]

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J03.4

Major Revisions in This Edition (1/2)

Page	Description
Throughout	Addition of V850E/MA2 to target devices
p.14	**1.1 Hardware Configuration** • Addition of SWEX-xxxSD-1 to extension probes • Addition of conversion socket for V850E/MA1 (161-pin FBGA) • Addition of conversion socket for V850E/MA2 (100-pin LQFP)
p.15	Change of **1.2 Features (When Connected to IE-V850E-MC-A)** to **1.2 Hardware Specifications (When Connected to IE-V850E-MC-A)**
p.16	Change of **1.3 Function Specifications (When Connected to IE-V850E-MC-A)** to **1.3 System Specifications of IE-703107-MC-EM1 (When Connected to IE-V850E-MC-A)**
pp.17 to 19	**1.4 System Configuration** • Change of **Figure 1-1 System Configuration** to **Figure 1-1 System Configuration (V850E/MA1, 144-Pin LQFP)** • Addition of **Figure 1-2 System Configuration (V850E/MA1, 161-Pin FBGA)** • Addition of **Figure 1-3 System Configuration (V850E/MA2, 100-Pin LQFP)**
p.20	**1.5 Contents in Carton** • Addition and modification of description • Modification of **Figure 1-4 Contents in Carton**
p.21	Modification of **Figure 1-5 Connection Between IE-V850E-MC-A and IE-703107-MC-EM1**
pp.24, 25	**2.1 Names and Functions of IE-703107-MC-EM1 Components** • Modification of **Figure 2-1 IE-703107-MC-EM1** • Addition and modification of description in **(6)** to **(10)**
pp.26 to 30	**2.2 Clock Settings** • Addition and modification of description • Addition of **Figure 2-2 Outline of Clock Settings** • Change of **Table 2-1 Clock Setting (When the Emulator is Used as a Stand-Alone Unit)** to **Table 2-1 List of Hardware Settings for Each Clock Setting** • Change of **Table 2-2 Clock Setting (When the Emulator is Used in Target System Connection)** to **Table 2-2 Settings When Using Mounted Internal Clock** • Addition of **Figure 2-3 Outline When Using Mounted Internal Clock** • Addition of **Table 2-3 Settings When Changing Mounted Internal Clock** • Addition of **Figure 2-4 Outline When Changing Mounted Crystal Oscillator and Using It as Internal Clock** • Addition of **Table 2-4 Settings When Using External Clock** • Addition of **Figure 2-5 Outline When Using Crystal Oscillator on Target System as External Clock**
p.31	Change of **2.3 MODE Pin Setting** to **2.3 Operation Mode Settings**
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p.35	Addition and modification of description in **CHAPTER 3 FACTORY SETTINGS**
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Major Revisions in This Edition (2/2)

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pp.73 to 81	**APPENDIX C CONNECTORS FOR TARGET CONNECTION** • Addition and modification of description in **C.1 Usage (LQFP Package)** • Addition and modification of description in **C.2 Cautions on Handling Connectors (LQFP Package)** • Addition of **C.3 Notes on Board Design (FBGA Package)** • Addition of **C.4 Soldering CSSOCKET (Main Enclosure Connector) to Target Board (FGBA Package)** • Addition of **C.5 Using LSPACK to Mount IC (FBGA Package)** • Addition of **C.6 Connecting In-Circuit Emulator (FBGA Package)** • Addition of **C.7 Notes on Handling LSPACK/CSSOCKET (FBGA Package)**
p.82	Modification of **Figure D-1 Method of Inserting Plastic Spacer**
p.83	Addition of **APPENDIX E REVISION HISTORY**

The mark ★ shows major revised points.

INTRODUCTION

Target Readers

This manual is intended for users who design and develop application systems using the V850E/MA1 and V850E/MA2.

Purpose

The purpose of this manual is to describe the proper operation of the IE-703107-MC-EM1, and its basic specifications.

Organization

This manual is broadly divided into the following parts.

- Overview
- Names and functions of components
- Factory settings
- Cautions
- Differences between target devices and target interface circuits

How to Read This Manual

It is assumed that the reader of this manual has general knowledge of electrical engineering, logic circuits, and microcontrollers.
The IE-703107-MC-EM1 is used connected to the IE-V850E-MC-A in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-703107-MC-EM1. For the names and functions, and the connection of parts, refer to the **IE-V850E-MC, IE-V850E-MC-A User's Manual (U14487E)**, which is a separate volume.

To understand the basic specifications and operation methods broadly
→ Read this manual in the order listed in **CONTENTS**.

To know the operation methods and command functions of the IE-V850E-MC-A and IE-703107-MC-EM1
→ Read the user's manual of the debugger (separate volume) that is used.

Conventions

Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeral representations:	Binary ··· ×××× or ××××B
	Decimal ··· ××××
	Hexadecimal ··· ××××H

Prefixes representing the power of 2 (address space, memory capacity):
K (kilo): $2^{10} = 1024$
M (mega): $2^{20} = 1024^2$

Terminology The meanings of terms used in this manual are listed below.

Target device	This is the device to be emulated.
Target system	The system (user-built system) to be debugged. This includes the target program and hardware configured by the user.

Related Documents When using this manual, refer to the following manuals.
The related documents indicated in this publication may include preliminary versions.
However, preliminary versions are not marked as such.

○ **Documents related to development tools (user's manuals)**

Product Name		Document Number
IE-V850E-MC, IE-V850E-MC-A (In-Circuit Emulator)		U14487E
IE-703107-MC-EM1 (In-Circuit Emulator Option Board)		This manual
V850E/MA1 Hardware		U14359E
V850E/MA2 Hardware		U14980E
V850 Series Development Tools (Supporting 32-Bit OS) Windows™ Based (Application Note)	Tutorial Guide	U16544E
CA850 (C Compiler Package) Ver.2.50	Operation	U16053E
	C Language	U16054E
	PM plus	U16055E
	Assembly Language	U16042E
ID850 (Ver.2.50 or later) (Integrated Debugger)	Operation	U16217E
SM850 (Ver.2.50 or later) (System Simulator)	Operation	U16218E
RX850 (Real-Time OS)	Basics	U13430E
	Installation	U13410E
RX850 Pro (Real-Time OS)	Basics	U13773E
	Installation	U13774E
RD850 (Ver. 3.0) (Task Debugger)		U13737E
RD850 Pro (Ver. 3.0) (Task Debugger)		U13916E
AZ850 (System Performance Analyzer)		U14410E
PG-FP4 (Flash Memory Programmer)		U15260E

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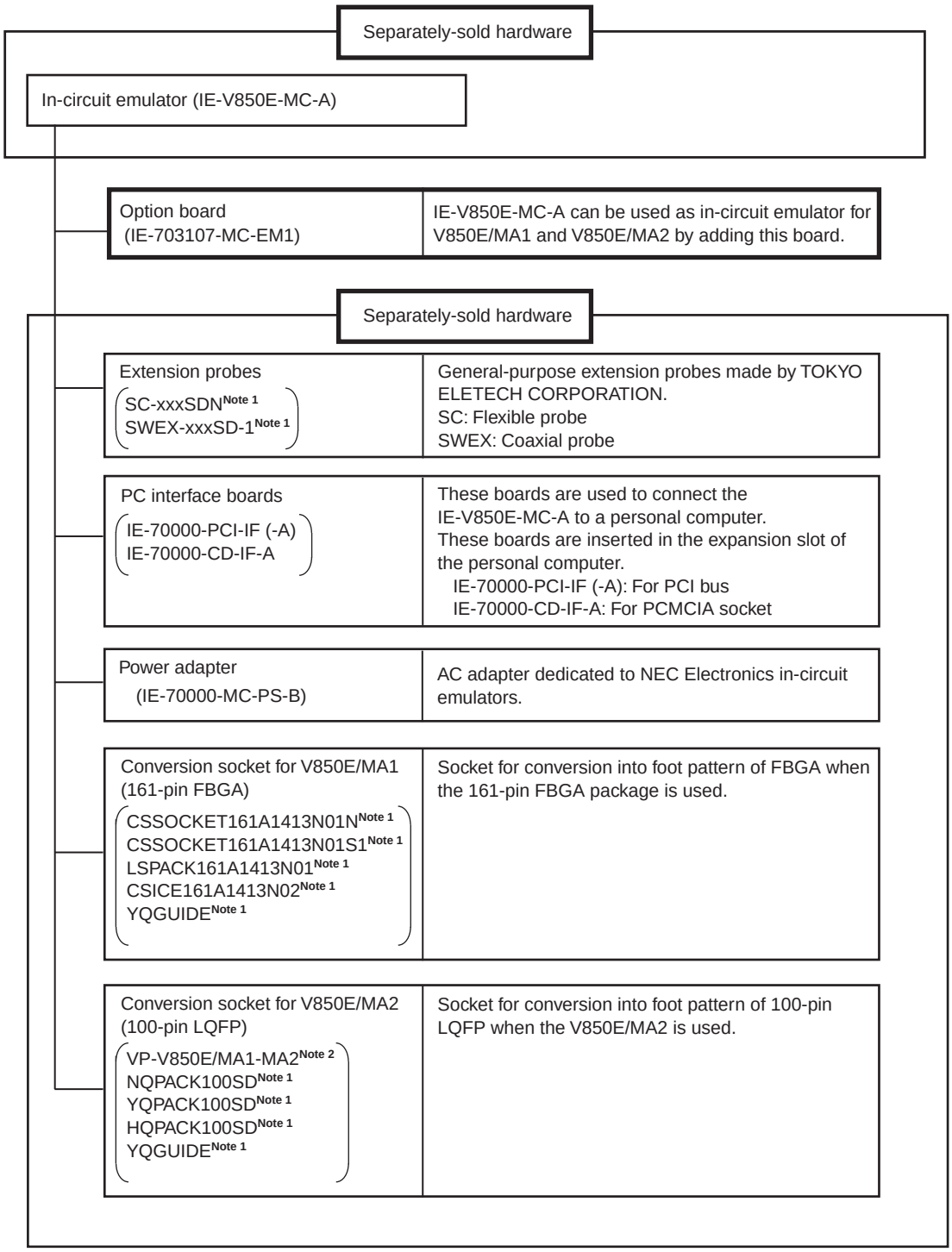
CHAPTER 1 OVERVIEW

The IE-703107-MC-EM1 is an option board for the in-circuit emulator IE-V850E-MC-A. By connecting the IE-703107-MC-EM1 to IE-V850E-MC-A, hardware and software can be debugged efficiently in system development using the V850E/MA1 and V850E/MA2.

In this manual, the basic setup sequences and switch settings of the IE-703107-MC-EM1 when connecting it to the IE-V850E-MC-A are described. For the names and functions of the parts of the IE-V850E-MC-A, and for the connection of elements, refer to the **IE-V850E-MC, IE-V850E-MC-A User's Manual (U14487E)** which is a separate volume.

1.1 Hardware Configuration



Notes 1. For further information, contact Daimaru Kogyo Co., Ltd.
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Osaka Electronics Department (TEL +81-6-6244-6672)

2. For further information, contact Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191)

★ 1.2 Hardware Specifications (When Connected to IE-V850E-MC-A)

Table 1-1. Hardware Specifications

Parameter		Value	
Target device		V850E/MA1	μPD703103AGJ-UEN μPD703105AGJ-xxx-UEN μPD703106AGJ-xxx-UEN μPD703107AGJ-xxx-UEN μPD70F3107AGJ-UEN μPD703106AF1-xxx-EN4 μPD703107AF1-xxx-EN4 μPD70F3107AF1-EN4 μPD703106AGJ(A)-xxx-UEN μPD703107AGJ(A)-xxx-UEN μPD70F3107AGJ(A)-xxx-UEN
		V850E/MA2	μPD703108GC-8EU
Target board interface voltage		$V_{DD} = AV_{DD} = CV_{DD} = AV_{REF} = 3.3 \pm 0.3$ V $V_{SS} = AV_{SS} = CV_{SS} = 0$ V	
Maximum operation frequency		50 MHz (40 MHz when the in-circuit emulator is used for the V850E/MA2)	
External dimensions (refer to **APPENDIX A DIMENSIONS**)	Height	15 mm	
	Length	206 mm	
	Width	96 mm	
Power consumption		9.1 W (Max.)	
Weight		190 g	

Remark “xxx” indicates ROM code suffix.

- Extremely lightweight and compact
- Higher equivalence with target device can be achieved by omitting buffer between signal cables.
- External data of 8 bits can be traced by connecting an external logic probe (included).
- The following pins can be masked.
  $\overline{\text{RESET}}$, NMI, $\overline{\text{WAIT}}$, $\overline{\text{HLDRQ}}$, STOP

★ 1.3 System Specifications of IE-703107-MC-EM1 (When Connected to IE-V850E-MC-A)

Table 1-2. System Specifications of IE-703107-MC-EM1 (When Connected to IE-V850E-MC-A)

Parameter		Specification
Emulation memory capacity	Internal ROM	1 MB (Max.)
	External memory	4 MB (Max.)
Execution/pass detection coverage	Internal ROM	1 MB (Max.)
Program execution function	Real-time execution function	Go, execution from cursor position, automatic go, execution up to cursor position, restart, return out
	Non-real-time execution function	Step-in, next over, slow-motion
Break function		Event detection break, software break, forced break, break via come function, break on condition met during step execution, failsafe break
Trace function	Trace condition	All trace, section trace, qualify trace
	Memory capacity	168 bits × 32 K frames
Other functions		Mapping function, event function, snapshot function, stub function, register manipulation function, memory manipulation function, time measurement function, real-time RAM sampling function

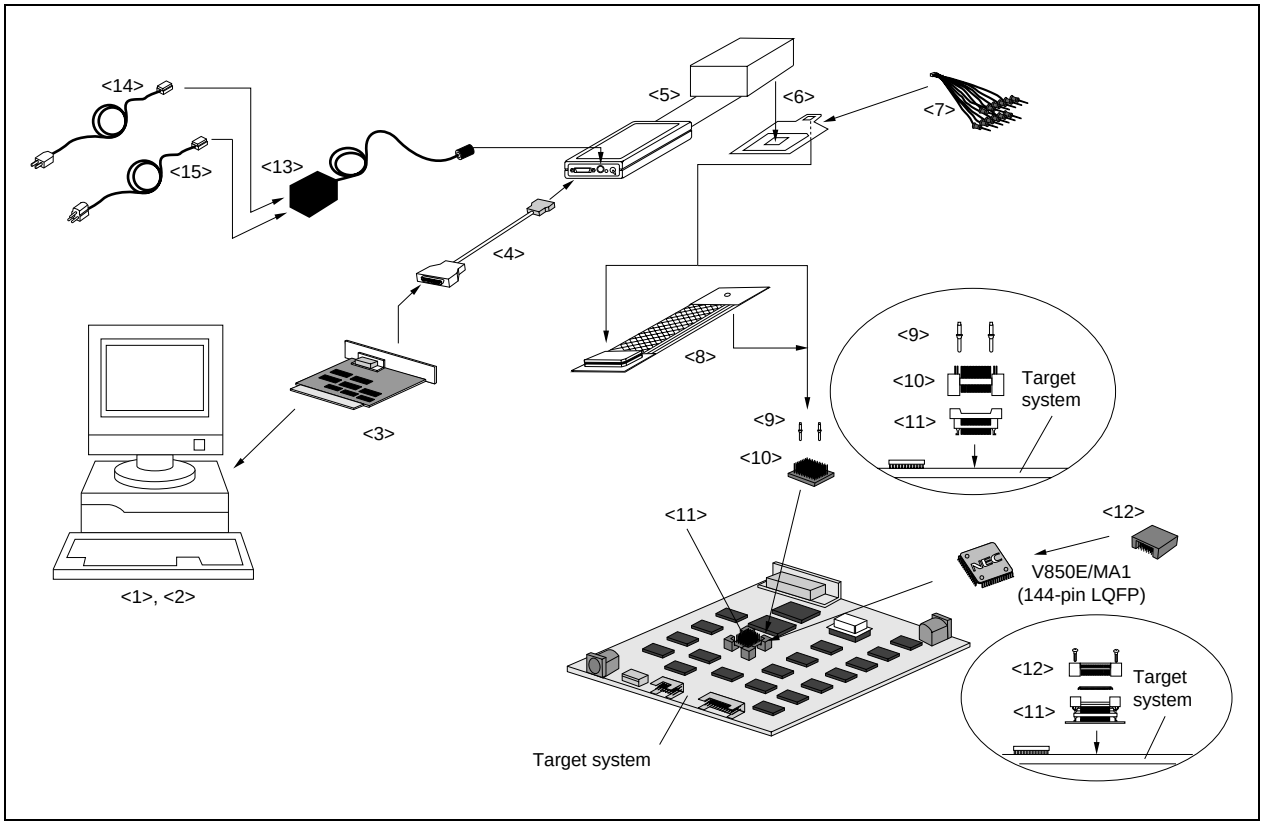
Caution Some of the functions may not be supported depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-703107-MC-EM1 to the IE-V850E-MC-A, which is then connected to a personal computer (PC-9800 series, PC/AT™ or compatible) is shown below.

★
- V850E/MA1 (144-pin LQFP): Refer to **Figure 1-1**.
- V850E/MA1 (161-pin FBGA): Refer to **Figure 1-2**.
- V850E/MA2 (100-pin LQFP): Refer to **Figure 1-3**.

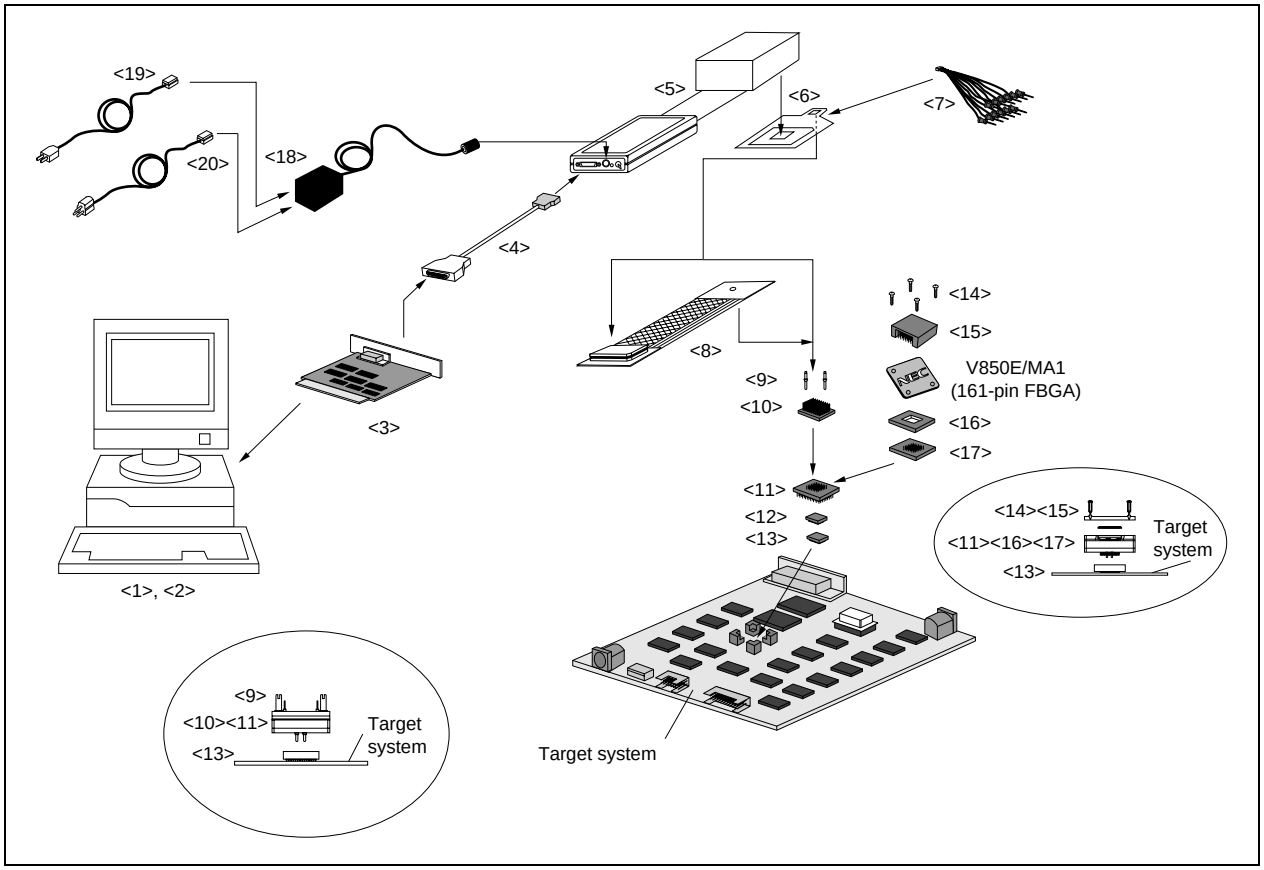
★ **Figure 1-1. System Configuration (V850E/MA1, 144-Pin LQFP)**



Remarks 1. <1> Personal computer (PC-9800 series, PC/AT or compatible)
<2> Debugger (sold separately), device file
<3> PC interface board (IE-70000-PCI-IF(-A), IE-70000-CD-IF-A: sold separately)
<4> PC interface cable (included with IE-V850E-MC-A)
<5> In-circuit emulator (IE-V850E-MC-A: sold separately)
<6> In-circuit emulator option board (IE-703107-MC-EM1: this product)
<7> External logic probe (included with IE-703107-MC-EM1)
<8> Extension probe (SC-144SDN, SWEX-144SD-1: sold separately)
<9> Guide screws (YQGUIDE: included)
<10> IE connector for 144-pin LQFP (YQPACK144SD: included)
<11> Target connection socket for 144-pin LQFP (NQPACK144SD: included)
<12> Cover for mounting device in 144-pin LQFP (HQPACK144SD: included)
<13> Power adapter (IE-70000-MC-PS-B: sold separately)
<14> AC100 V power cable (sold separately: included with IE-70000-MC-PS-B)
<15> AC220 V power cable (sold separately: included with IE-70000-MC-PS-B)

2. The encircled portions show enlarged figures of the connectors for target connection.

★ **Figure 1-2. System Configuration (V850E/MA1, 161-Pin FBGA)**



Remarks 1. <1> Personal computer (PC-9800 series, PC/AT or compatible)

<2> Debugger (sold separately), device file

<3> PC interface board (IE-70000-PCI-IF(-A), IE-70000-CD-IF-A: sold separately)

<4> PC interface cable (included with IE-V850E-MC-A)

<5> In-circuit emulator (IE-V850E-MC-A: sold separately)

<6> In-circuit emulator option board (IE-703107-MC-EM1: this product)

<7> External logic probe (included with IE-703107-MC-EM1)

<8> Extension probe (SC-144SDN, SWEX-144SD-1: sold separately)

<9> Guide screws (YQGUIDE: included)

<10> IE connector for 161-pin FBGA (CSICE161A1413N02: sold separately)

<11> Pogo pin connector for 161-pin FBGA (LSPACK161A1413N01: sold separately)

<12> Stacking socket for 161-pin FBGA (option) (CSSOCKET161A1413N01S1: sold separately)

<13> Target connection socket for 161-pin FBGA (CSSOCKET161A1413N01N: sold separately)

This is a type of target connection socket without guide pins.

The type of target connection socket with guide pins is the CSSOCKET161A1413N01.

<14> Screw for mounting device (included with LSPACK161A1413N01)

<15> Cover for mounting device (included with LSAPCK161A1413N01)

<16> Spacer for mounting device (included with LSPACK161A1413N01)

<17> Guide plate for mounting device (included with LSPACK161A1413N01)

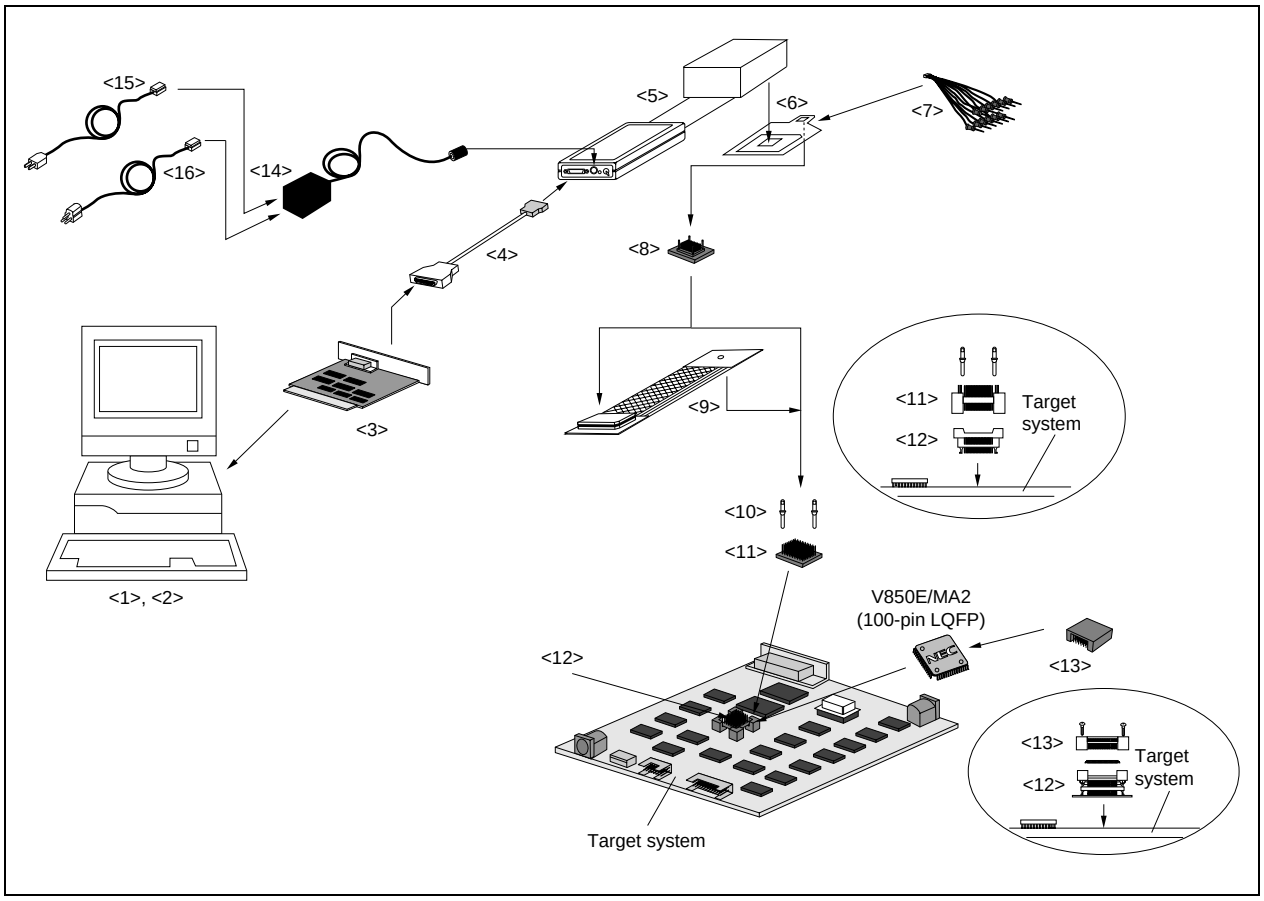
<18> Power adapter (IE-70000-MC-PS-B: sold separately)

<19> AC100 V power cable (sold separately: included with IE-70000-MC-PS-B)

<20> AC220 V power cable (sold separately: included with IE-70000-MC-PS-B)

2. The encircled portions show enlarged figures of the connectors for target connection.

★ **Figure 1-3. System Configuration (V850E/MA2, 100-Pin LQFP)**



Remarks 1. <1> Personal computer (PC-9800 series, PC/AT or compatible)

<2> Debugger (sold separately), device file

<3> PC interface board (IE-70000-PCI-IF(-A), IE-70000-CD-IF-A: sold separately)

<4> PC interface cable (included with IE-V850E-MC-A)

<5> In-circuit emulator (IE-V850E-MC-A: sold separately)

<6> In-circuit emulator option board (IE-703107-MC-EM1: this product)

<7> External logic probe (included with IE-703107-MC-EM1)

<8> 144-pin to 100-pin conversion adapter (VP-V850E/MA1-MA2: sold separately)

<9> Extension probe (SC-100SDN, SWEX-100SD-1: sold separately)

<10> Guide screws (YQGUIDE: included)

<11> IE connector for 100-pin LQFP (YQPACK100SD: included with VP-V850E/MA1-MA2)

<12> Target connection socket for 100-pin LQFP (NQPACK100SD: included with VP-V850E/MA1-MA2)

<13> Cover for mounting device in 100-pin LQFP (HQPACK100SD: included with VP-V850E/MA1-MA2)

<14> Power adapter (IE-70000-MC-PS-B: sold separately)

<15> AC100 V power cable (sold separately: included with IE-70000-MC-PS-B)

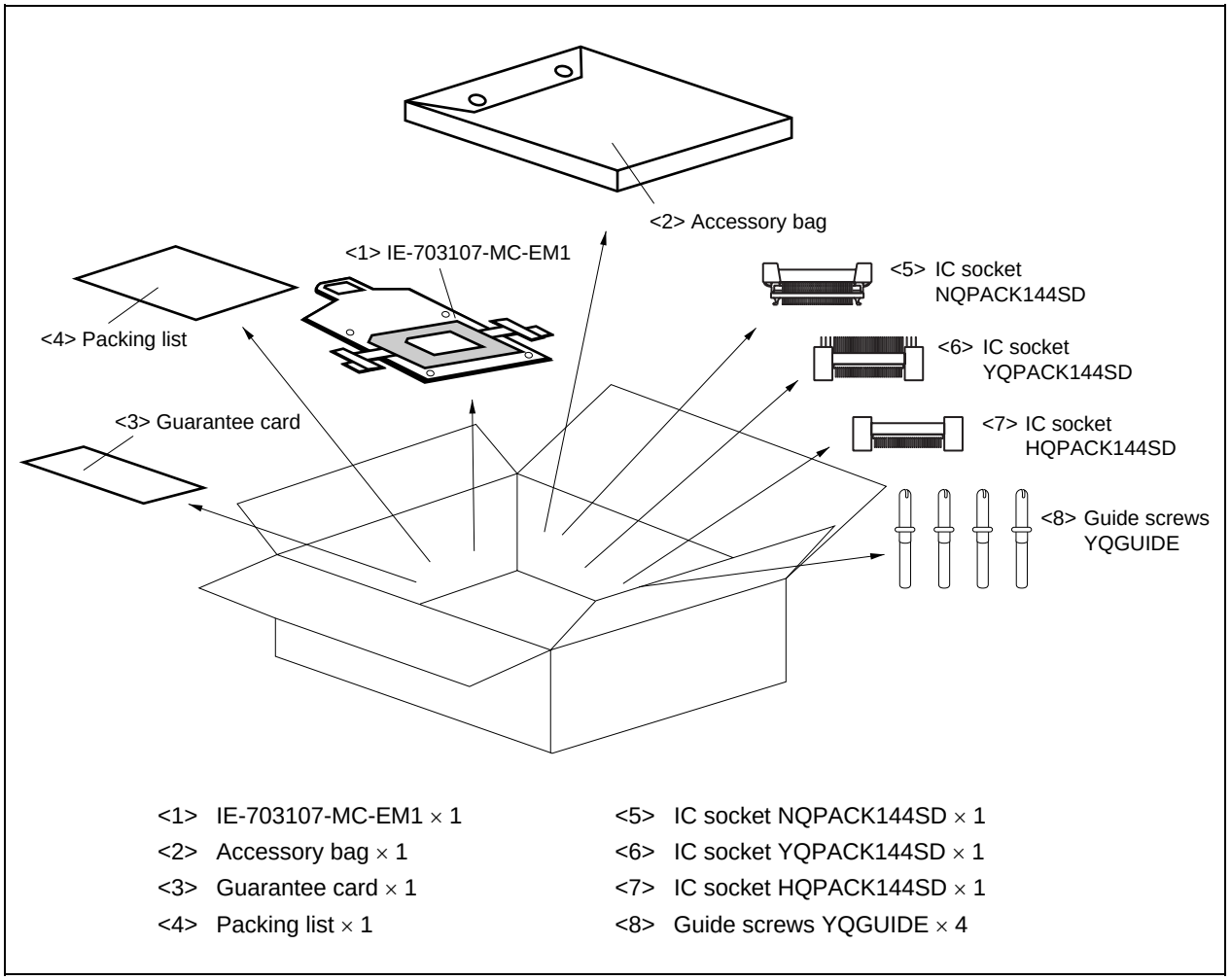
<16> AC220 V power cable (sold separately: included with IE-70000-MC-PS-B)

2. The encircled portions show enlarged figures of the connectors for target connection.

1.5 Contents in Carton

The carton of the IE-703107-MC-EM1 contains the main unit, a guarantee card, a packing list, and an accessory bag. Make sure that the accessory bag contains this manual and connector accessories. In the case of missing or damaged items, contact an NEC Electronics sales representative or distributor.

★ **Figure 1-4. Contents in Carton**



★ Check that the accessory bag contains this manual, a packing list, an external logic probe, and a restriction document.

1.6 Connection Between IE-V850E-MC-A and IE-703107-MC-EM1

The procedure for connecting the IE-V850E-MC-A and IE-703107-MC-EM1 is described below.

Caution Connect carefully so as not to break or bend connector pins.

<1> Remove the POD cover (lower) of the IE-V850E-MC-A.
<2> Set the PGA socket lever of the IE-703107-MC-EM1 to the OPEN position as shown in Figure 1-5 (b).
<3> Connect the IE-703107-MC-EM1 to the PGA socket at the rear of the POD (refer to **Figure 1-5 (c)**). When connecting, position the IE-V850E-MC-A and IE-703107-MC-EM1 so that they are horizontal.
Spacers can be connected to fix the POD (refer to **APPENDIX D MOUNTING OF PLASTIC SPACER**).
<4> Set the PGA socket lever of the IE-703107-MC-EM1 to the CLOSE position as shown in Figure 1-5 (b).
<5> Fix the POD cover (lower) to the soldered side of the IE-703107-MC-EM1 using the nylon rivets supplied with the IE-V850E-MC-A.

★ **Figure 1-5. Connection Between IE-V850E-MC-A and IE-703107-MC-EM1 (1/2)**

(a) Connection overview

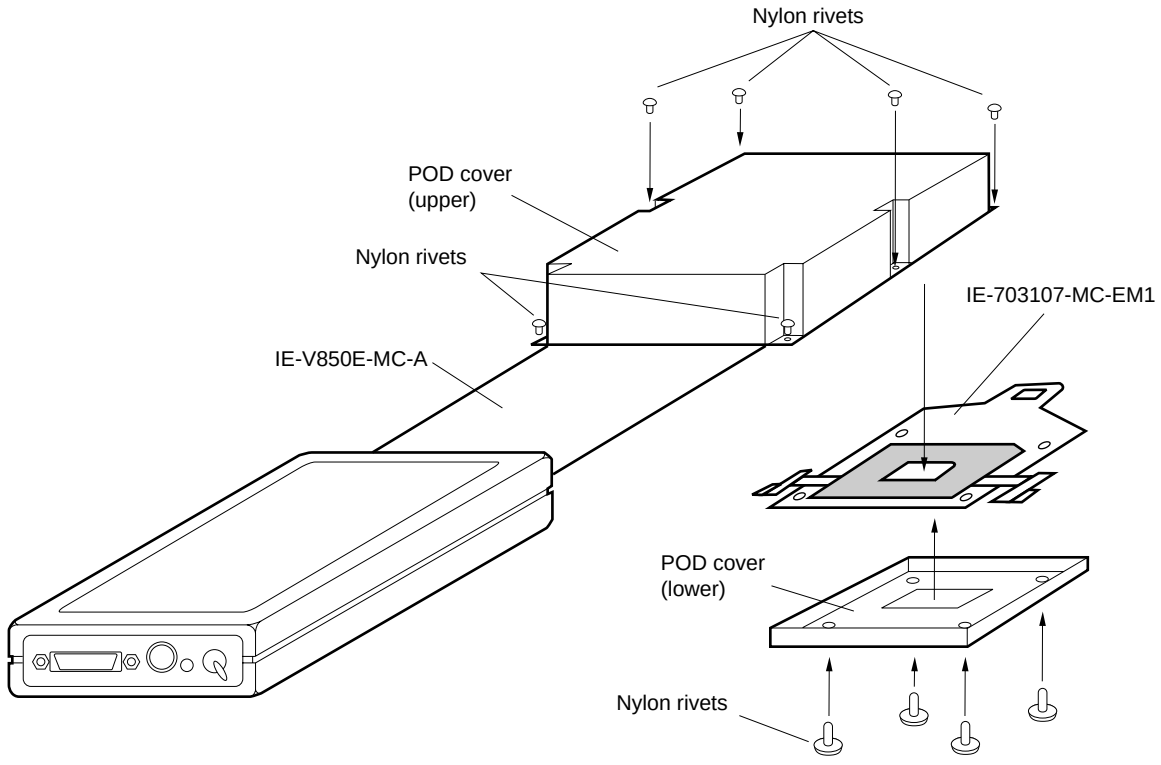
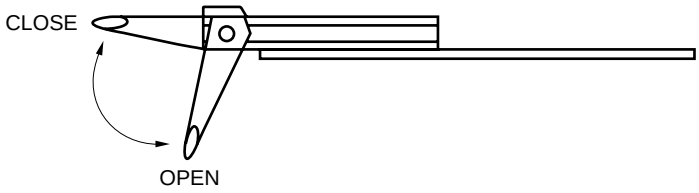
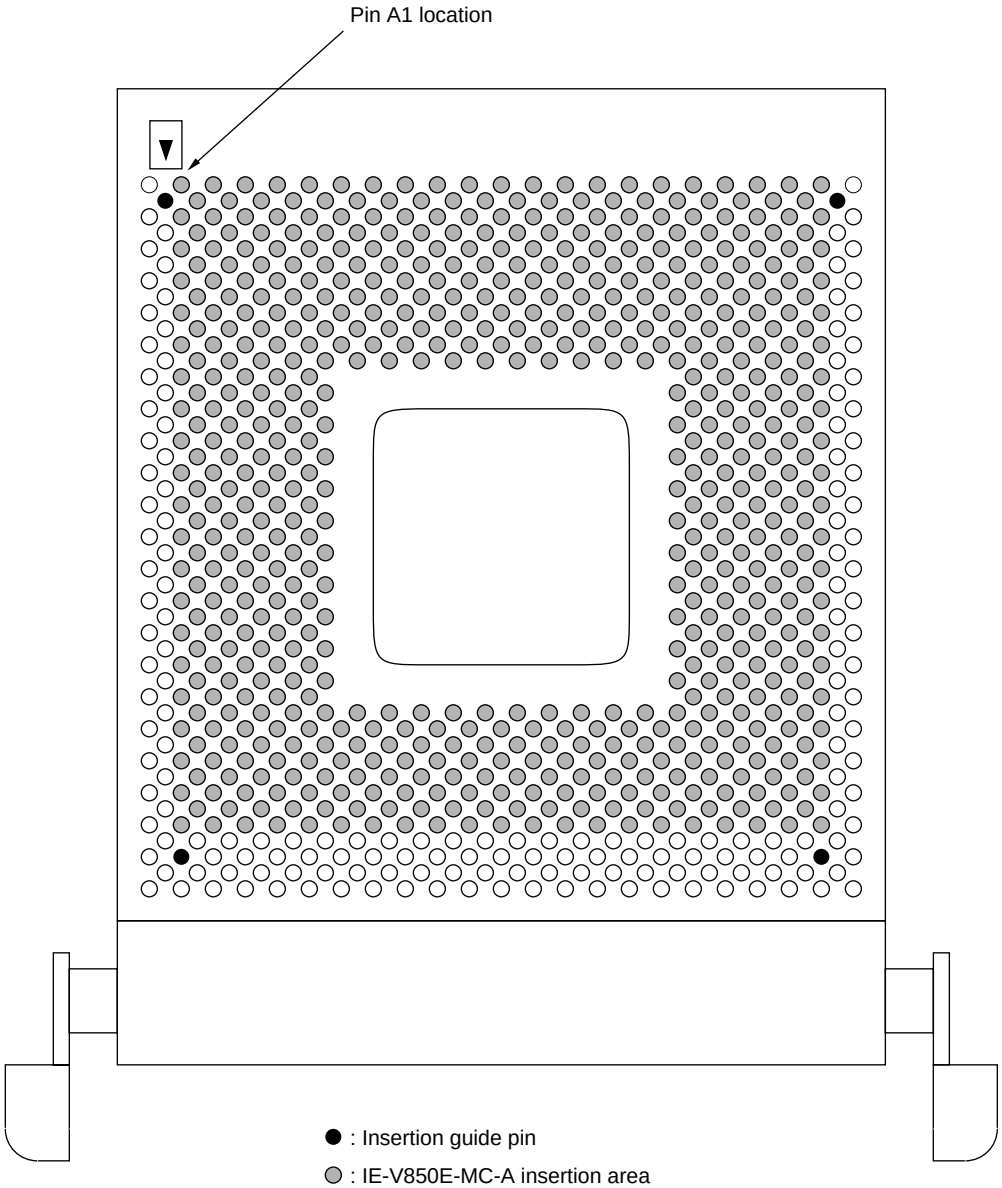


Figure 1-5. Connection Between IE-V850E-MC-A and IE-703107-MC-EM1 (2/2)

(b) PGA socket lever of IE-703107-MC-EM1



(c) Connecting part (IE-703107-MC-EM1)



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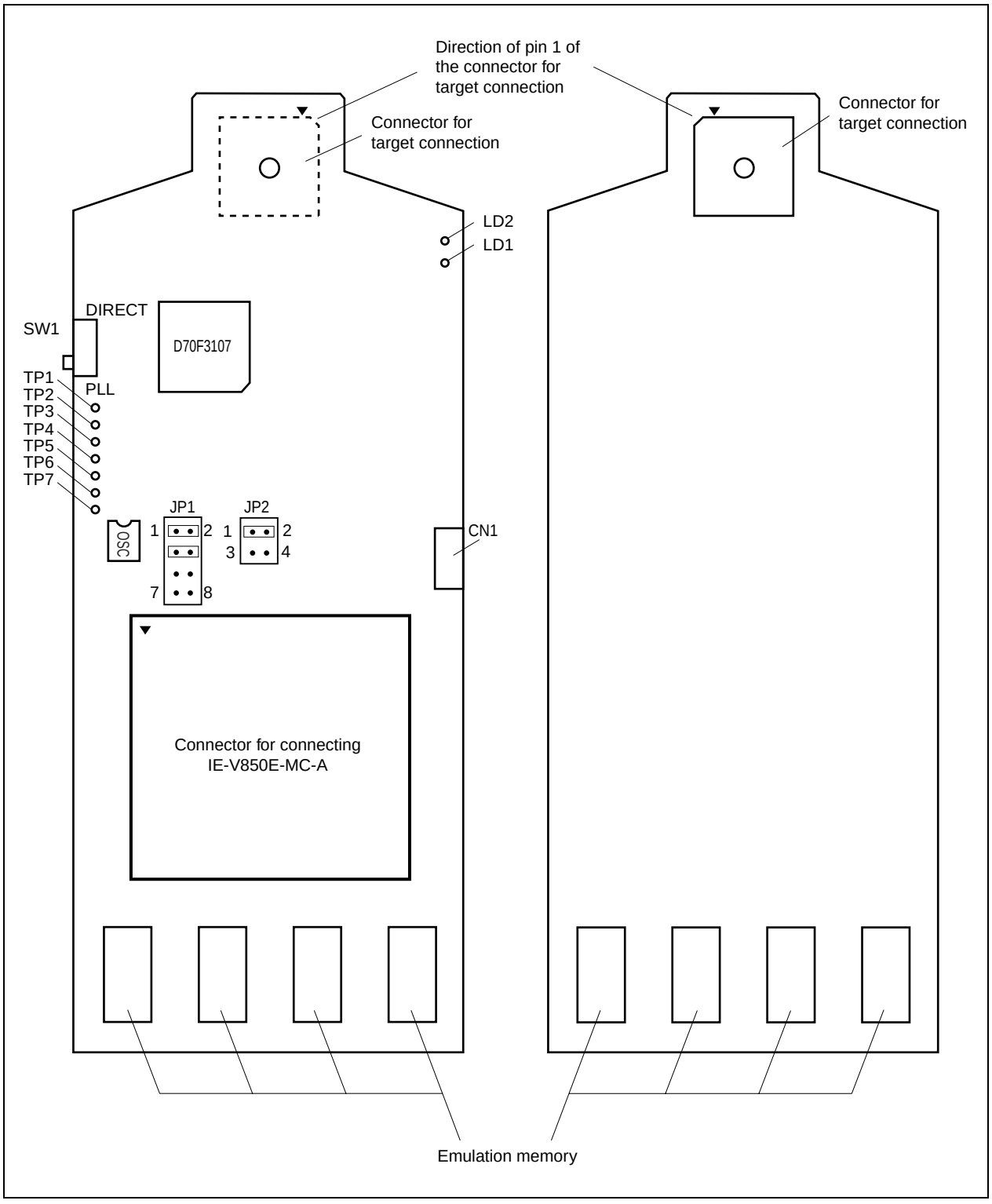
CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS

This chapter describes the names, functions, and switch settings of components comprising the IE-703107-MC-EM1. For the details of the pod, jumper, and switch positions, etc., refer to the **IE-V850E-MC**, **IE-V850E-MC-A User's Manual (U14487E)**.

2.1 Names and Functions of IE-703107-MC-EM1 Components

★ **Figure 2-1. IE-703107-MC-EM1**



(1) Test pins (TP1 to TP7)

To leave the DMA cycle or refresh cycle in the tracer, or cause a break, connect these pins to the external logic probe.

- TP1: GND
- TP2: $\overline{\text{REFRQ}}$
- TP3: DMAAK0
- TP4: DMAAK1
- TP5: DMAAK2
- TP6: DMAAK3
- TP7: Test pin for product shipment inspection

(2) SW1

This is a switch for clock mode switching (for details, refer to **2.2 Clock Settings**).

(3) JP1

This is a jumper for switching the clock supply source (for details, refer to **2.2 Clock Settings**).

(4) JP2

This is a jumper for switching the power supply (for details, refer to **2.4 Power Supply Settings**).

(5) CN1

Connects the external logic probe (included).

(6) LD1 (CKSEL: Green)

★ This LED indicates the level input to the CKSEL pin. If the target system is not connected, whether this LED lights or not is determined by the setting of SW1.

LED Status	When Used as Stand-Alone Unit	When Used Connected to Target System
Lit	SW1 = DIRECT	The CKSEL signal from the target system is high
Extinguished	SW1 = PLL	The CKSEL signal from the target system is low

★ **(7) LD2 (RUN: Yellow)**

This LED indicates whether the program is under execution.

LED Status	Meaning
Lit	User program is being executed.
Extinguished	User program is halted.

(8) Connector for IE-V850E-MC-A connection

This is a connector for connecting the IE-V850E-MC-A.

(9) Connector for target connection

This is a connector for connecting the target system or the extension probe.

(10) Emulation memory

This is a memory that replaces the memory/memory mapped I/O on the target system (for details, refer to **2.5 Emulation Memory**).

2.2 Clock Settings

★ 2.2.1 Outline of clock settings

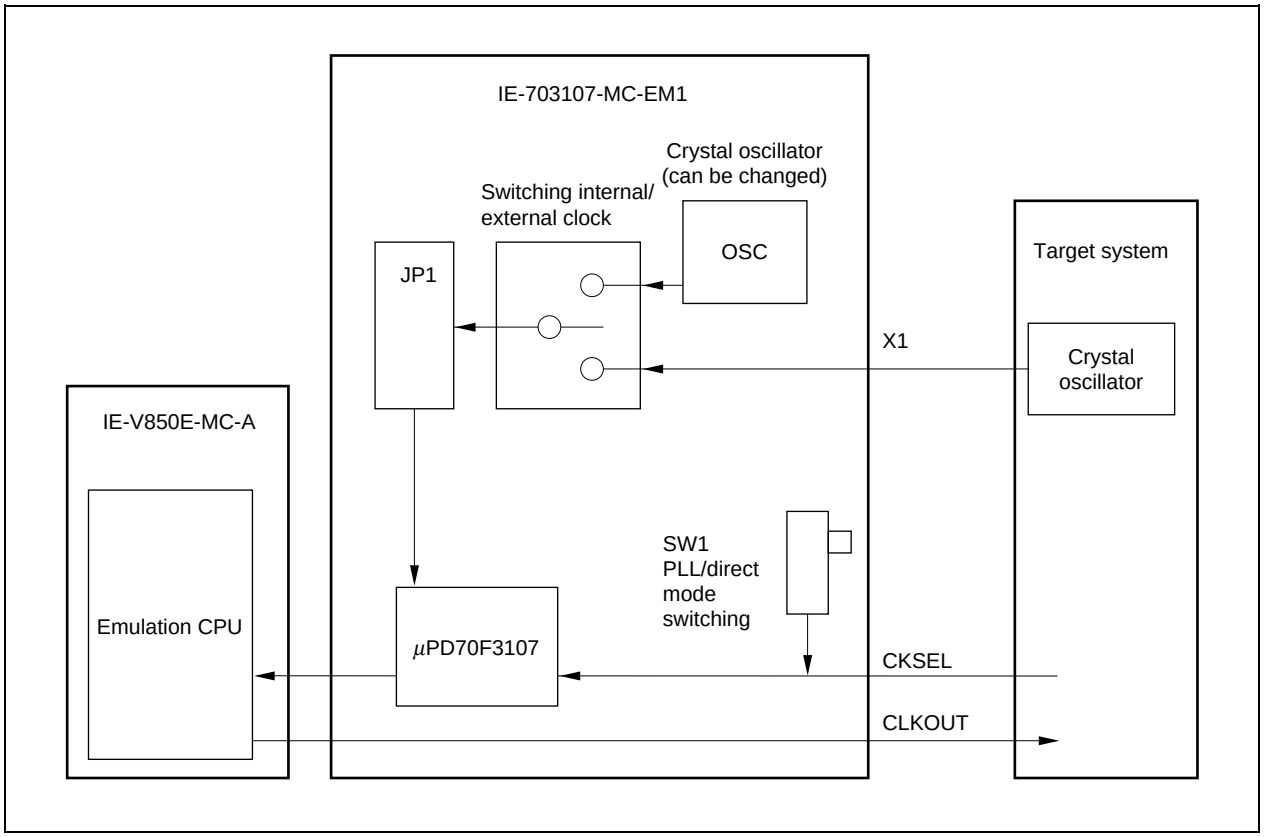
The following three clock setting methods are available.

For details, refer to **2.2.2 Clock setting methods**.

(1) Use the crystal oscillator mounted on the IE-703107-MC-EM1 as the internal clock.
(2) Change the crystal oscillator mounted on the IE-703107-MC-EM1 and use it as the internal clock.
(3) Use the crystal oscillator on the target system as an external clock.

Caution When using an external clock, input a square wave to the X1 pin.
When a clock generated by a crystal/ceramic resonator is used, the IE-703107-MC-EM1 does not operate.

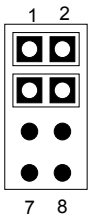
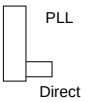
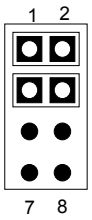
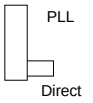
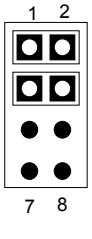
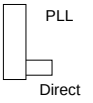
Figure 2-2. Outline of Clock Settings



★ 2.2.2 Clock setting methods

A list of the hardware settings for each clock setting is shown below.

Table 2-1. List of Hardware Settings for Each Clock Setting

Type of Clock Used	Clock Source Selection[Note 1]	OSC Crystal Oscillator	JP1 Setting	Clock Mode	SW1	CKSEL Pin[Note 2]
(1) Use crystal oscillator (OSC) mounted on IE-703107-MC-EM1 as internal clock.	Internal	Factory setting (5.000 MHz)		PLL		Low-level input
				Direct		High-level input
(2) Change crystal oscillator (OSC) mounted on IE-703107-MC-EM1 and use it as the internal clock[Note 3].	Internal	Change (to other than 5.000 MHz)		PLL		Low-level input
				Direct		High-level input
(3) Use the crystal oscillator on the target system as an external clock.	External	Crystal oscillator can be either mounted or not mounted		PLL		Low-level input
				Direct		High-level input

Notes 1. Select the clock source in the clock source selection area in the configuration dialog box on the debugger.

2. The input setting to the CKSEL pin is made only when a target system is connected. Leave this pin open when operating the emulator on a stand-alone basis. The emulator operates according to the setting of SW1.

3. When replacing the crystal oscillator on the emulator, use an oscillator with the following specifications.

Power supply voltage	5 V
Output level	CMOS
Shape	8-pin type
Pin layout	Pin 1: NC Pin 4: GND Pin 5: OUT Pin 8: V_{DD}

Caution Settings other than those described above are prohibited.

(1) Using the crystal oscillator (OSC) mounted on the IE-703107-MC-EM1 as the internal clock

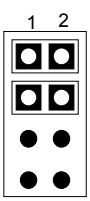
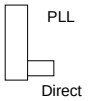
<1> Mount the 5.000 MHz crystal oscillator mounted at factory shipment in the OSC socket of the IE-703107-MC-EM1 (with the default settings).

<2> Change JP1 as indicated in Table 2-2 (with the default settings).

<3> Set the SW1 and CKSEL pins according to the clock mode to be used, as shown in Table 2-2.

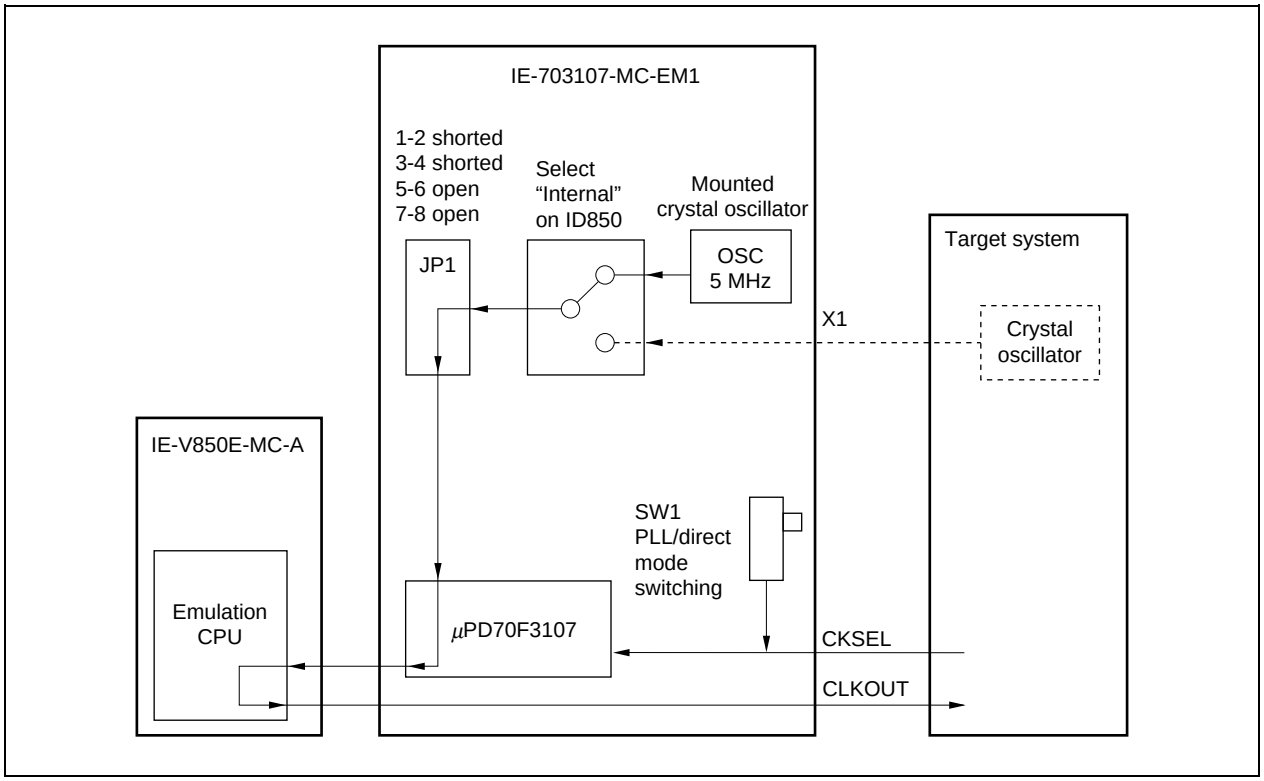
<4> To start up the integrated debugger (ID850), select “Internal” in the clock source selection area in the configuration dialog box (clock selection in emulator).

Table 2-2. Settings When Using Mounted Internal Clock

Type of Clock Used	Clock Source Selection	OSC Crystal Oscillator	JP1 Setting	Clock Mode	SW1	CKSEL Pin[Note]
Use crystal oscillator (OSC) mounted on IE-703107-MC-EM1 as internal clock.	Internal	Factory setting (5.000 MHz)		PLL		Low-level input
				Direct		High-level input

Note The input setting to the CKSEL pin is made only when a target system is connected.
Leave this pin open when operating the emulator on a stand-alone basis. The emulator operates according to the setting of SW1.

Figure 2-3. Outline When Using Mounted Internal Clock



(2) Changing the crystal oscillator (OSC) mounted on the IE-703107-MC-EM1 and using it as the internal clock

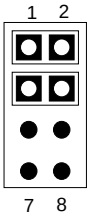
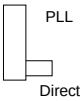
<1> Remove the crystal oscillator (OSC) that is mounted on the IE-703107-MC-EM1 and mount the oscillator to be used.

<2> Set JP1 as shown in Table 2-3 (with the default settings).

<3> Set the SW1 and CKSEL pins according to the clock mode to be used, as shown in Table 2-3.

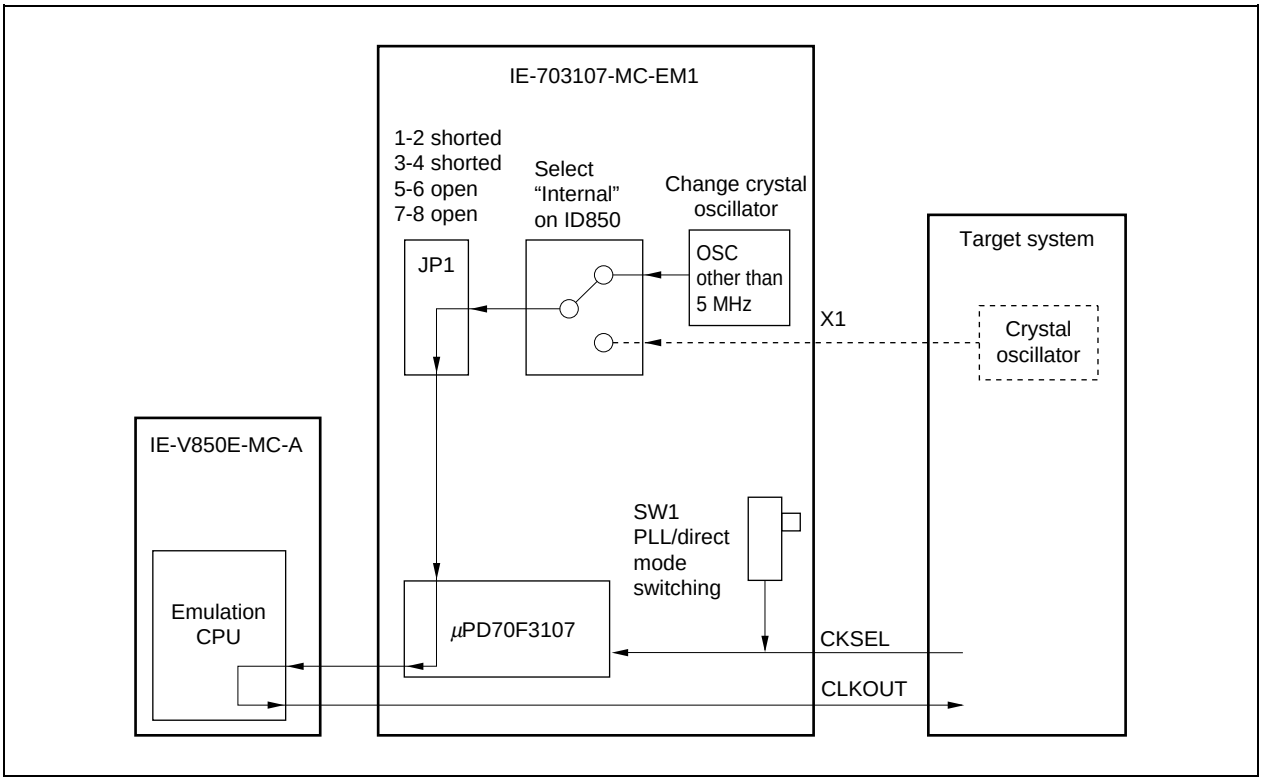
<4> Select “Internal” in the clock source selection area in the configuration dialog box on the integrated debugger (ID850).

Table 2-3. Settings When Changing Mounted Internal Clock

Type of Clock Used	Clock Source Selection	OSC Crystal Oscillator	JP1 Setting	Clock Mode	SW1	CKSEL Pin[Note]
Change the crystal oscillator mounted on IE-703107-MC-EM1 and use it as the internal clock.	Internal	Change (to other than 5.000 MHz)		PLL		Low-level input
				Direct		High-level input

Note The input setting to the CKSEL pin is made only when a target system is connected.
Leave this pin open when operating the emulator on a stand-alone basis. The emulator operates according to the setting of SW1.

Figure 2-4. Outline When Changing Mounted Crystal Oscillator and Using It as Internal Clock



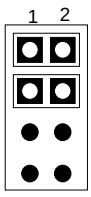
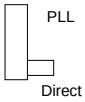
(3) Using the target system crystal oscillator as an external clock

<1> Set JP1 as shown in Table 2-5 (with the default setting).

<2> Set the SW1 and CKSEL pins according to the clock mode to be used, as shown in Table 2-5.

<3> Select “External” in the clock source selection area in the configuration dialog box on the integrated debugger (ID850).

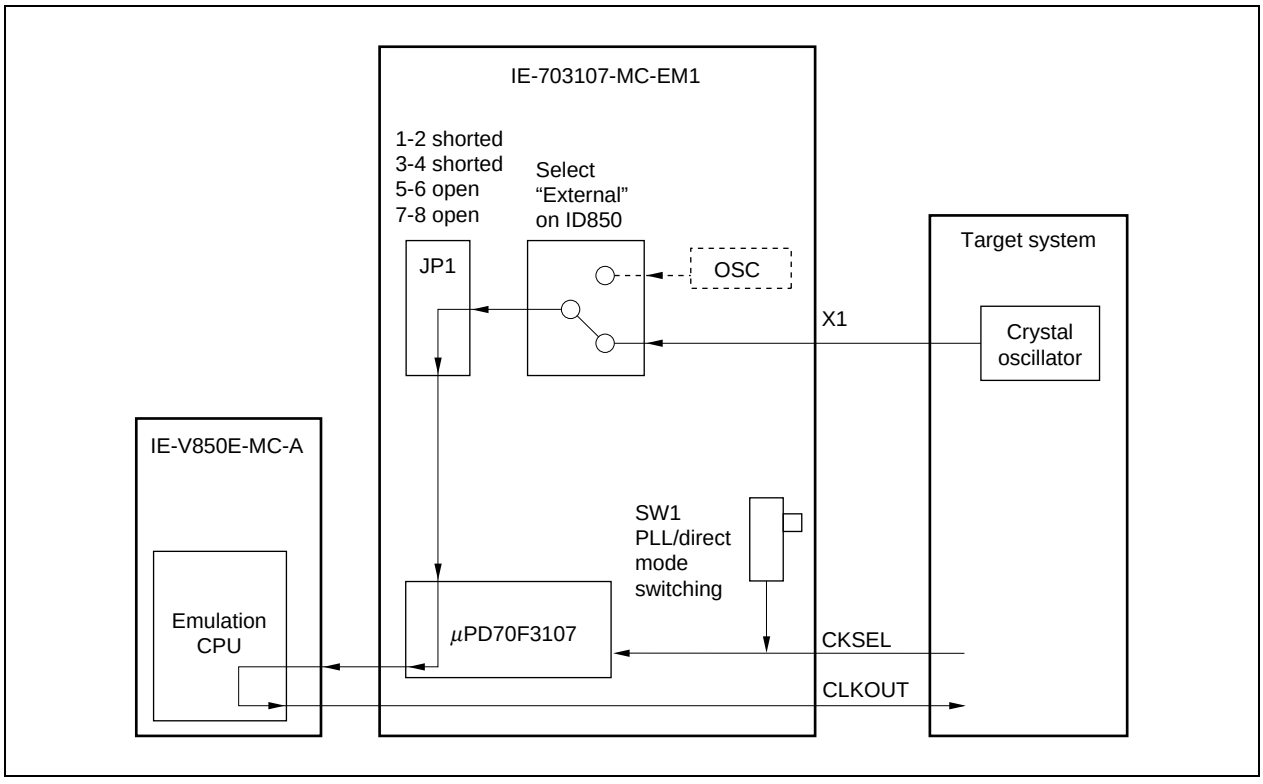
Table 2-4. Settings When Using External Clock

Type of Clock Used	Clock Source Selection	OSC Crystal Oscillator	JP1 Setting	Clock Mode	SW1	CKSEL Pin[Note]
Use crystal oscillator on target system as external clock.	External	Crystal oscillator can be either mounted or not mounted		PLL		Low-level input
				Direct		High-level input

Note The input setting to the CKSEL pin is made only when a target system is connected.
Leave this pin open when operating the emulator on a stand-alone basis. The emulator operates according to the setting of SW1.

Caution Be sure to input a square wave to the X1 pin.
When a clock generated by a crystal/ceramic resonator is used, the IE-703107-MC-EM1 does not operate.

Figure 2-5. Outline When Using Crystal Oscillator on Target System as External Clock



★ 2.3 Operation Mode Settings

The IE-703107-MC-EM1 supports the following operation modes equivalent to those of the actual device. These operation modes are selected on the debugger.

Target Device	Operation Mode	Selection in ID850[Note]
V850E/MA1	Single-chip mode 0	MODE00
	Single-chip mode 1	MODE01
	ROMless mode 0	MODE02
	ROMless mode 1	MODE03
V850E/MA2	ROMless mode 0	MODE00
	ROMless mode 1	MODE01

Note Make settings in accordance with the operation mode to be used in the mask setting area of the configuration dialog box that opens when the debugger (ID850) is started.

Caution To operate the emulator in the ROMless mode, be sure to map the emulation memory or the memory on the target system from address 0H.

Note that the IE-703107-MC-EM1 cannot emulate the MODE pin because the level input to the MODE pin is realized by the pin mask function of the debugger.
For how to set the pins on the target system, refer to the **V850E/MA1 Hardware User's Manual (U14359E)** or **V850E/MA2 Hardware User's Manual (U14980E)**.

2.4 Power Supply Settings

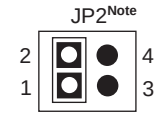
The power supply (V_{DD}) is set by using JP2.

★ 2.4.1 JP2 setting when emulator operates as stand-alone unit

When JP2 is set as shown in Figure 2-6, the IE-703107-MC-EM1 detects the power on the target system side and automatically selects whether V_{DD} is supplied from the internal power supply of the emulator or from the target system (with the default settings).

Caution If the JP2 setting is incorrect, the emulator may be damaged.

★ **Figure 2-6. Setting of JP2 (for Automatic Selection of Power)**

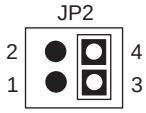


Set to 1-2 shorted, 3-4 open

Note A relay is used for power selection. Depending on the combination with the target system, the relay repeatedly turns ON/OFF when the power to the target system is turned OFF, issuing a sound continuously. In this case, make the setting shown in Figure 2-7.

Caution If the JP2 setting is incorrect, the emulator may be damaged.

★ **Figure 2-7. Setting of JP2 (to Use Power from Target System)**



Set to 1-2 open, 3-4 shorted

Figure 2-7 shows the setting of JP2 to supply power from the target system to V_{DD}.
With this setting, however, note that the emulator does not operate when the target system is not connected.

★ 2.5 Emulation Memory

This is a substitute memory used to emulate the memory or memory mapped I/O on the target system (capacity: 4 MB).

The emulation memory is mounted on the IE-703107-MC-EM1.

2.5.1 Wait setting for emulation memory

The data wait, address wait, and idle state for the emulation memory are set as follows.

(1) ID850

Select from the following three types on the configuration screen.

Selection	Wait Type	Emulation Memory Access	External Memory Access
WAIT MASK	Data wait	Fixed to 0 waits	Depends on DWC0/1 register setting WAIT signal masked
	Address wait	Fixed to 0 waits	Depends on ASC register setting
	Idle state	Fixed to 0 cycles	Depends on BCC register setting
1 WAIT ACCESS	Data wait	Fixed to 1 wait	Depends on DWC0/1 register setting and WAIT signal status
	Address wait	Fixed to 0 waits	Depends on ASC register setting
	Idle state	Fixed to 0 cycles	Depends on BCC register setting
TARGET WAIT	Data wait	Depends on DWC0/1 register setting However, 1 wait when set to 0 waits	Depends on DWC0/1 register setting and WAIT signal status
	Address wait	Fixed to 0 waits	Depends on ASC register setting
	Idle state	Depends on BCC register setting	Depends on BCC register setting

(2) MULTI

Select mask or unmask for WAIT and EMWAIT using the “Pinmask” command.

Selection	Wait Type	Emulation Memory Access	External Memory Access
WAIT: Mask EMWAIT: Mask	Data wait	Fixed to 0 waits	Depends on DWC0/1 register setting WAIT signal masked
	Address wait	Fixed to 0 waits	Depends on ASC register setting
	Idle state	Fixed to 0 cycles	Depends on BCC register setting
WAIT: Unmask EMWAIT: Mask	Data wait	Fixed to 1 wait	Depends on DWC0/1 register setting and WAIT signal status
	Address wait	Fixed to 0 waits	Depends on ASC register setting
	Idle state	Fixed to 0 cycles	Depends on BCC register setting
WAIT: Unmask EMWAIT: Unmask	Data wait	Depends on DWC0/1 register setting However, 1 wait when set to 0 waits	Depends on DWC0/1 register setting and WAIT signal status
	Address wait	Fixed to 0 waits	Depends on ASC register setting
	Idle state	Depends on BCC register setting	Depends on BCC register setting

2.5.2 Cautions related to emulation memory

(1) Number of data waits required for emulation memory access

The number of data waits required to be inserted for emulation memory access varies depending on the operating frequency of the emulator.

4 MHz ≤ Operating frequency < 25 MHz	0 waits
25 MHz ≤ Operating frequency ≤ 40 MHz	1 wait
40 MHz < Operating frequency	2 waits

(2) Bus sizing

Make the bus sizing 16 bits (set BSn0 of BSC register to 1).

An 8-bit bus cannot be used.

(3) $\overline{\text{WAIT}}$ pin

The number of data waits for the emulation memory is not affected by the $\overline{\text{WAIT}}$ pin.

(4) Address wait

Address waits cannot be inserted in the emulation memory.

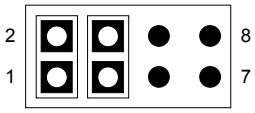
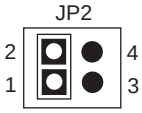
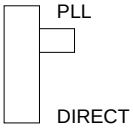
When address waits need to be inserted, set as follows.

Number of data waits for CS space of emulation memory	=	Number of address waits for external memory or external I/O	+	Number of data waits for external memory or external I/O

This setting is effective to make the access speed to the emulation memory equal to that of the external memory or external I/O to measure the performance, etc.

For how to insert waits in the emulation memory, refer to **2.5.1 Wait setting for emulation memory**.

CHAPTER 3 FACTORY SETTINGS

Item	Setting	Remark
JP1		All settings other than those set in the factory are prohibited.
★ JP2		Detects the power of the target system and automatically selects whether V_{DD} is supplied from the internal power supply of the emulator or from the target system.
SW1		Set to PLL mode.
★ OSC	5.000 MHz crystal oscillator is mounted.	The frequency can be varied by replacing the crystal oscillator.

CHAPTER 4 CAUTIONS

★ 4.1 Cautions on Terminating Pins

The pins that perform special processing in the emulator are explained below.

For detailed circuit configuration, refer to **CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS**.

(1) Pins that cannot be emulated

The following pins cannot be emulated because they are left open inside the emulator or connected to 3.3 V or GND via resistor. Evaluate these pins by using the target device.

Table 4-1. Pins That Cannot Be Emulated

Pin Name 1	Target Device	Pin No.
MODE0	V850E/MA1 (144-pin LQFP)	58
	V850E/MA1 (161-pin FBGA)	M8
	V850E/MA2 (100-pin LQFP)	36
MODE1	V850E/MA1 (144-pin LQFP)	57
	V850E/MA1 (161-pin FBGA)	P8
	V850E/MA2 (100-pin LQFP)	35
MODE2	V850E/MA1 (144-pin LQFP)	18
	V850E/MA1 (161-pin FBGA)	G1
	V850E/MA2 (100-pin LQFP)	21
X2	V850E/MA1 (144-pin LQFP)	62
	V850E/MA1 (161-pin FBGA)	N9
	V850E/MA2 (100-pin LQFP)	40
CV_{DD}	V850E/MA1 (144-pin LQFP)	61
	V850E/MA1 (161-pin FBGA)	P9
	V850E/MA2 (100-pin LQFP)	39

(2) X1 pin

The X1 pin is pulled down using 33 kΩ when an external clock is selected.

Because the external clock is input to the clock generator via 74HC157, a delay time of up to 13.2 ns is generated.

This pin is pulled down using 33 kΩ and is left open when the internal clock is selected.

(3) CKSEL pin

The CKSEL pin can be pulled up or down, depending on the setting of SW1.

It is pulled down using 33 kΩ when “PLL” is selected by SW1. This pin is pulled up using 33 kΩ when “DIRECT” is selected.

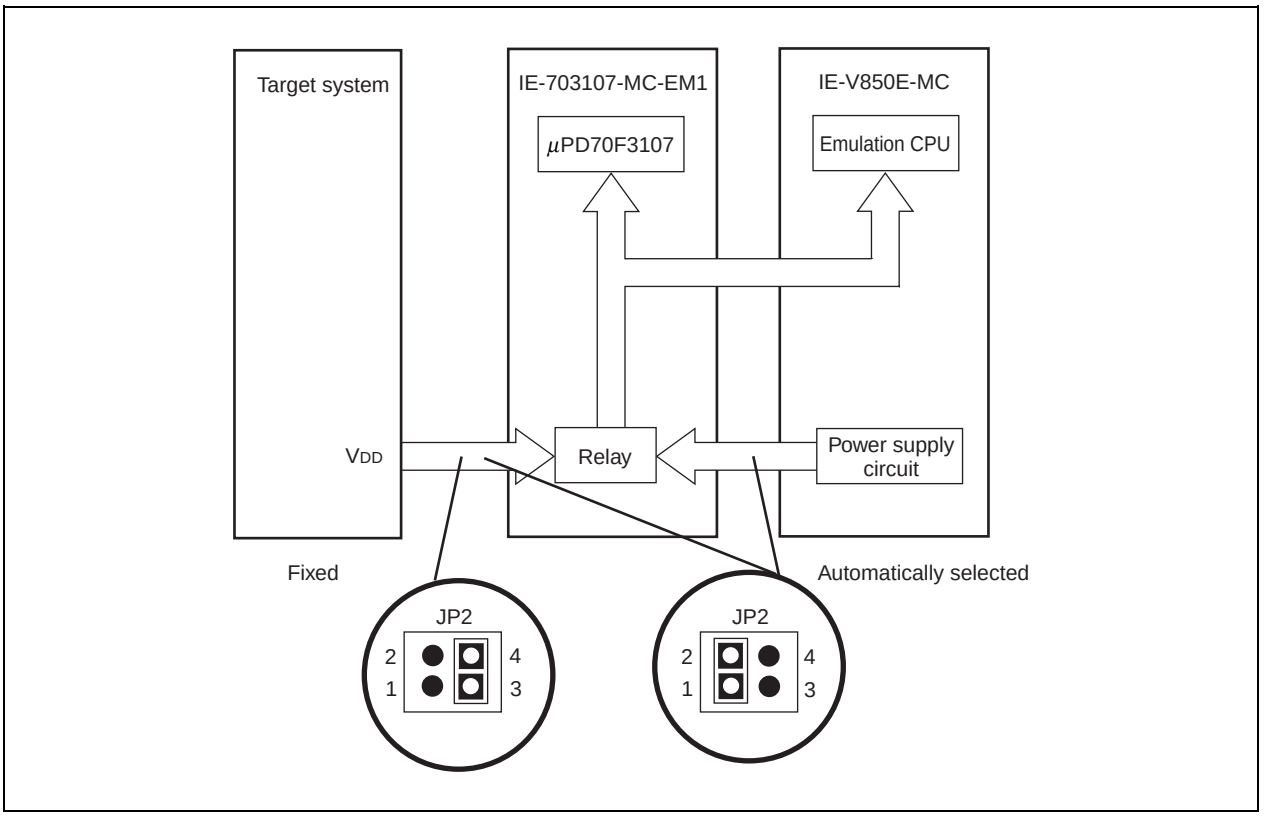
(4) V_{DD} pin

<1> V_{DD} in the target system is used to operate the circuits in the emulator.

When pins 1 and 2 of JP2 are shorted, and 3 and 4 are left open, the emulator detects V_{DD} of the target system and automatically selects whether V_{DD} of the target system or the internal power supply of the emulator is to be used.

<2> When pins 1 and 2 of JP2 are left open, and 3 and 4 are shorted, the emulator always uses V_{DD} from the target system. With this setting of JP2, the emulator does not operate if the target system is not connected. However, sneaking of power can be avoided.

★ **Figure 4-1. Schematic Diagram of Power Supply Flow**



★ 4.2 Notes on Internal RAM

The emulator maps the internal RAM to a 12 KB space of 0xFFFC000 to 0xFFFEFFF.

V850E/MA1 (internal RAM: 4 KB): 0xFFFC000 to 0xFFFCFFF

V850E/MA1 (internal RAM: 10 KB): 0xFFFC000 to 0xFFFE7FF

V850E/MA2 (internal RAM: 4 KB): 0xFFFC000 to 0xFFFCFFF

The target device is mapped as shown above. Consequently, the higher 8 KB space (0xFFFD000 to 0xFFFEFFF) or higher 2 KB space (0xFFFE800 to 0xFFFEFFF) of the emulator's 12 KB internal RAM area does not exist in the target device.

If the higher 8 KB or 2 KB space is accessed, the emulator cannot issue a fail-safe break. It is therefore necessary to set an access break in advance.

★ CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter shows the internal equivalent circuits of the emulator signals to be connected to the target system. Some pins cannot be emulated because of the internal processing of the emulator (refer to **CHAPTER 4 CAUTIONS**).

The equivalent circuits are shown in Figures 5-1 to 5-10.

Tables 5-1 to 5-10 show lists of the pins corresponding to the respective equivalent circuits.

Figure 5-1. Pin Equivalent Circuit 1

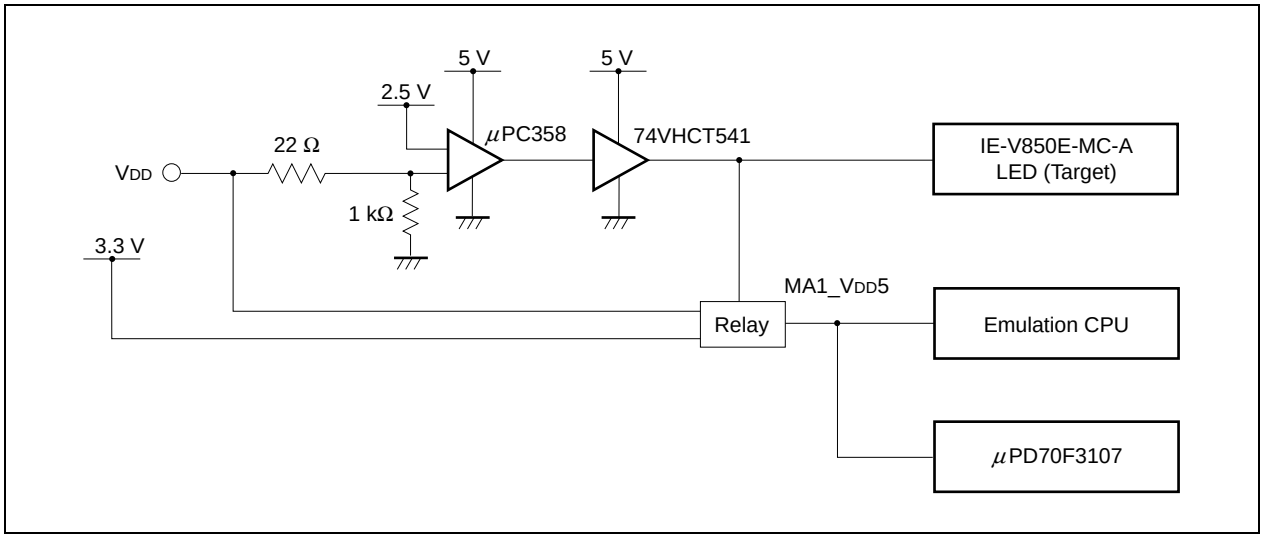


Table 5-1. Corresponding Pin List (Pin Equivalent Circuit 1)

Pin Name 1	Target Device	Pin No.
V_{DD}	V850E/MA1 (144-pin LQFP)	8, 27, 37, 47, 81, 98, 112, 124, 134
	V850E/MA1 (161-pin FBGA)	A12, C6, C8, F4, L6, F12, J3, K14, P1
	V850E/MA2 (100-pin LQFP)	11, 33, 55, 83, 93

Figure 5-2. Pin Equivalent Circuit 2

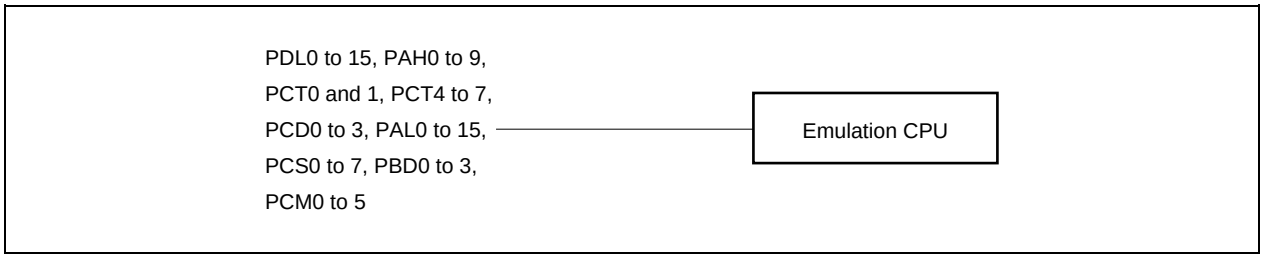


Table 5-2. Corresponding Pin List (Pin Equivalent Circuit 2) (1/5)

Pin Name 1	Pin Name 2	Pin Name 3	Pin Name 4	Target Device	Pin No.
PDL0	D0	–	–	V850E/MA1 (144-pin LQFP)	17
				V850E/MA1 (161-pin FBGA)	G3
				V850E/MA2 (100-pin LQFP)	20
PDL1	D1	–	–	V850E/MA1 (144-pin LQFP)	16
				V850E/MA1 (161-pin FBGA)	H4
				V850E/MA2 (100-pin LQFP)	19
PDL2	D2	–	–	V850E/MA1 (144-pin LQFP)	15
				V850E/MA1 (161-pin FBGA)	F1
				V850E/MA2 (100-pin LQFP)	18
PDL3	D3	–	–	V850E/MA1 (144-pin LQFP)	14
				V850E/MA1 (161-pin FBGA)	F2
				V850E/MA2 (100-pin LQFP)	17
PDL4	D4	–	–	V850E/MA1 (144-pin LQFP)	13
				V850E/MA1 (161-pin FBGA)	F3
				V850E/MA2 (100-pin LQFP)	16
PDL5	D5	–	–	V850E/MA1 (144-pin LQFP)	12
				V850E/MA1 (161-pin FBGA)	E1
				V850E/MA2 (100-pin LQFP)	15
PDL6	D6	–	–	V850E/MA1 (144-pin LQFP)	11
				V850E/MA1 (161-pin FBGA)	G4
				V850E/MA2 (100-pin LQFP)	14
PDL7	D7	–	–	V850E/MA1 (144-pin LQFP)	10
				V850E/MA1 (161-pin FBGA)	E2
				V850E/MA2 (100-pin LQFP)	13
PDL8	D8	–	–	V850E/MA1 (144-pin LQFP)	7
				V850E/MA1 (161-pin FBGA)	E3
				V850E/MA2 (100-pin LQFP)	10
PDL9	D9	–	–	V850E/MA1 (144-pin LQFP)	6
				V850E/MA1 (161-pin FBGA)	C2
				V850E/MA2 (100-pin LQFP)	9
PDL10	D10	–	–	V850E/MA1 (144-pin LQFP)	5
				V850E/MA1 (161-pin FBGA)	D2
				V850E/MA2 (100-pin LQFP)	8
PDL11	D11	–	–	V850E/MA1 (144-pin LQFP)	4
				V850E/MA1 (161-pin FBGA)	E4
				V850E/MA2 (100-pin LQFP)	7
PDL12	D12	–	–	V850E/MA1 (144-pin LQFP)	3
				V850E/MA1 (161-pin FBGA)	B2
				V850E/MA2 (100-pin LQFP)	6
PDL13	D13	–	–	V850E/MA1 (144-pin LQFP)	2
				V850E/MA1 (161-pin FBGA)	C3
				V850E/MA2 (100-pin LQFP)	5

Table 5-2. Corresponding Pin List (Pin Equivalent Circuit 2) (2/5)

Pin Name 1	Pin Name 2	Pin Name 3	Pin Name 4	Target Device	Pin No.
PDL14	D14	–	–	V850E/MA1 (144-pin LQFP)	1
				V850E/MA1 (161-pin FBGA)	D3
				V850E/MA2 (100-pin LQFP)	4
PDL15	D15	–	–	V850E/MA1 (144-pin LQFP)	144
				V850E/MA1 (161-pin FBGA)	A2
				V850E/MA2 (100-pin LQFP)	3
PAH0	A16	–	–	V850E/MA1 (144-pin LQFP)	123
				V850E/MA1 (161-pin FBGA)	D8
				V850E/MA2 (100-pin LQFP)	82
PAH1	A17	–	–	V850E/MA1 (144-pin LQFP)	122
				V850E/MA1 (161-pin FBGA)	A9
				V850E/MA2 (100-pin LQFP)	81
PAH2	A18	–	–	V850E/MA1 (144-pin LQFP)	121
				V850E/MA1 (161-pin FBGA)	B9
				V850E/MA2 (100-pin LQFP)	80
PAH3	A19	–	–	V850E/MA1 (144-pin LQFP)	120
				V850E/MA1 (161-pin FBGA)	C9
				V850E/MA2 (100-pin LQFP)	79
PAH4	A20	–	–	V850E/MA1 (144-pin LQFP)	119
				V850E/MA1 (161-pin FBGA)	D9
				V850E/MA2 (100-pin LQFP)	78
PAH5	A21	–	–	V850E/MA1 (144-pin LQFP)	118
				V850E/MA1 (161-pin FBGA)	B10
				V850E/MA2 (100-pin LQFP)	77
PAH6	A22	–	–	V850E/MA1 (144-pin LQFP)	117
				V850E/MA1 (161-pin FBGA)	C10
				V850E/MA2 (100-pin LQFP)	76
PAH7	A23	–	–	V850E/MA1 (144-pin LQFP)	116
				V850E/MA1 (161-pin FBGA)	D10
				V850E/MA2 (100-pin LQFP)	75
PAH8	A24	–	–	V850E/MA1 (144-pin LQFP)	115
				V850E/MA1 (161-pin FBGA)	A11
				V850E/MA2 (100-pin LQFP)	74
PAH9	A25	–	–	V850E/MA1 (144-pin LQFP)	114
				V850E/MA1 (161-pin FBGA)	B11
				V850E/MA2 (100-pin LQFP)	–
PCT0	$\overline{\text{LCAS}}$	$\overline{\text{LWR}}$	LDQM	V850E/MA1 (144-pin LQFP)	97
				V850E/MA1 (161-pin FBGA)	F13
				V850E/MA2 (100-pin LQFP)	65
PCT1	$\overline{\text{UCAS}}$	$\overline{\text{UWR}}$	UDQM	V850E/MA1 (144-pin LQFP)	96
				V850E/MA1 (161-pin FBGA)	F14
				V850E/MA2 (100-pin LQFP)	64

Table 5-2. Corresponding Pin List (Pin Equivalent Circuit 2) (3/5)

Pin Name 1	Pin Name 2	Pin Name 3	Pin Name 4	Target Device	Pin No.
PCT4	$\overline{RD}$	–	–	V850E/MA1 (144-pin LQFP)	95
				V850E/MA1 (161-pin FBGA)	F11
				V850E/MA2 (100-pin LQFP)	63
PCT5	$\overline{WE}$	–	–	V850E/MA1 (144-pin LQFP)	94
				V850E/MA1 (161-pin FBGA)	G12
				V850E/MA2 (100-pin LQFP)	62
PCT6	$\overline{OE}$	–	–	V850E/MA1 (144-pin LQFP)	93
				V850E/MA1 (161-pin FBGA)	G14
				V850E/MA2 (100-pin LQFP)	–
PCT7	$\overline{BCYST}$	–	–	V850E/MA1 (144-pin LQFP)	92
				V850E/MA1 (161-pin FBGA)	G13
				V850E/MA2 (100-pin LQFP)	–
PCD0	SDCKE	–	–	V850E/MA1 (144-pin LQFP)	111
				V850E/MA1 (161-pin FBGA)	D11
				V850E/MA2 (100-pin LQFP)	73
PCD1	SDCLK	–	–	V850E/MA1 (144-pin LQFP)	110
				V850E/MA1 (161-pin FBGA)	B12
				V850E/MA2 (100-pin LQFP)	72
PCD2	$\overline{LBE}$	$\overline{SDCAS}$	–	V850E/MA1 (144-pin LQFP)	109
				V850E/MA1 (161-pin FBGA)	A13
				V850E/MA2 (100-pin LQFP)	71
PCD3	$\overline{UBE}$	$\overline{SDRAS}$	–	V850E/MA1 (144-pin LQFP)	108
				V850E/MA1 (161-pin FBGA)	A14
				V850E/MA2 (100-pin LQFP)	70
PAL0	A0	–	–	V850E/MA1 (144-pin LQFP)	143
				V850E/MA1 (161-pin FBGA)	B3
				V850E/MA2 (100-pin LQFP)	2
PAL1	A1	–	–	V850E/MA1 (144-pin LQFP)	142
				V850E/MA1 (161-pin FBGA)	C4
				V850E/MA2 (100-pin LQFP)	1
PAL2	A2	–	–	V850E/MA1 (144-pin LQFP)	141
				V850E/MA1 (161-pin FBGA)	A3
				V850E/MA2 (100-pin LQFP)	100
PAL3	A3	–	–	V850E/MA1 (144-pin LQFP)	140
				V850E/MA1 (161-pin FBGA)	D4
				V850E/MA2 (100-pin LQFP)	99
PAL4	A4	–	–	V850E/MA1 (144-pin LQFP)	139
				V850E/MA1 (161-pin FBGA)	B4
				V850E/MA2 (100-pin LQFP)	98
PAL5	A5	–	–	V850E/MA1 (144-pin LQFP)	138
				V850E/MA1 (161-pin FBGA)	A4
				V850E/MA2 (100-pin LQFP)	97

Table 5-2. Corresponding Pin List (Pin Equivalent Circuit 2) (4/5)

Pin Name 1	Pin Name 2	Pin Name 3	Pin Name 4	Target Device	Pin No.
PAL6	A6	–	–	V850E/MA1 (144-pin LQFP)	137
				V850E/MA1 (161-pin FBGA)	D5
				V850E/MA2 (100-pin LQFP)	96
PAL7	A7	–	–	V850E/MA1 (144-pin LQFP)	136
				V850E/MA1 (161-pin FBGA)	C5
				V850E/MA2 (100-pin LQFP)	95
PAL8	A8	–	–	V850E/MA1 (144-pin LQFP)	133
				V850E/MA1 (161-pin FBGA)	B6
				V850E/MA2 (100-pin LQFP)	92
PAL9	A9	–	–	V850E/MA1 (144-pin LQFP)	132
				V850E/MA1 (161-pin FBGA)	A6
				V850E/MA2 (100-pin LQFP)	91
PAL10	A10	–	–	V850E/MA1 (144-pin LQFP)	131
				V850E/MA1 (161-pin FBGA)	D6
				V850E/MA2 (100-pin LQFP)	90
PAL11	A11	–	–	V850E/MA1 (144-pin LQFP)	130
				V850E/MA1 (161-pin FBGA)	C7
				V850E/MA2 (100-pin LQFP)	89
PAL12	A12	–	–	V850E/MA1 (144-pin LQFP)	129
				V850E/MA1 (161-pin FBGA)	A7
				V850E/MA2 (100-pin LQFP)	88
PAL13	A13	–	–	V850E/MA1 (144-pin LQFP)	128
				V850E/MA1 (161-pin FBGA)	B7
				V850E/MA2 (100-pin LQFP)	87
PAL14	A14	–	–	V850E/MA1 (144-pin LQFP)	127
				V850E/MA1 (161-pin FBGA)	D7
				V850E/MA2 (100-pin LQFP)	86
PAL15	A15	–	–	V850E/MA1 (144-pin LQFP)	126
				V850E/MA1 (161-pin FBGA)	A8
				V850E/MA2 (100-pin LQFP)	85
PCS0	–	–	–	V850E/MA1 (144-pin LQFP)	107
				V850E/MA1 (161-pin FBGA)	D12
				V850E/MA2 (100-pin LQFP)	69
PCS1	–	–	–	V850E/MA1 (144-pin LQFP)	106
				V850E/MA1 (161-pin FBGA)	B13
				V850E/MA2 (100-pin LQFP)	–
PCS2	–	–	–	V850E/MA1 (144-pin LQFP)	105
				V850E/MA1 (161-pin FBGA)	C13
				V850E/MA2 (100-pin LQFP)	–
PCS3	–	–	–	V850E/MA1 (144-pin LQFP)	104
				V850E/MA1 (161-pin FBGA)	C12
				V850E/MA2 (100-pin LQFP)	68

Table 5-2. Corresponding Pin List (Pin Equivalent Circuit 2) (5/5)

Pin Name 1	Pin Name 2	Pin Name 3	Pin Name 4	Target Device	Pin No.
PCS4	–	–	–	V850E/MA1 (144-pin LQFP)	103
				V850E/MA1 (161-pin FBGA)	E12
				V850E/MA2 (100-pin LQFP)	67
PCS5	–	–	–	V850E/MA1 (144-pin LQFP)	102
				V850E/MA1 (161-pin FBGA)	D13
				V850E/MA2 (100-pin LQFP)	–
PCS6	–	–	–	V850E/MA1 (144-pin LQFP)	101
				V850E/MA1 (161-pin FBGA)	E11
				V850E/MA2 (100-pin LQFP)	–
PCS7	–	–	–	V850E/MA1 (144-pin LQFP)	100
				V850E/MA1 (161-pin FBGA)	E13
				V850E/MA2 (100-pin LQFP)	66
PBD0	DMAAK0	–	–	V850E/MA1 (144-pin LQFP)	32
				V850E/MA1 (161-pin FBGA)	L4
				V850E/MA2 (100-pin LQFP)	28
PBD1	DMAAK1	–	–	V850E/MA1 (144-pin LQFP)	31
				V850E/MA1 (161-pin FBGA)	K3
				V850E/MA2 (100-pin LQFP)	27
PBD2	DMAAK2	–	–	V850E/MA1 (144-pin LQFP)	30
				V850E/MA1 (161-pin FBGA)	L2
				V850E/MA2 (100-pin LQFP)	–
PBD3	DMAAK3	–	–	V850E/MA1 (144-pin LQFP)	29
				V850E/MA1 (161-pin FBGA)	K4
				V850E/MA2 (100-pin LQFP)	–
PCM0	$\overline{\text{WAIT}}$	–	–	V850E/MA1 (144-pin LQFP)	91
				V850E/MA1 (161-pin FBGA)	G11
				V850E/MA2 (100-pin LQFP)	61
PCM1	CLKOUT	BUSCLK	–	V850E/MA1 (144-pin LQFP)	90
				V850E/MA1 (161-pin FBGA)	H14
				V850E/MA2 (100-pin LQFP)	60
PCM2	$\overline{\text{HLDAK}}$	–	–	V850E/MA1 (144-pin LQFP)	89
				V850E/MA1 (161-pin FBGA)	H13
				V850E/MA2 (100-pin LQFP)	59
PCM3	$\overline{\text{HLDRQ}}$	–	–	V850E/MA1 (144-pin LQFP)	88
				V850E/MA1 (161-pin FBGA)	H13
				V850E/MA2 (100-pin LQFP)	58
PCM4	$\overline{\text{REFRQ}}$	–	–	V850E/MA1 (144-pin LQFP)	87
				V850E/MA1 (161-pin FBGA)	H11
				V850E/MA2 (100-pin LQFP)	57
PCM5	SELFRQ	–	–	V850E/MA1 (144-pin LQFP)	86
				V850E/MA1 (161-pin FBGA)	J13
				V850E/MA2 (100-pin LQFP)	–

Figure 5-3. Pin Equivalent Circuit 3

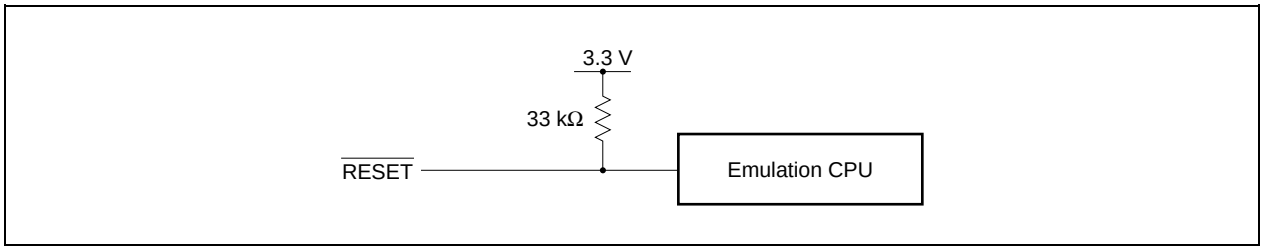


Table 5-3. Corresponding Pin List (Pin Equivalent Circuit 3)

Pin Name 1	Target Device	Pin No.
$\overline{\text{RESET}}$	V850E/MA1 (144-pin LQFP)	59
	V850E/MA1 (161-pin FBGA)	L9
	V850E/MA2 (100-pin LQFP)	37

Figure 5-4. Pin Equivalent Circuit 4

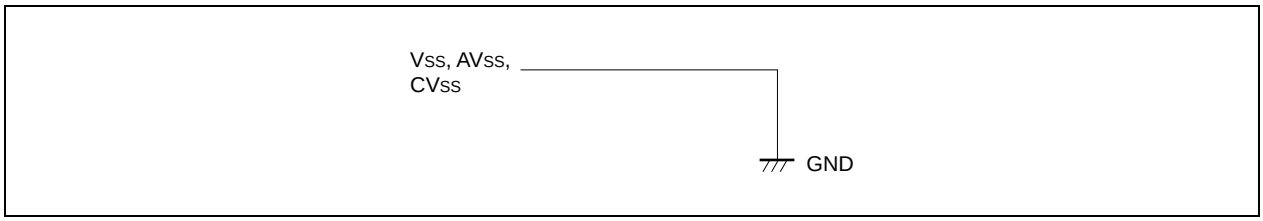


Table 5-4. Corresponding Pin List (Pin Equivalent Circuit 4)

Pin Name 1	Target Device	Pin No.
V_{SS}	V850E/MA1 (144-pin LQFP)	9, 28, 113, 125, 135, 48, 38, 99, 82
	V850E/MA1 (161-pin FBGA)	B5, B8, C11, D1, E14, K2, K13, M6, P2
	V850E/MA2 (100-pin LQFP)	12, 34, 56, 84, 94
AV_{SS0}	V850E/MA1 (144-pin LQFP)	72
	V850E/MA1 (161-pin FBGA)	N13
	V850E/MA2 (100-pin LQFP)	50
CV_{SS}	V850E/MA1 (144-pin LQFP)	64
	V850E/MA1 (161-pin FBGA)	N10
	V850E/MA2 (100-pin LQFP)	42

Figure 5-5. Pin Equivalent Circuit 5

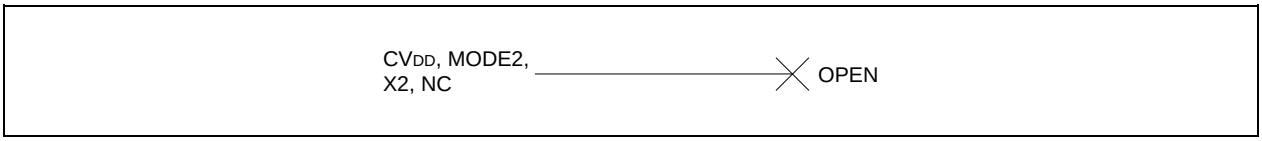


Table 5-5. Corresponding Pin List (Pin Equivalent Circuit 5)

Pin Name 1	Pin Name 2	Package	Pin No.
CV_{DD}	–	V850E/MA1 (144-pin LQFP)	61
		V850E/MA1 (161-pin FBGA)	P9
		V850E/MA2 (100-pin LQFP)	39
MODE2	V_{PP}	V850E/MA1 (144-pin LQFP)	18
		V850E/MA1 (161-pin FBGA)	G1
		V850E/MA2 (100-pin LQFP)	–
X2	–	V850E/MA1 (144-pin LQFP)	62
		V850E/MA1 (161-pin FBGA)	N9
		V850E/MA2 (100-pin LQFP)	40
NC	–	V850E/MA1 (144-pin LQFP)	–
		V850E/MA1 (161-pin FBGA)	A1, A5, A10, B1, B14, C1, C14, D14, E5, L1, M1, M14, N1, N14, P5, P11, P14
		V850E/MA2 (100-pin LQFP)	–

Figure 5-6. Pin Equivalent Circuit 6

Table 5-6. Corresponding Pin List (Pin Equivalent Circuit 6) (1/4)

Pin Name 1	Pin Name 2	Pin Name 3	Target Device	Pin No.
P00	PWM0	–	V850E/MA1 (144-pin LQFP)	26
			V850E/MA1 (161-pin FBGA)	K1
			V850E/MA2 (100-pin LQFP)	–
P01	TI000	INTP000	V850E/MA1 (144-pin LQFP)	25
			V850E/MA1 (161-pin FBGA)	J2
			V850E/MA2 (100-pin LQFP)	26
P02	INTP001	–	V850E/MA1 (144-pin LQFP)	24
			V850E/MA1 (161-pin FBGA)	J4
			V850E/MA2 (100-pin LQFP)	25
P03	TO00	–	V850E/MA1 (144-pin LQFP)	23
			V850E/MA1 (161-pin FBGA)	J1
			V850E/MA2 (100-pin LQFP)	24

Table 5-6. Corresponding Pin List (Pin Equivalent Circuit 6) (2/4)

Pin Name 1	Pin Name 2	Pin Name 3	Target Device	Pin No.
P04	$\overline{\text{DMARQ0}}$	$\overline{\text{INTP100}}$	V850E/MA1 (144-pin LQFP)	22
			V850E/MA1 (161-pin FBGA)	H3
			V850E/MA2 (100-pin LQFP)	23
P05	$\overline{\text{DMARQ1}}$	$\overline{\text{INTP101}}$	V850E/MA1 (144-pin LQFP)	21
			V850E/MA1 (161-pin FBGA)	H2
			V850E/MA2 (100-pin LQFP)	22
P06	$\overline{\text{DMARQ2}}$	$\overline{\text{INTP102}}$	V850E/MA1 (144-pin LQFP)	20
			V850E/MA1 (161-pin FBGA)	H1
			V850E/MA2 (100-pin LQFP)	–
P07	$\overline{\text{DMARQ3}}$	$\overline{\text{INTP103}}$	V850E/MA1 (144-pin LQFP)	19
			V850E/MA1 (161-pin FBGA)	G2
			V850E/MA2 (100-pin LQFP)	–
P10	PWM1	–	V850E/MA1 (144-pin LQFP)	36
			V850E/MA1 (161-pin FBGA)	N2
			V850E/MA2 (100-pin LQFP)	–
P11	INTP020	TI010	V850E/MA1 (144-pin LQFP)	35
			V850E/MA1 (161-pin FBGA)	L3
			V850E/MA2 (100-pin LQFP)	30
P12	INTO011	–	V850E/MA1 (144-pin LQFP)	34
			V850E/MA1 (161-pin FBGA)	M2
			V850E/MA2 (100-pin LQFP)	29
P13	TO01	–	V850E/MA1 (144-pin LQFP)	33
			V850E/MA1 (161-pin FBGA)	M3
			V850E/MA2 (100-pin LQFP)	–
P20	NMI	–	V850E/MA1 (144-pin LQFP)	46
			V850E/MA1 (161-pin FBGA)	N5
			V850E/MA2 (100-pin LQFP)	32
P21	INTP020	TI020	V850E/MA1 (144-pin LQFP)	45
			V850E/MA1 (161-pin FBGA)	M5
			V850E/MA2 (100-pin LQFP)	–
P22	INTP021	–	V850E/MA1 (144-pin LQFP)	44
			V850E/MA1 (161-pin FBGA)	P4
			V850E/MA2 (100-pin LQFP)	–
P23	TO02	–	V850E/MA1 (144-pin LQFP)	43
			V850E/MA1 (161-pin FBGA)	L5
			V850E/MA2 (100-pin LQFP)	–
P24	$\overline{\text{TC0}}$	$\overline{\text{INTP110}}$	V850E/MA1 (144-pin LQFP)	42
			V850E/MA1 (161-pin FBGA)	N4
			V850E/MA2 (100-pin LQFP)	31
P25	$\overline{\text{TC1}}$	$\overline{\text{INTP111}}$	V850E/MA1 (144-pin LQFP)	41
			V850E/MA1 (161-pin FBGA)	P3
			V850E/MA2 (100-pin LQFP)	–

Table 5-6. Corresponding Pin List (Pin Equivalent Circuit 6) (3/4)

Pin Name 1	Pin Name 2	Pin Name 3	Target Device	Pin No.
P26	$\overline{TC2}$	$\overline{INTP112}$	V850E/MA1 (144-pin LQFP)	40
			V850E/MA1 (161-pin FBGA)	M4
			V850E/MA2 (100-pin LQFP)	–
P27	$\overline{TC3}$	$\overline{INTP113}$	V850E/MA1 (144-pin LQFP)	39
			V850E/MA1 (161-pin FBGA)	N3
			V850E/MA2 (100-pin LQFP)	–
AV_{DD}	AV_{REF}	–	V850E/MA1 (144-pin LQFP)	71
			V850E/MA1 (161-pin FBGA)	N12
			V850E/MA2 (100-pin LQFP)	49
P30	SO2	$\overline{INTP130}$	V850E/MA1 (144-pin LQFP)	56
			V850E/MA1 (161-pin FBGA)	N8
			V850E/MA2 (100-pin LQFP)	–
P31	SI2	$\overline{INTP131}$	V850E/MA1 (144-pin LQFP)	55
			V850E/MA1 (161-pin FBGA)	L8
			V850E/MA2 (100-pin LQFP)	–
P32	$\overline{SCK2}$	$\overline{INTP132}$	V850E/MA1 (144-pin LQFP)	54
			V850E/MA1 (161-pin FBGA)	P7
			V850E/MA2 (100-pin LQFP)	–
P33	TXD2	$\overline{INTP133}$	V850E/MA1 (144-pin LQFP)	53
			V850E/MA1 (161-pin FBGA)	N7
			V850E/MA2 (100-pin LQFP)	–
P34	RXD2	$\overline{INTP120}$	V850E/MA1 (144-pin LQFP)	52
			V850E/MA1 (161-pin FBGA)	M7
			V850E/MA2 (100-pin LQFP)	–
P35	$\overline{INTP121}$	–	V850E/MA1 (144-pin LQFP)	51
			V850E/MA1 (161-pin FBGA)	P6
			V850E/MA2 (100-pin LQFP)	–
P36	$\overline{INTP122}$	–	V850E/MA1 (144-pin LQFP)	50
			V850E/MA1 (161-pin FBGA)	L7
			V850E/MA2 (100-pin LQFP)	–
P37	ADTRG	INTP123	V850E/MA1 (144-pin LQFP)	49
			V850E/MA1 (161-pin FBGA)	N6
			V850E/MA2 (100-pin LQFP)	–
P40	TXD0	SO0	V850E/MA1 (144-pin LQFP)	70
			V850E/MA1 (161-pin FBGA)	M11
			V850E/MA2 (100-pin LQFP)	48
P41	RXD0	SI0	V850E/MA1 (144-pin LQFP)	69
			V850E/MA1 (161-pin FBGA)	P13
			V850E/MA2 (100-pin LQFP)	47
P42	$\overline{SCK0}$	–	V850E/MA1 (144-pin LQFP)	68
			V850E/MA1 (161-pin FBGA)	N11
			V850E/MA2 (100-pin LQFP)	46

Table 5-6. Corresponding Pin List (Pin Equivalent Circuit 6) (4/4)

Pin Name 1	Pin Name 2	Pin Name 3	Target Device	Pin No.
P43	TXD1	SC1	V850E/MA1 (144-pin LQFP)	67
			V850E/MA1 (161-pin FBGA)	L10
			V850E/MA2 (100-pin LQFP)	45
P44	RXD1	SI1	V850E/MA1 (144-pin LQFP)	66
			V850E/MA1 (161-pin FBGA)	P12
			V850E/MA2 (100-pin LQFP)	44
P45	$\overline{\text{SCK1}}$	–	V850E/MA1 (144-pin LQFP)	65
			V850E/MA1 (161-pin FBGA)	M10
			V850E/MA2 (100-pin LQFP)	43
P50	INTP030	TI30	V850E/MA1 (144-pin LQFP)	85
			V850E/MA1 (161-pin FBGA)	J12
			V850E/MA2 (100-pin LQFP)	–
P51	INTP031	–	V850E/MA1 (144-pin LQFP)	84
			V850E/MA1 (161-pin FBGA)	J14
			V850E/MA2 (100-pin LQFP)	–
P52	TO03	–	V850E/MA1 (144-pin LQFP)	83
			V850E/MA1 (161-pin FBGA)	J11
			V850E/MA2 (100-pin LQFP)	–
P70	ANI0	–	V850E/MA1 (144-pin LQFP)	80
			V850E/MA1 (161-pin FBGA)	K12
			V850E/MA2 (100-pin LQFP)	54
P71	ANI1	–	V850E/MA1 (144-pin LQFP)	79
			V850E/MA1 (161-pin FBGA)	K11
			V850E/MA2 (100-pin LQFP)	53
P72	ANI2	–	V850E/MA1 (144-pin LQFP)	78
			V850E/MA1 (161-pin FBGA)	L14
			V850E/MA2 (100-pin LQFP)	52
P73	ANI3	–	V850E/MA1 (144-pin LQFP)	77
			V850E/MA1 (161-pin FBGA)	L13
			V850E/MA2 (100-pin LQFP)	51
P74	ANI4	–	V850E/MA1 (144-pin LQFP)	76
			V850E/MA1 (161-pin FBGA)	L12
			V850E/MA2 (100-pin LQFP)	–
P75	ANI5	–	V850E/MA1 (144-pin LQFP)	75
			V850E/MA1 (161-pin FBGA)	M13
			V850E/MA2 (100-pin LQFP)	–
P76	ANI6	–	V850E/MA1 (144-pin LQFP)	74
			V850E/MA1 (161-pin FBGA)	M12
			V850E/MA2 (100-pin LQFP)	–
P77	ANI7	–	V850E/MA1 (144-pin LQFP)	73
			V850E/MA1 (161-pin FBGA)	L11
			V850E/MA2 (100-pin LQFP)	–

Figure 5-7. Pin Equivalent Circuit 7

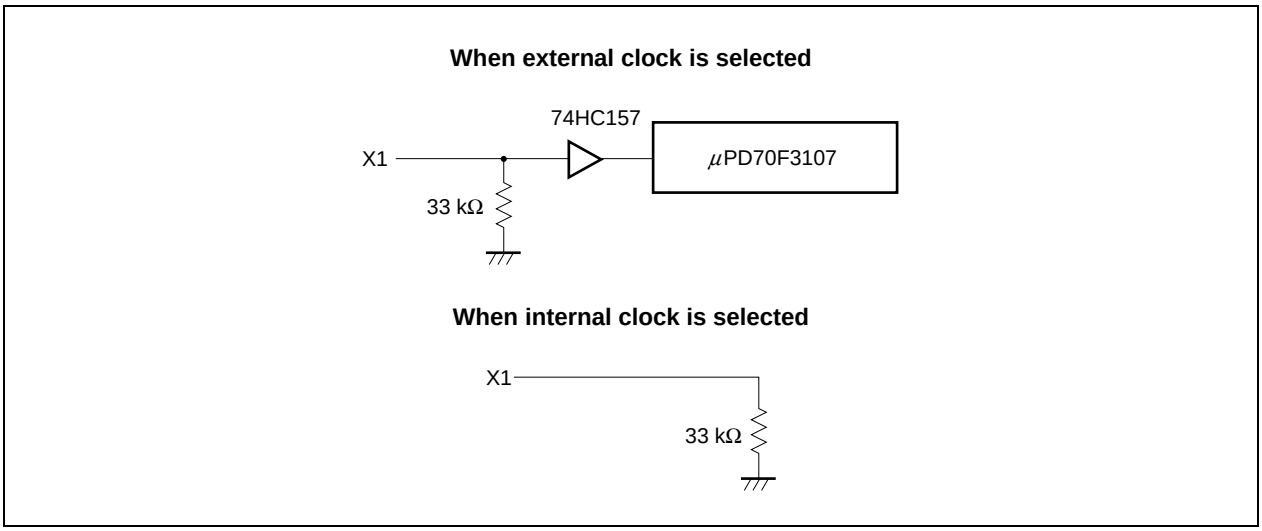


Table 5-7. Corresponding Pin List (Pin Equivalent Circuit 7)

Pin Name 1	Package	Pin No.
X1	V850E/MA1 (144-pin LQFP)	63
	V850E/MA1 (161-pin FBGA)	P10
	V850E/MA2 (100-pin LQFP)	41

Figure 5-8. Pin Equivalent Circuit 8

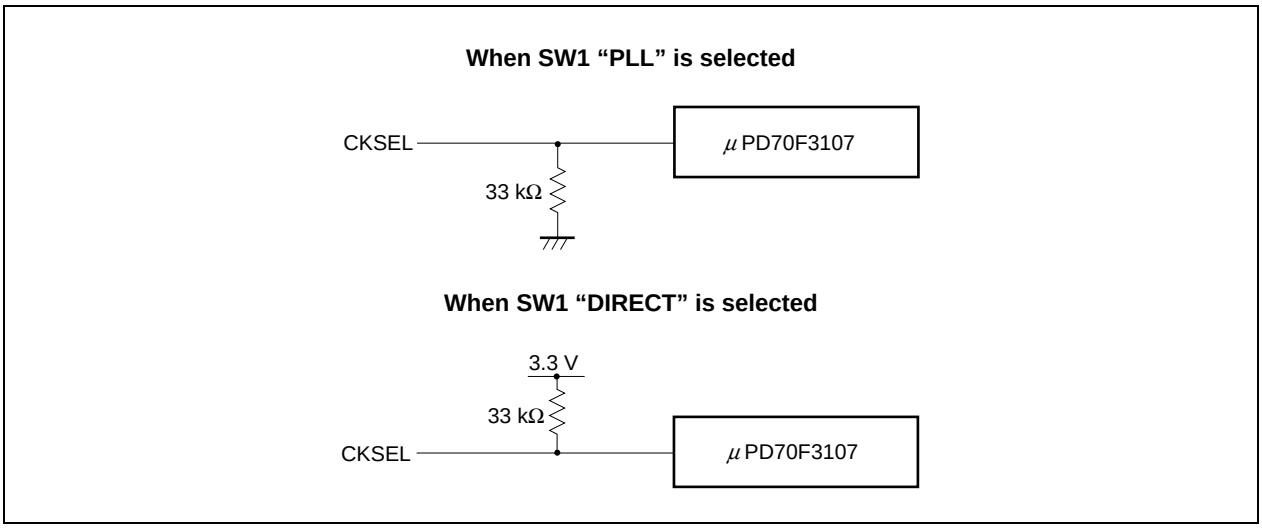


Table 5-8. Corresponding Pin List (Pin Equivalent Circuit 8)

Pin Name 1	Package	Pin No.
CKSEL	V850E/MA1 (144-pin LQFP)	60
	V850E/MA1 (161-pin FBGA)	M9
	V850E/MA2 (100-pin LQFP)	38

Figure 5-9. Pin Equivalent Circuit 9

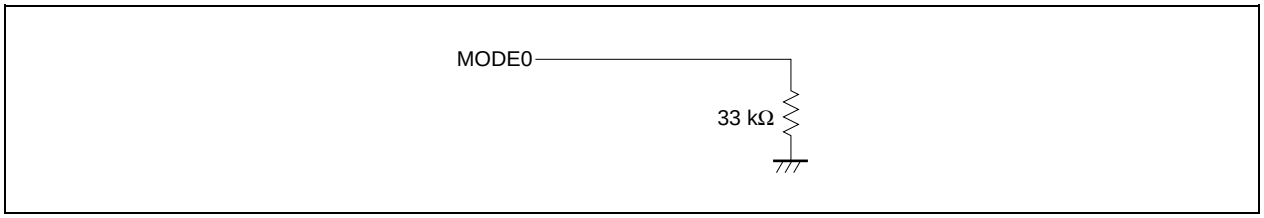


Table 5-9. Corresponding Pin List (Pin Equivalent Circuit 9)

Pin Name 1	Package	Pin No.
MODE0	V850E/MA1 (144-pin LQFP)	58
	V850E/MA1 (161-pin FBGA)	M8
	V850E/MA2 (100-pin LQFP)	36

Figure 5-10. Pin Equivalent Circuit 10

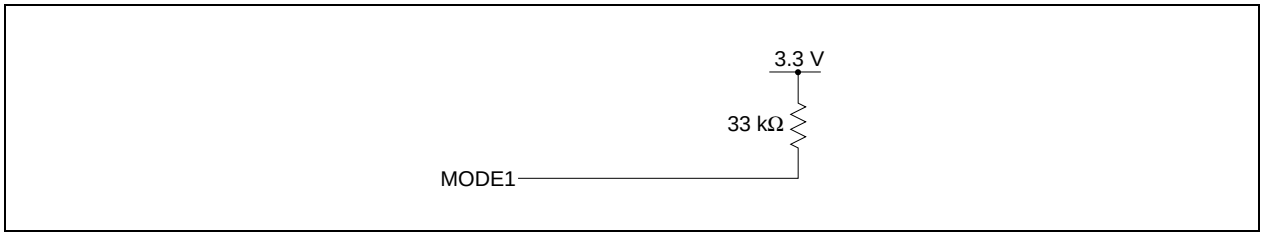


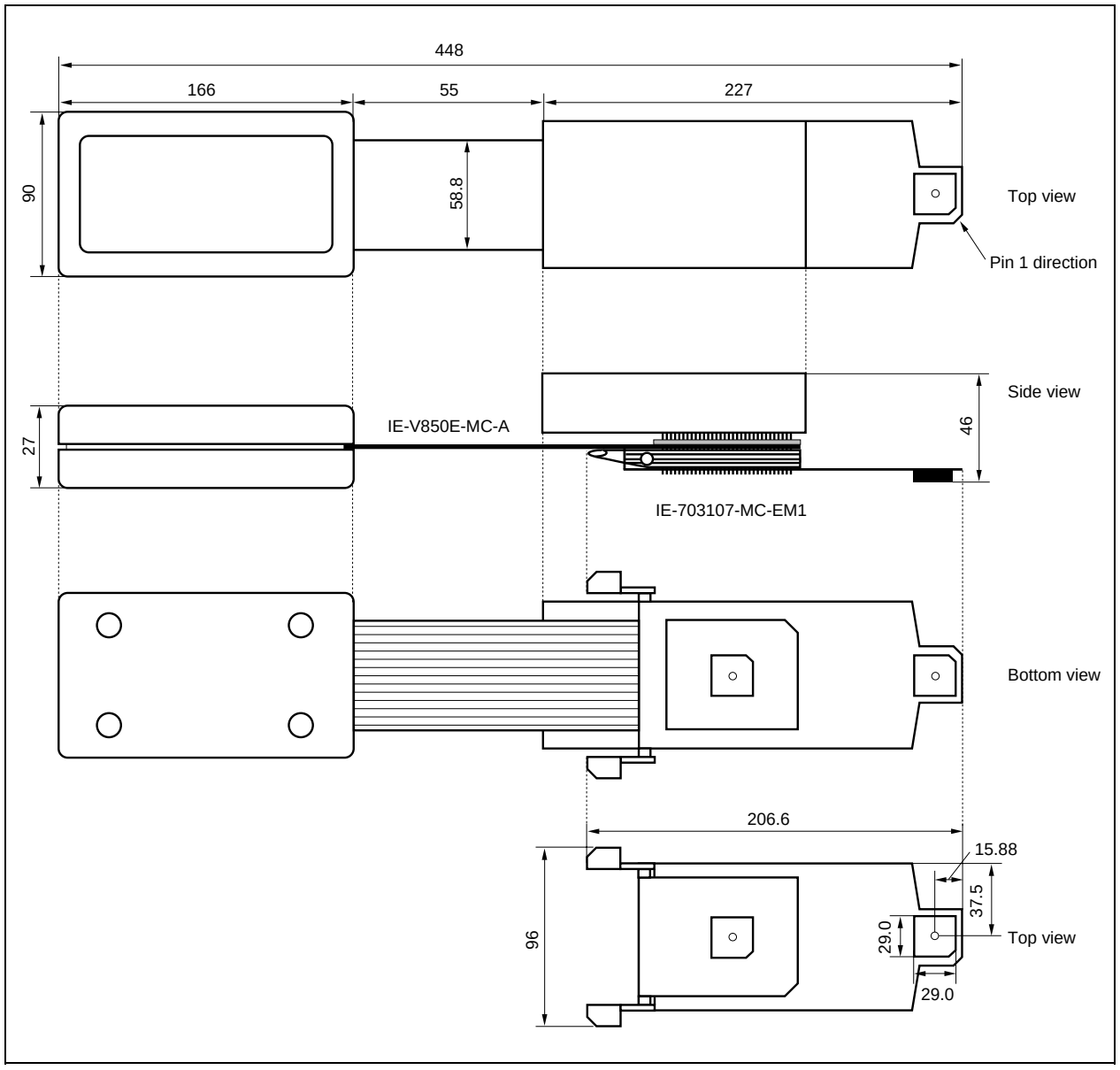
Table 5-10. Corresponding Pin List (Pin Equivalent Circuit 10)

Pin Name 1	Package	Pin No.
MODE1	V850E/MA1 (144-pin LQFP)	57
	V850E/MA1 (161-pin FBGA)	P8
	V850E/MA2 (100-pin LQFP)	35

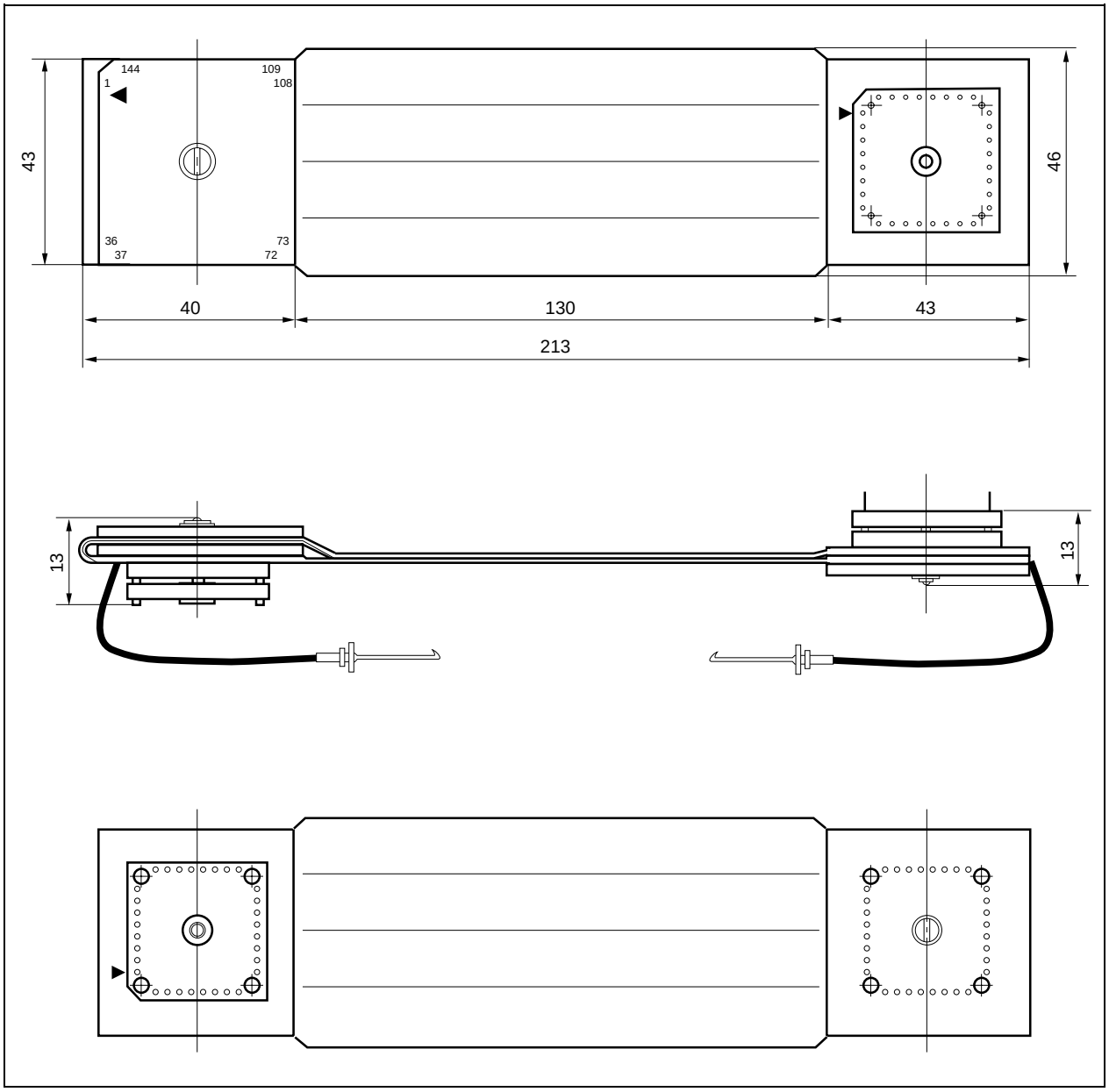
APPENDIX A DIMENSIONS

A.1 Corresponding Package Dimensions

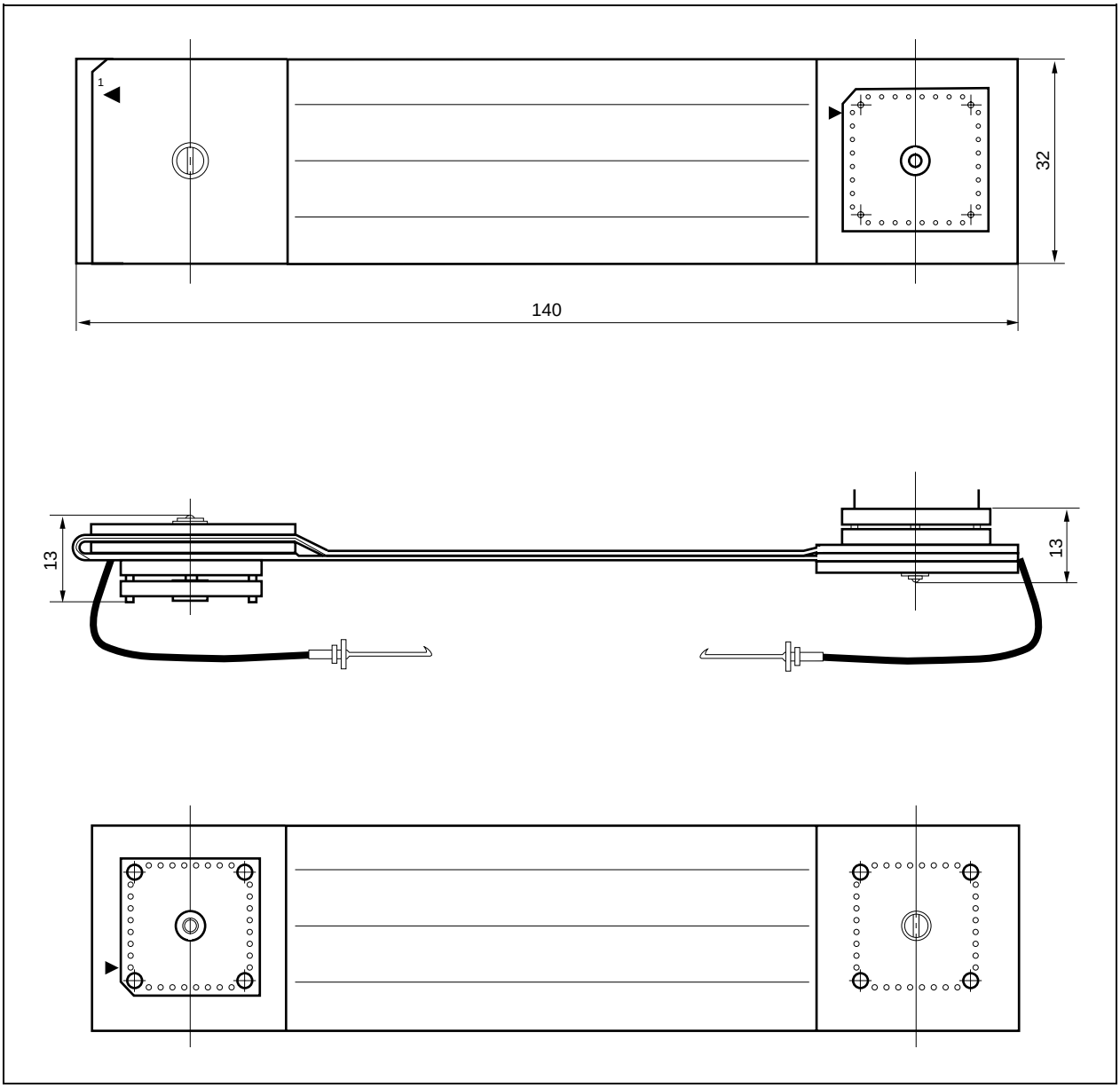
★ **(1) IE-V850E-MC-A + IE-703107-MC-EM1 (Unit: mm)**



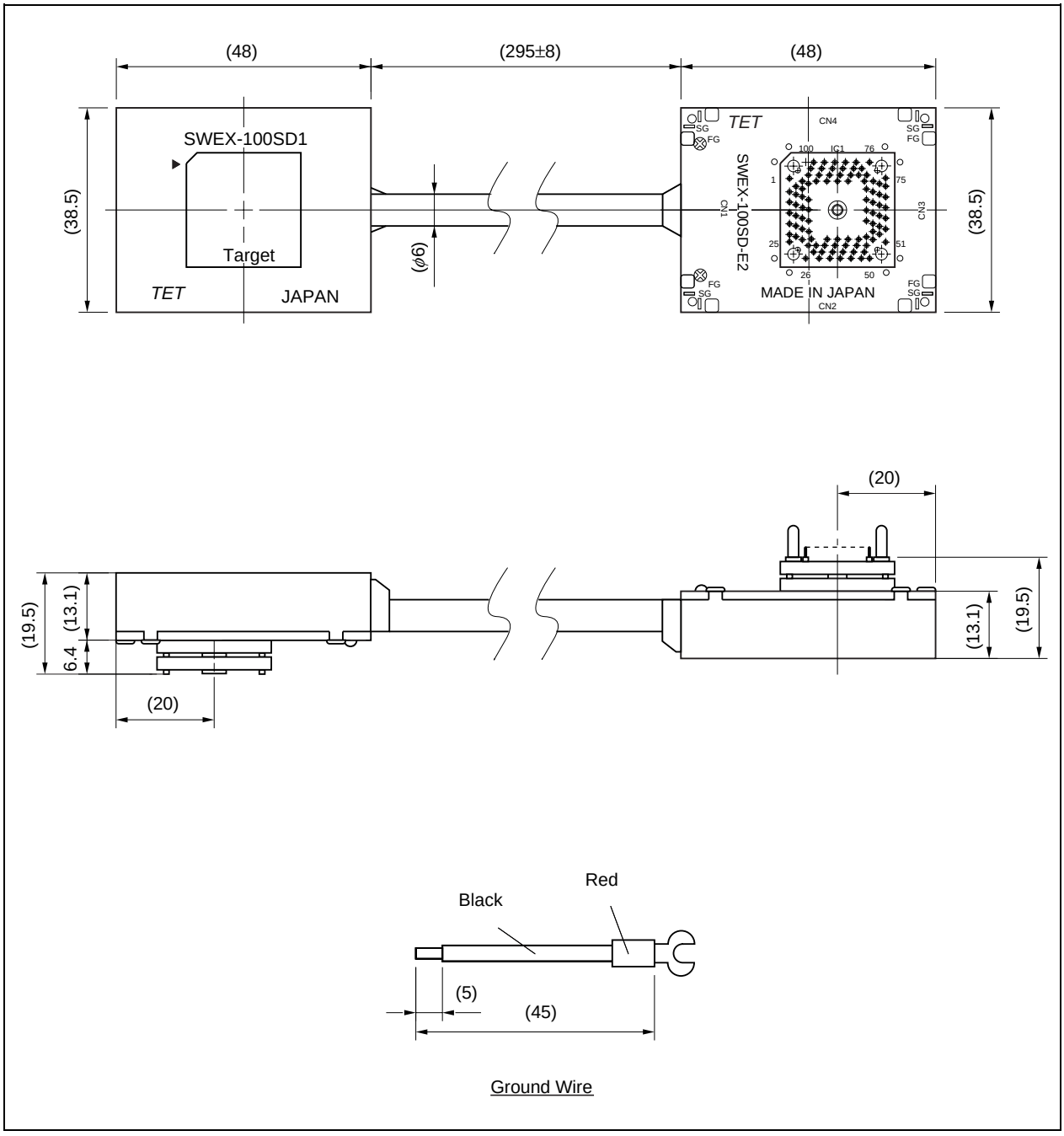
(2) SC-144SDN (Unit: mm)



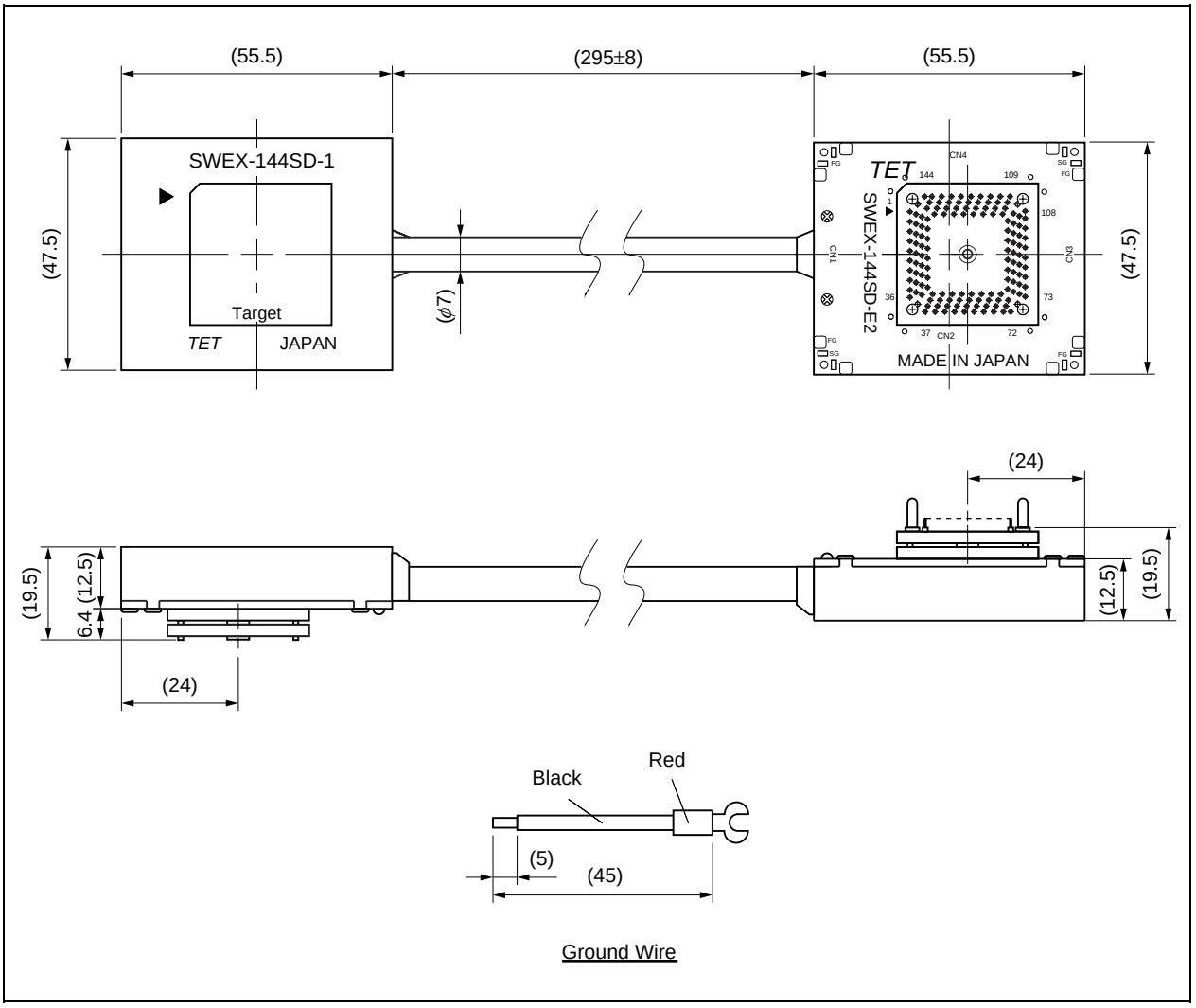
★ **(3) SC-100SDN (Unit: mm)**



★ **(4) SWEX-100SD-1 (Unit: mm)**

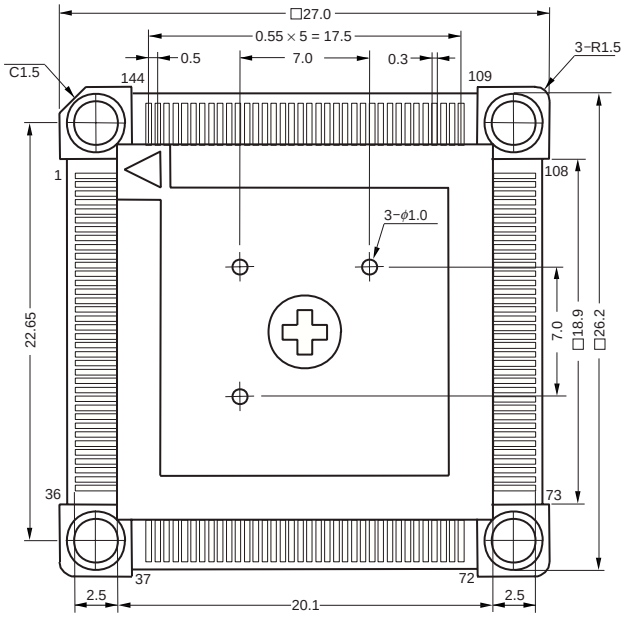


★ **(5) SWEX-144SD-1 (Unit: mm)**

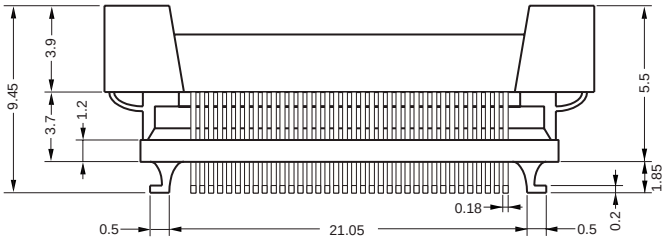


(6) NQPACK144SD (Unit: mm)

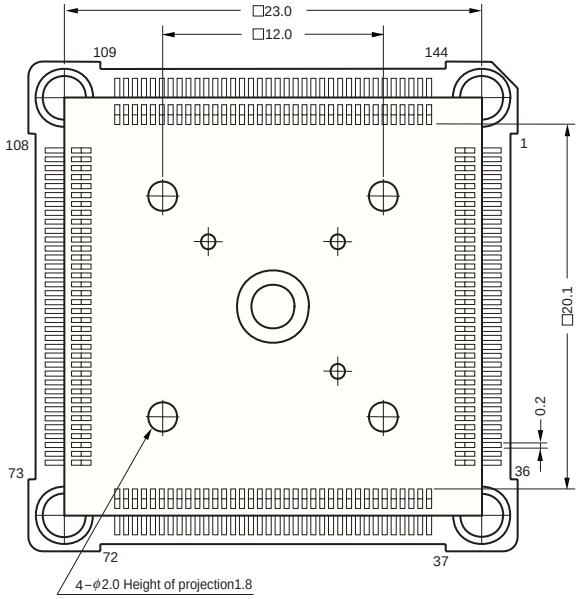
[Top View]



[Side View]

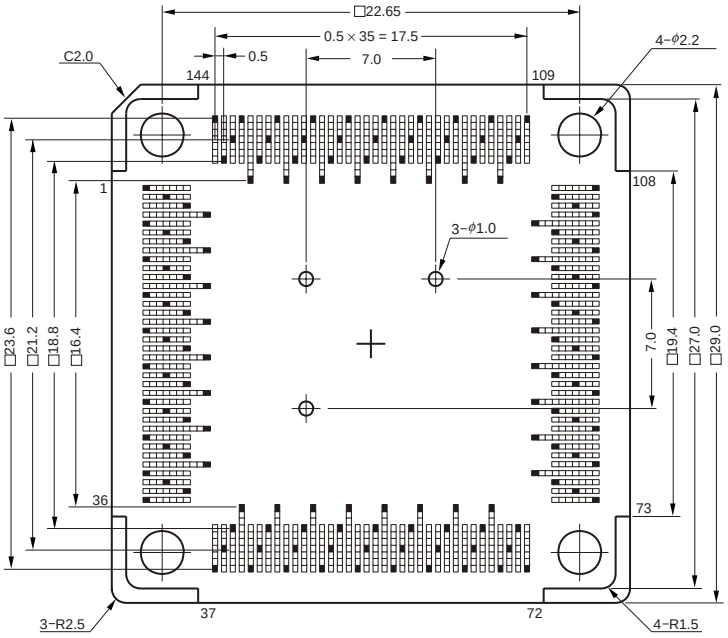


[Bottom View]

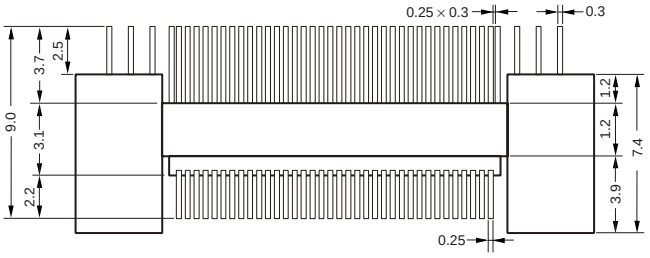


(7) YQPACK144SD (Unit: mm)

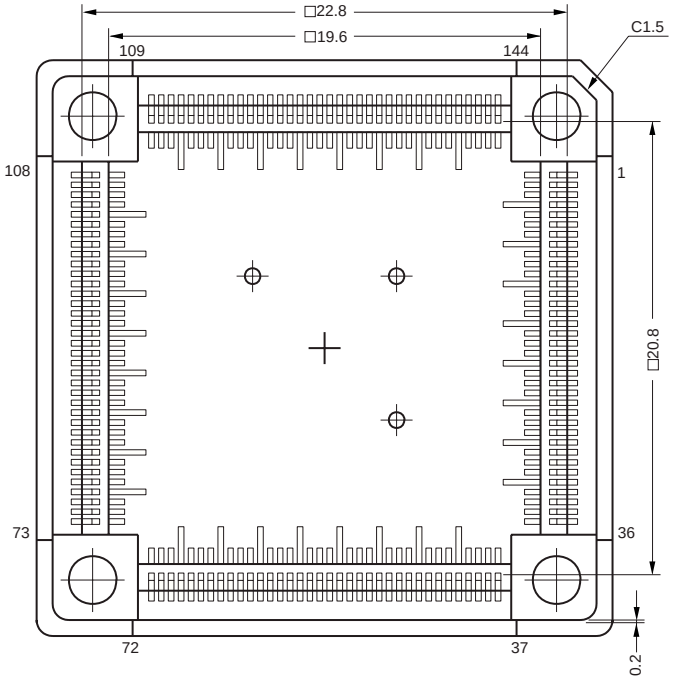
[Top View]



[Side View]

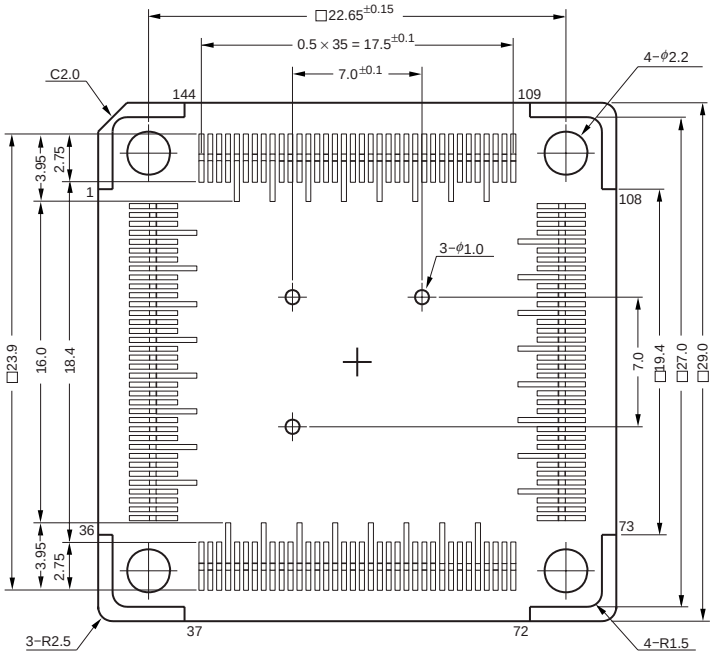


[Bottom View]

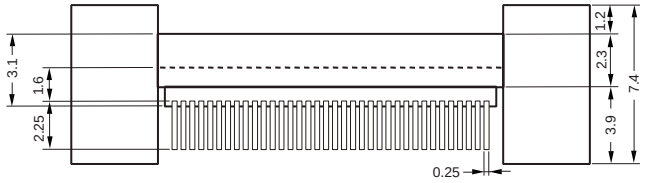


(8) HQPACK144SD (Unit: mm)

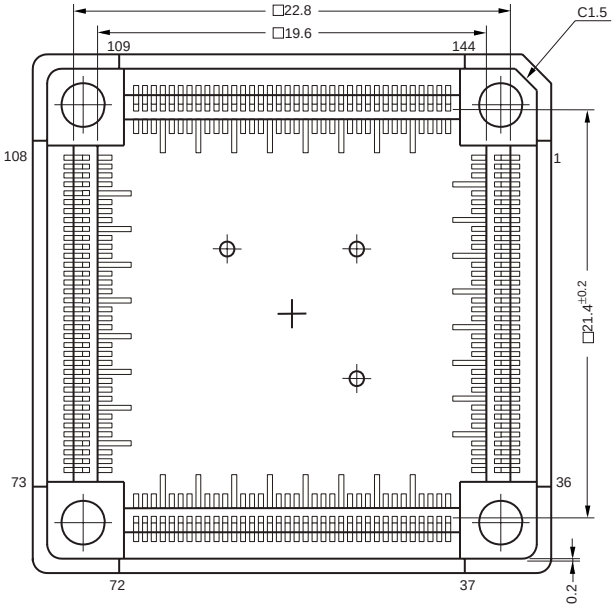
[Top View]



[Side View]

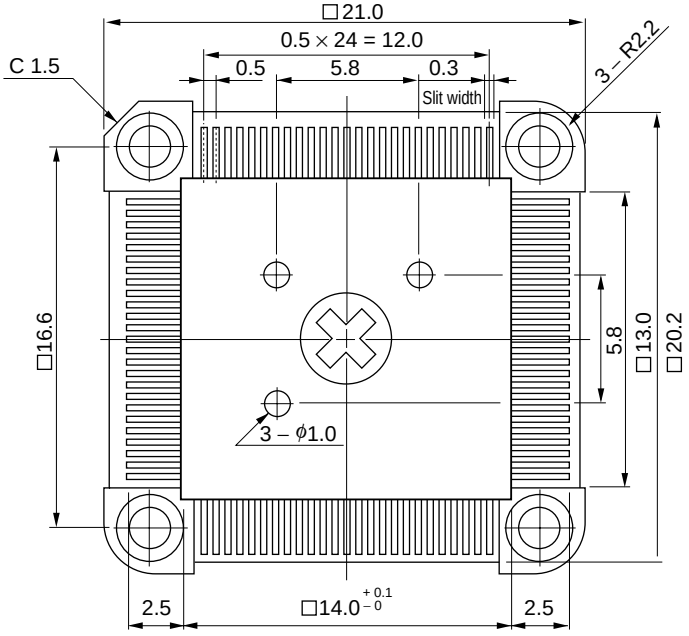


[Bottom View]

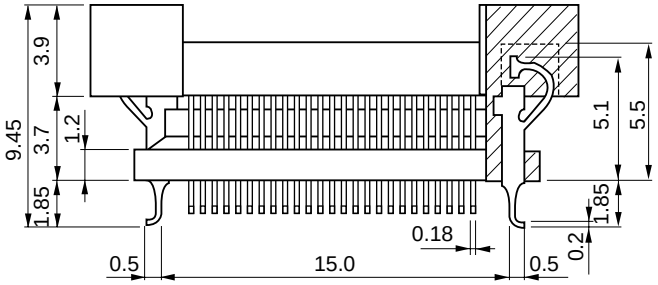


★ **(9) NQPACK100SD (Unit: mm)**

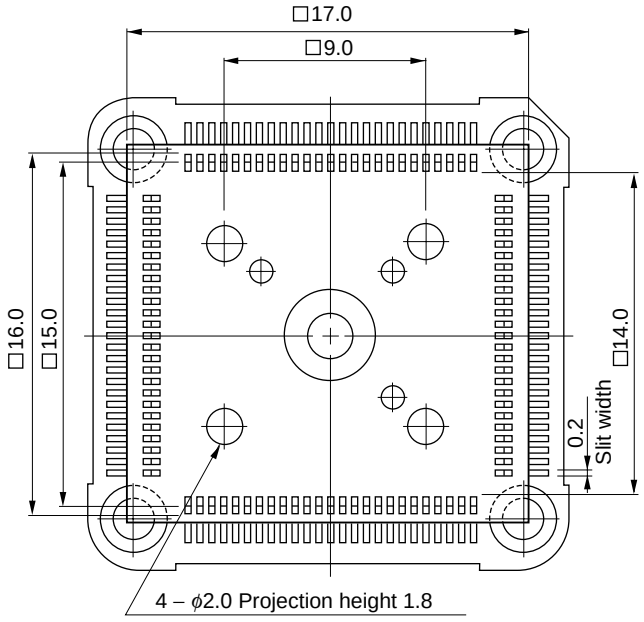
[Top View]



[Side View]

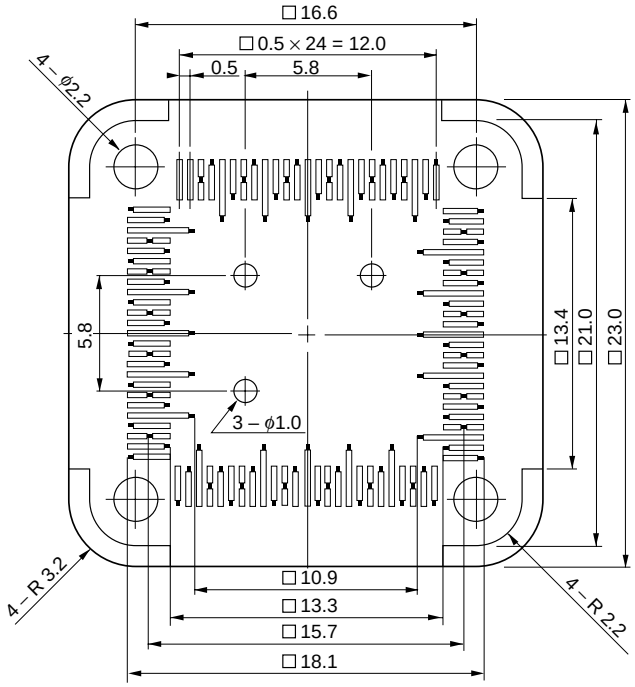


[Bottom View]

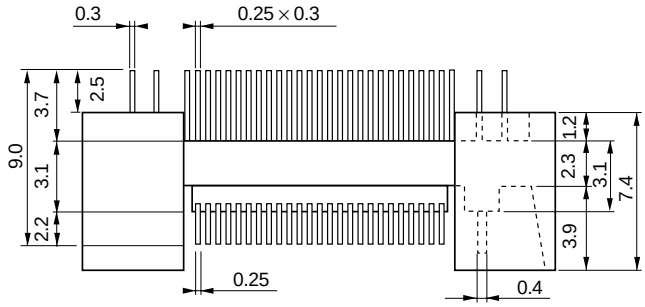


★ **(10) YQPACK100SD (Unit: mm)**

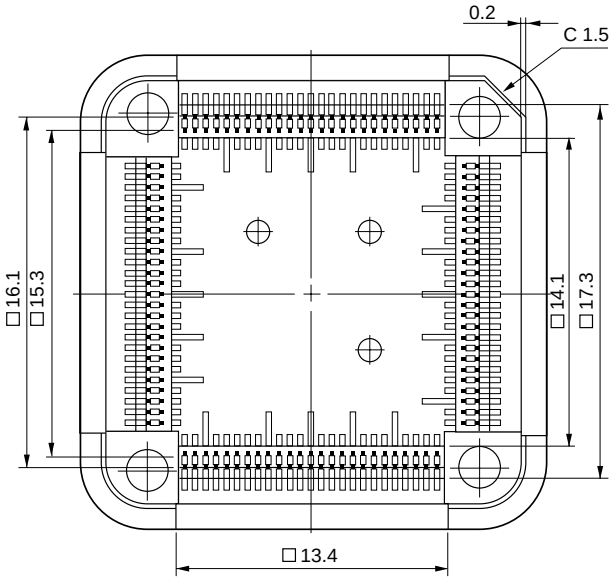
[Top View]



[Side View]

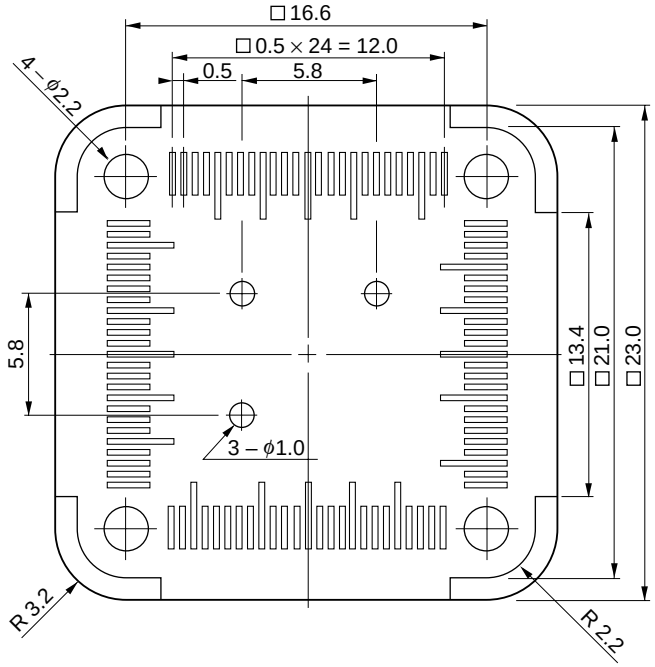


[Bottom View]

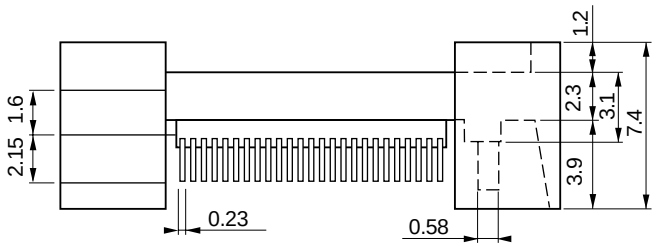


★ **(11) HQPACK100SD (Unit: mm)**

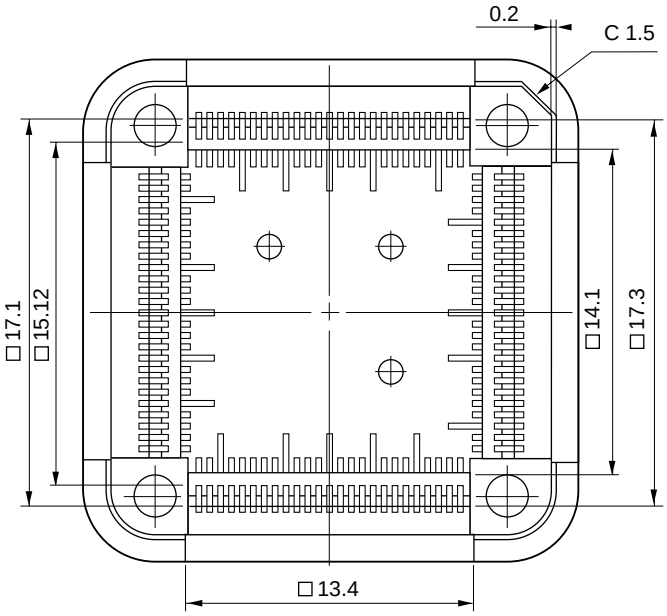
[Top View]



[Side View]

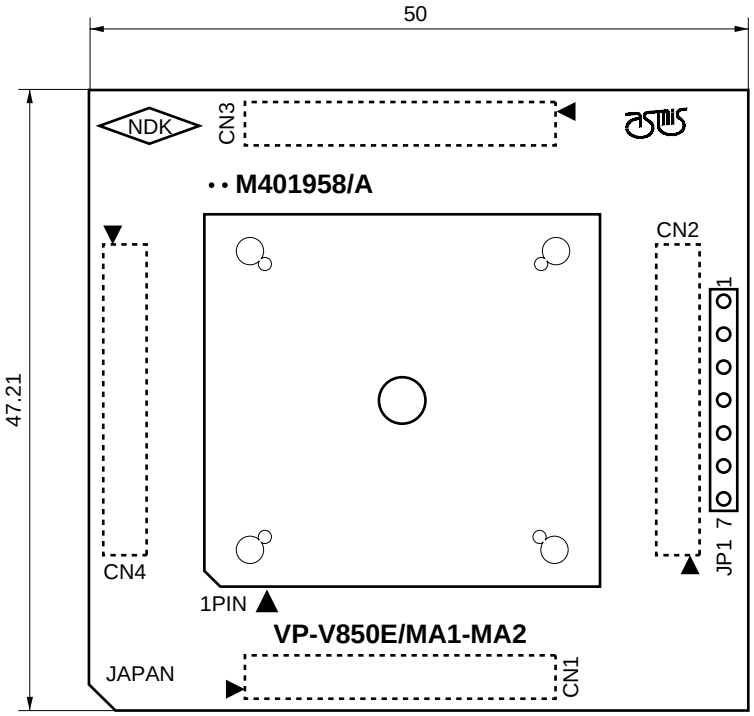


[Bottom View]

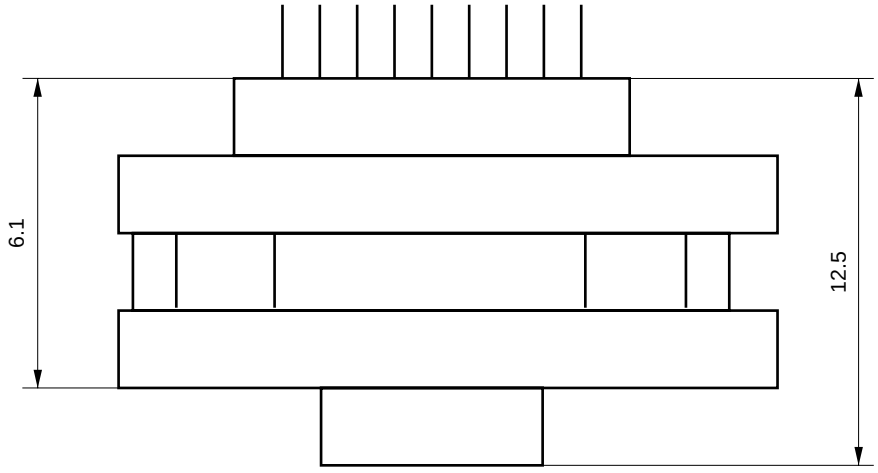


★ **(12) VP-V850E/MA1-MA2 (Unit: mm)**

[Top View]

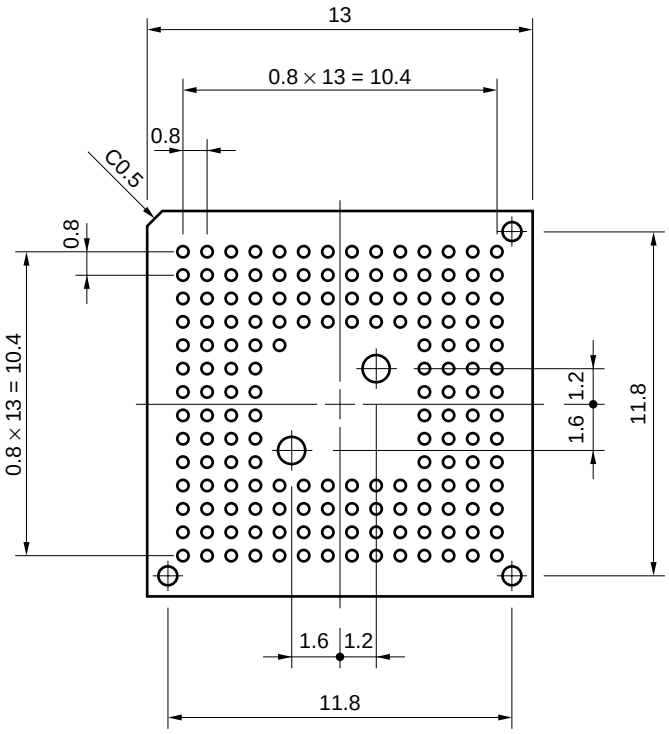


[Side View]

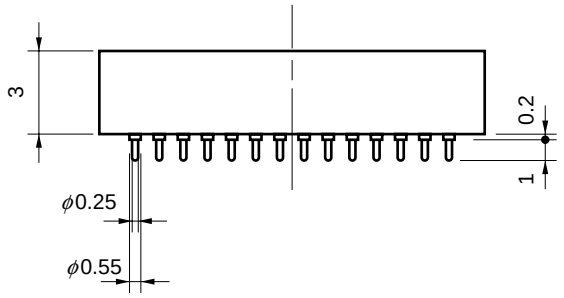


★ **(13) CSSOCKET161A1413N01N (Unit: mm)**

[Top View]

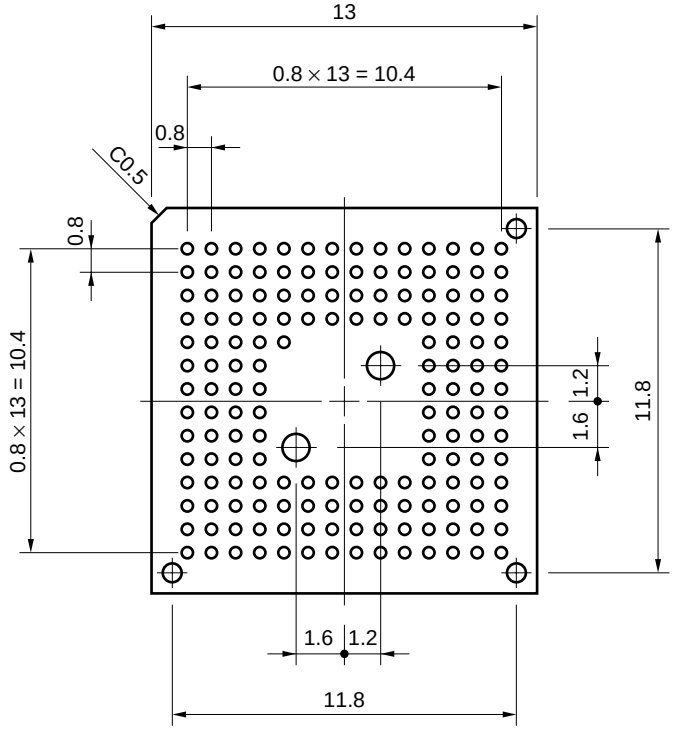


[Side View]

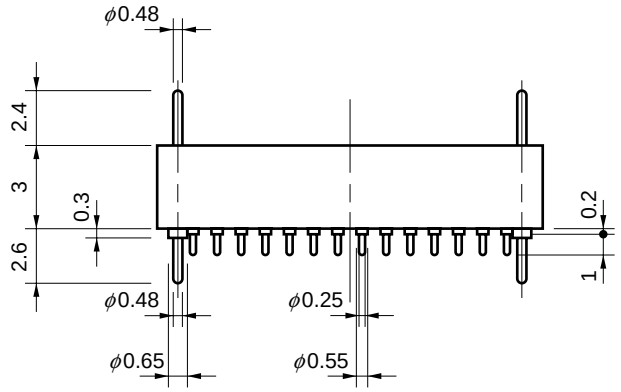


★ (14) CSSOCKET161A1413N01 (Unit: mm)

[Top View]

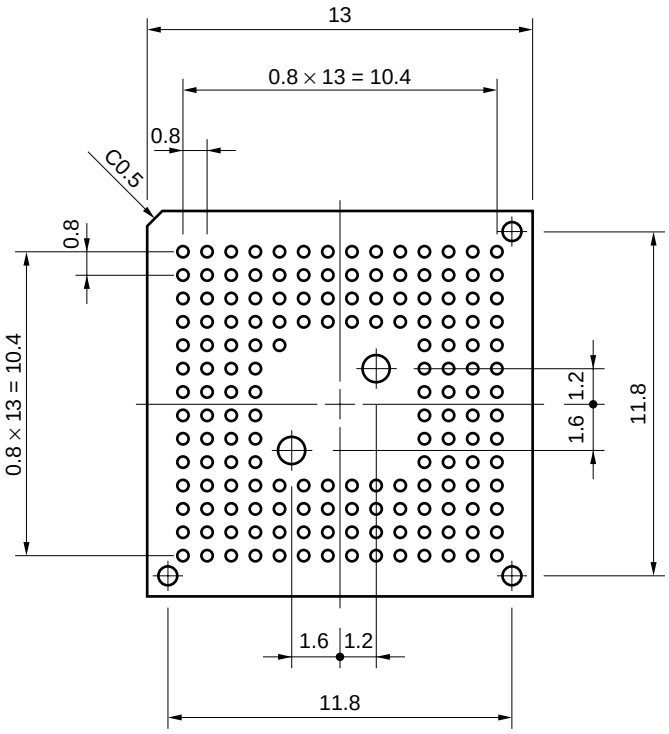


[Side View]

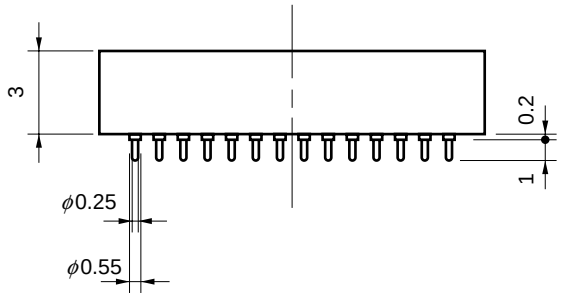


★ **(15) CSSOCKET161A1413N01S1 (Unit: mm)**

[Top View]

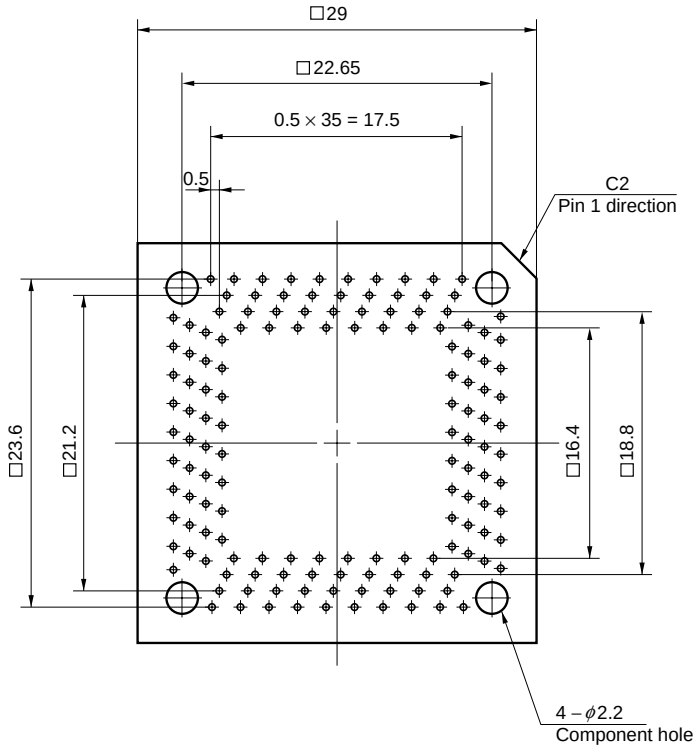


[Side View]

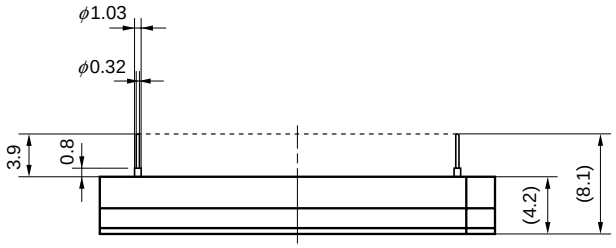


★ (16) CSICE161A1413N02 (Unit: mm)

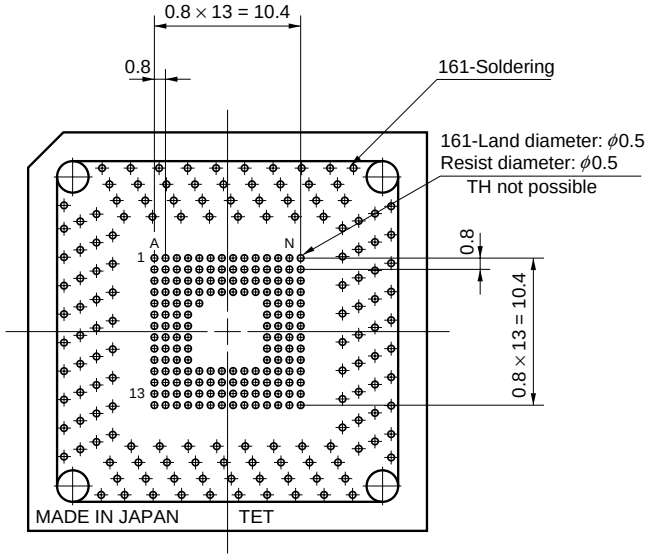
[Top View]



[Side View]

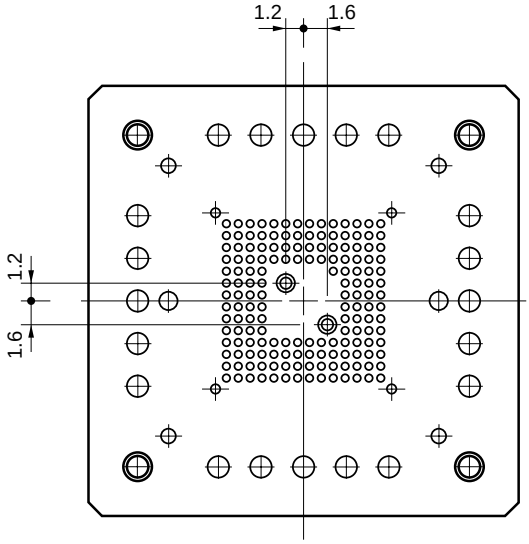


[Bottom View]

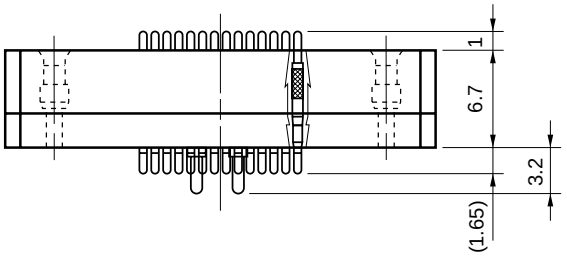


★ **(17) LSPACK161A1413N01 (CSICE, without device mounting cover) (Unit: mm)**

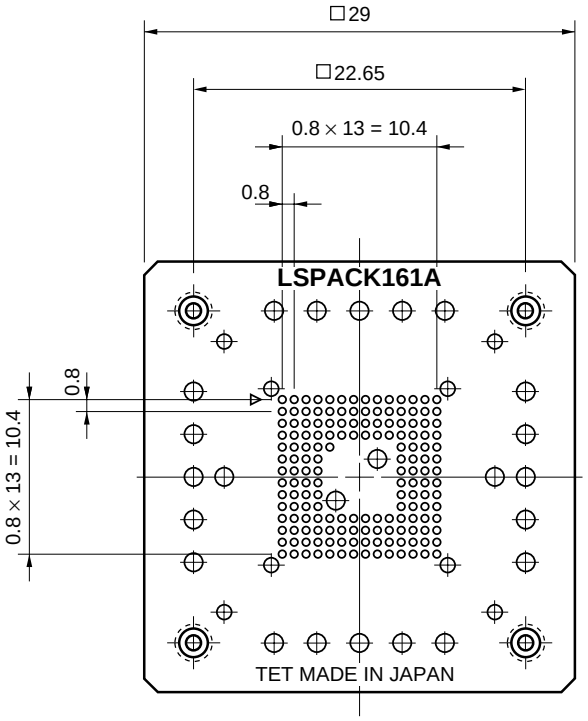
[Top View]



[Side View]

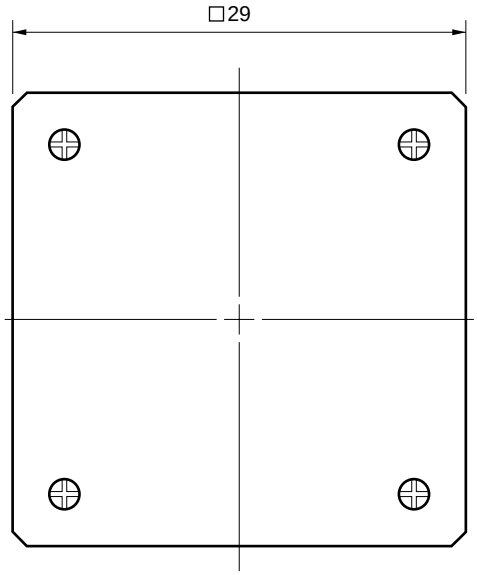


[Bottom View]

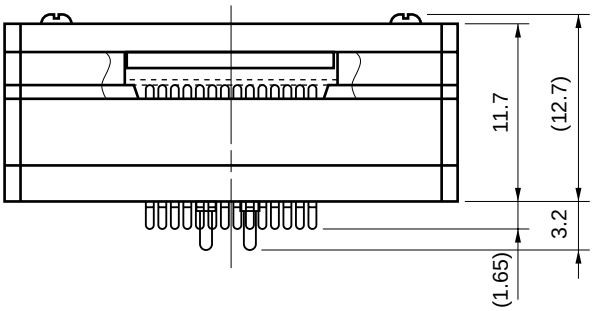


★ **(18) LSPACK161A1413N01 (with device mounting cover) (Unit: mm)**

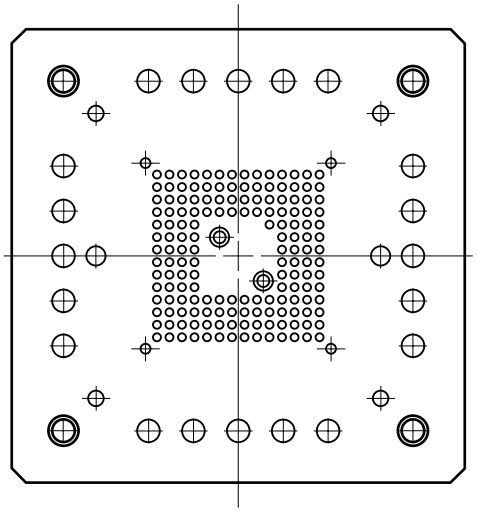
[Top View]



[Side View]



[Bottom View]

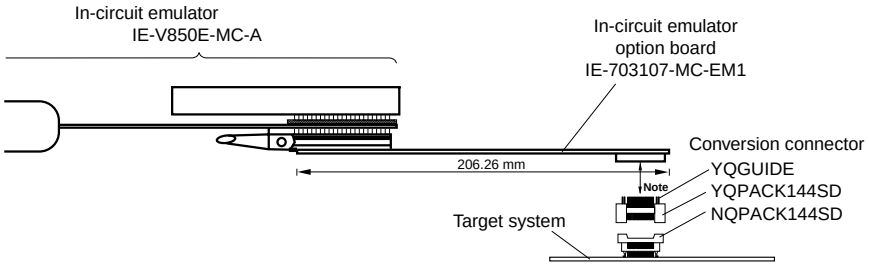


★ A.2 Conditions for Connecting of In-Circuit Emulator Option Board and Conversion Connector

The following shows a diagram of the conditions for connecting the in-circuit emulator option board and conversion connector. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.

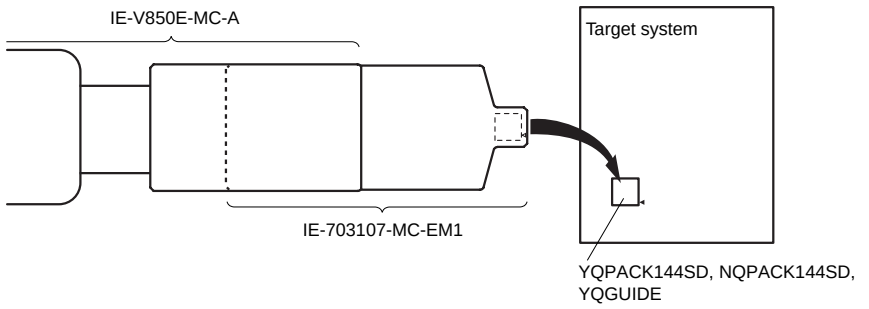
★ (1) V850E/MA1, 144-pin plastic LQFP (fine pitch) (20 × 20)

Side View

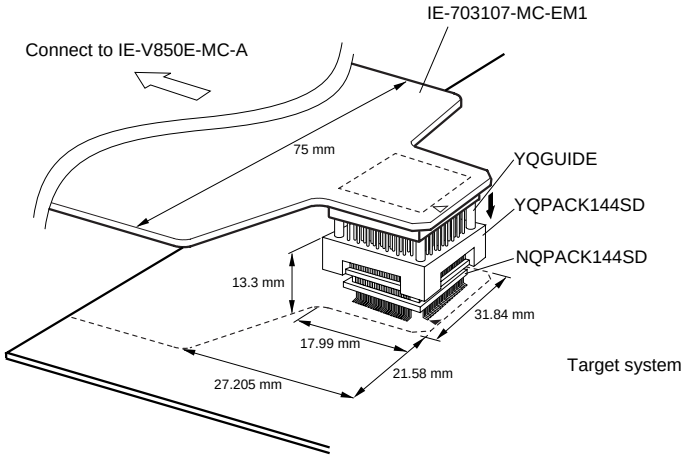


Note The YQSOCKET144SDN (sold separately) can be inserted here to adjust the height (height: 3.2 mm).

Top View



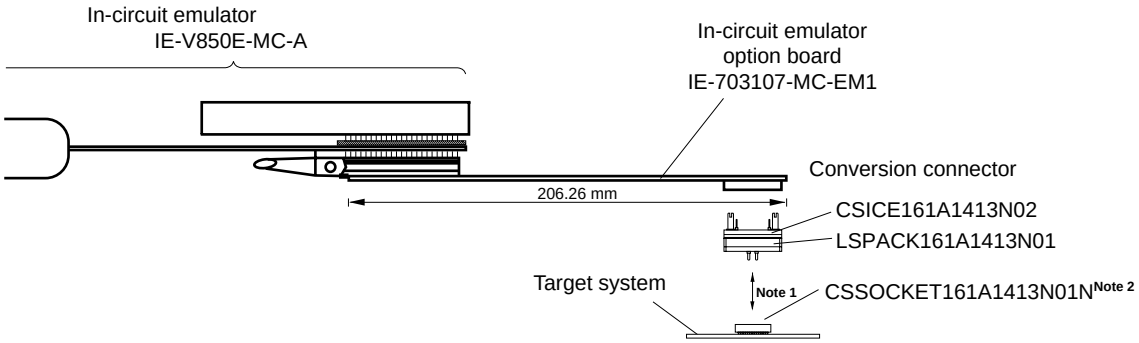
Connection condition diagram



Remark The connector for the 161-pin plastic FBGA package is under development.

(2) V850E/MA1, 161-pin plastic FBGA (13 × 13)

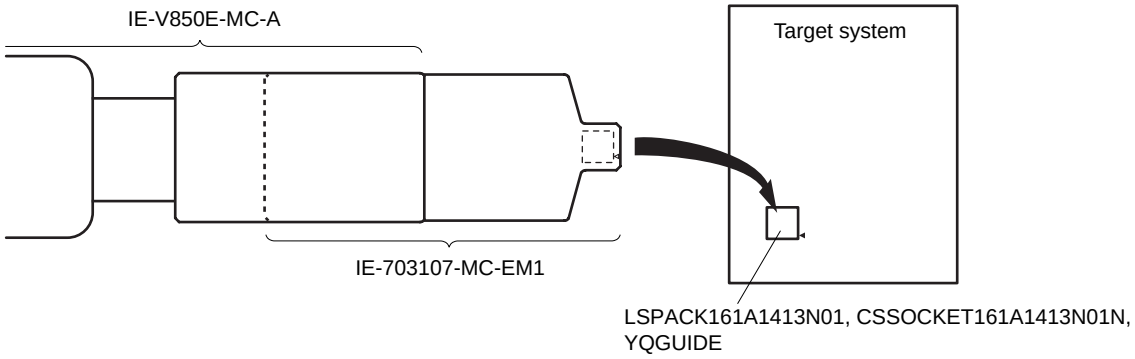
Side View



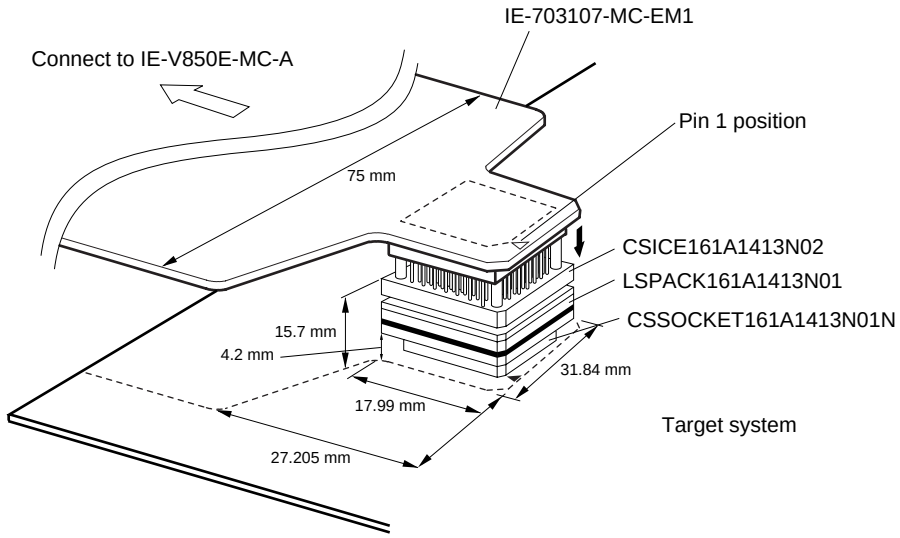
Notes 1. The CSSOCKET161A1413N01S1 (sold separately) can be inserted here to adjust the height (height: 3.2 mm).

2. This is a target socket without guides. Remove suffix N from the part number when a target socket with guides is needed.

Top View

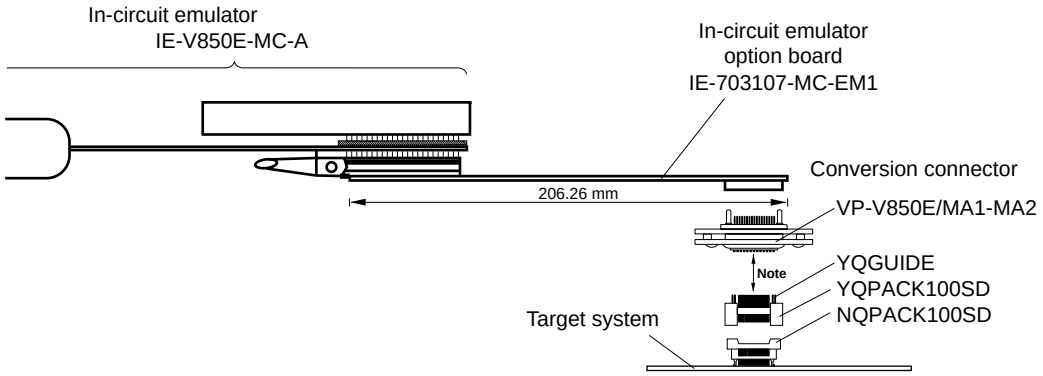


Connection condition diagram



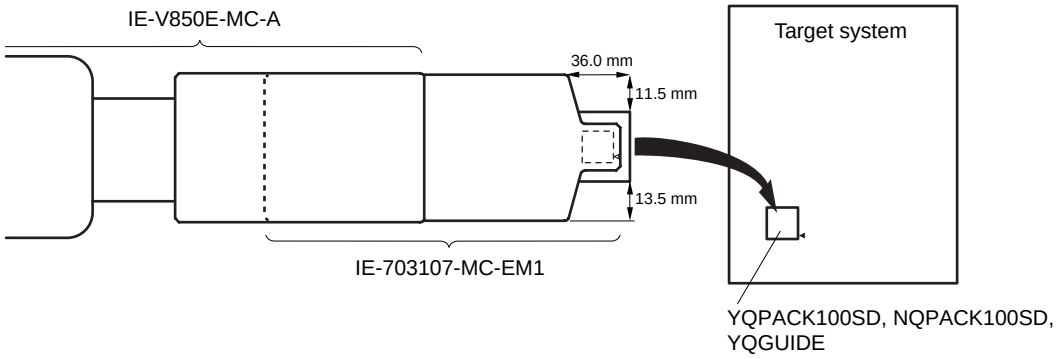
(3) V850E/MA2, 100-pin plastic LQFP (fine pitch) (14 × 14)

Side View

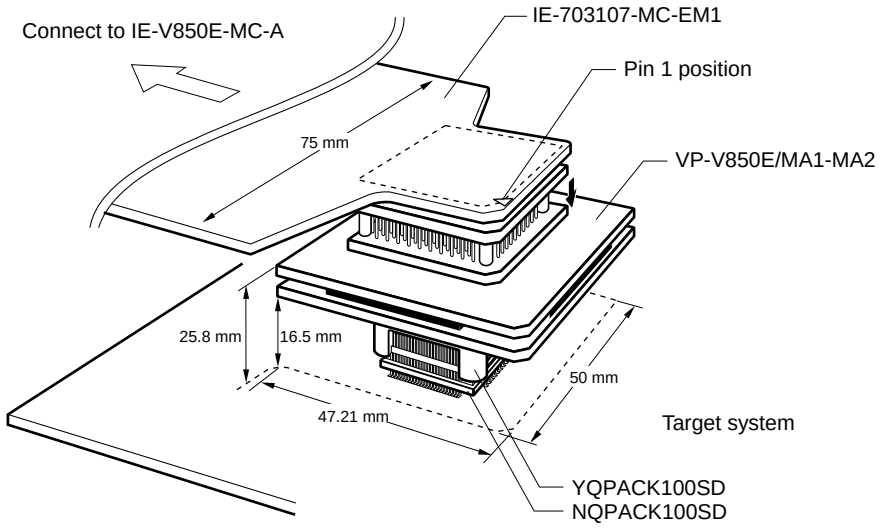


Note The YQSOCKET100SDN (sold separately) can be inserted here to adjust the height (height: 3.2 mm).

Top View

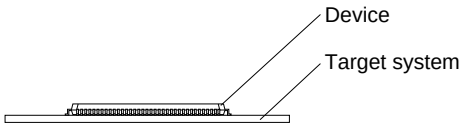


Connection condition diagram



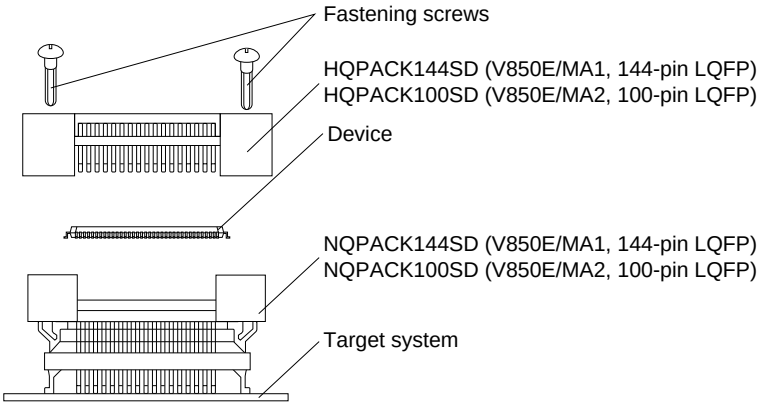
APPENDIX B EXAMPLE OF USE OF CONNECTOR FOR TARGET CONNECTION

(1) When directly connecting device to target system (connector for target connection is not used)

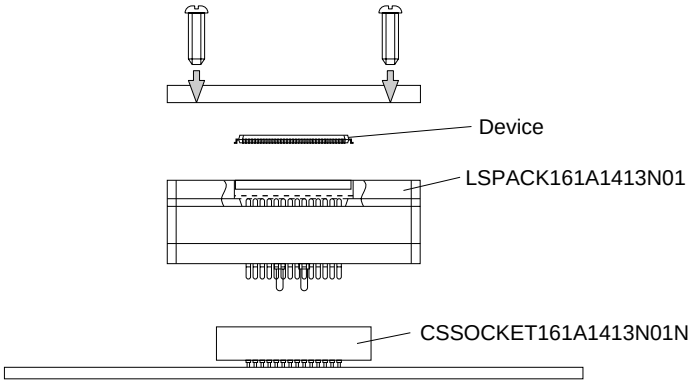


(2) When connecting device using connector for target connection

(a) LQFP package



(b) FBGA package



APPENDIX C CONNECTORS FOR TARGET CONNECTION

★ C.1 Usage (LQFP Package)

(1) When mounting NQPACK144SD on target system

<1> Coat the tip of the four projections (points) at the bottom of the NQPACK144SD or NQPACK100SD with two-component type epoxy adhesive (cure time longer than 30 minutes) and bond the NQPACK144SD or NQPACK100SD to the target system. If not bonded properly, the pad of the printed circuit board may peel off when the emulator is removed from the target system. If the lead of the NQPACK144SD or NQPACK100SD is not aligned with the pad of the target system easily, perform step <2> to adjust the position.

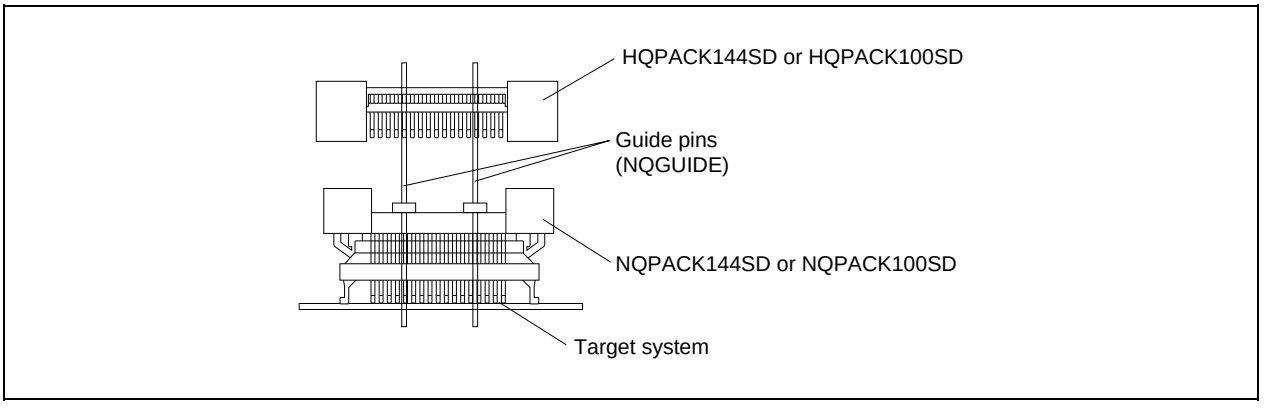
<2> To adjust the position, insert the guide pins for position-adjustment (NQGUIDE) provided with the NQPACK144SD or NQPACK100SD into the pin holes at the upper side of NQPACK144SD or NQPACK100SD (refer to **Figure C-1**). The diameter of a hole is ϕ = 1.0 mm. There are three non-through holes (refer to **APPENDIX A DIMENSIONS**).

<3> After setting the HQPACK144SD or HQPACK100SD, solder the NQPACK144SD or NQPACK100SD to the target system. By following this sequence, adherence of flux or solder sputtering to contact pins of the NQPACK144SD or NQPACK100SD can be avoided.

Recommended soldering conditions… Reflow: 240°C, 20 seconds max.
Partial heating: 240°C, 10 seconds max. (per pin row)

<4> Remove the guide pins.

Figure C-1. Mounting of NQPACK144SD or NQPACK100SD



Remark NQPACK144SD or NQPACK100SD: Connector for target connection
HQPACK144SD or HQPACK100SD: Cover for device mounting

(2) When mounting device

Caution Check for abnormal conditions such as resin burr or bent pins before mounting a device on the NQPACK144SD or NQPACK100SD. Moreover, check that the hold pins of the HQPACK144SD or HQPACK100SD are not broken or bent before mounting the HQPACK144SD or HQPACK100SD on top of the device. If there are broken or bent pins, fix them with a thin, flat plate such as a blade.

<1> Make sure that the NQPACK144SD or NQPACK100SD is clean and the device pins are parallel (flat) before mounting a device on the NQPACK144SD or NQPACK100SD. Then, after mounting the NQPACK144SD or NQPACK100SD to the target board, fix the device and the HQPACK144SD or HQPACK100SD (refer to **Figure C-2**).

<2> Using the screws provided with the HQPACK144SD or HQPACK100SD (four locations: M2 × 6 mm), secure the HQPACK144SD or HQPACK100SD, device, and NQPACK144SD or NQPACK100SD.
Tighten the screws in a crisscross pattern with the screwdriver provided or a driver with a torque gauge (avoid tightening only one screw strongly). Tighten the screws with 0.55 kg·f·cm (0.054 Nm) max. torque. Excessive tightening may diminish conductivity.
At this time, each pin is fixed inside the plastic wall dividers by the contact pin of the NQPACK144SD or NQPACK100SD and the hold pin of the HQPACK144SD or HQPACK100SD (refer to **Figure C-3**). Thus, pins cannot cause a short with pins of neighboring devices.

Figure C-2. Mounting of Device

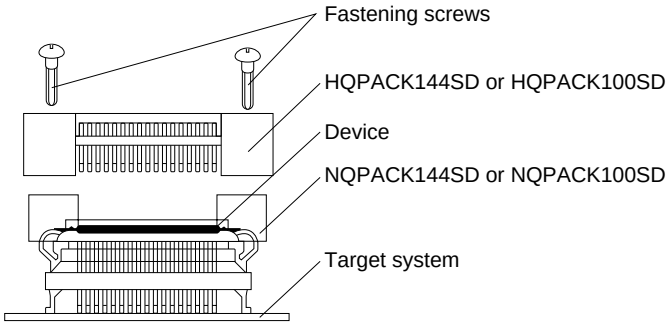
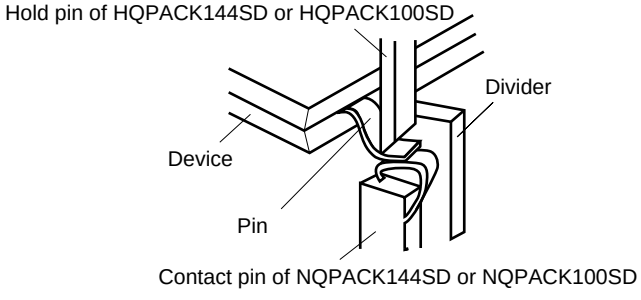


Figure C-3. NQPACK144SD or NQPACK100SD and Device Pin



★ C.2 Cautions on Handling Connectors (LQFP Package)

(1) When taking connectors out of the case, remove the sponge while holding the main unit.

(2) When soldering the NQPACK144SD or NQPACK100SD to the target system, cover with the HQPACK144SD or HQPACK100SD to protect it against splashing flux.

Recommended soldering conditions… Reflow: 240°C, 20 seconds max.
Partial heating: 240°C, 10 seconds max. (per pin row)

(3) Check for abnormal conditions such as resin burr or bent pins before mounting a device on the NQPACK144SD or NQPACK100SD. Moreover, check that the hold pins of the HQPACK144SD or HQPACK100SD are not broken or bent before mounting the HQPACK144SD or HQPACK100SD. If there are broken or bent pins, fix them with a thin, flat plate such as a blade.

(4) When securing the YQPACK144SD or YQPACK100SD (connector for emulator connection) or HQPACK144SD or HQPACK100SD to the NQPACK144SD or NQPACK100SD with screws, tighten the four screws temporarily with the screwdriver provided or a driver with a torque gauge, then tighten the screws in a crisscross pattern (with 0.054 Nm max. torque).
Excessive tightening of only one screw may diminish conductivity.
If the conductivity is diminished after screw-tightening, stop tightening, remove the screws and check that the NQPACK144SD or NQPACK100SD is not dirty and make sure the device pins are parallel.

(5) Device pins do not have high strength. Repeatedly connecting to the NQPACK144SD or NQPACK100SD may cause pins to bend. When mounting a device on NQPACK144SD or NQPACK100SD, check and adjust bent pins.

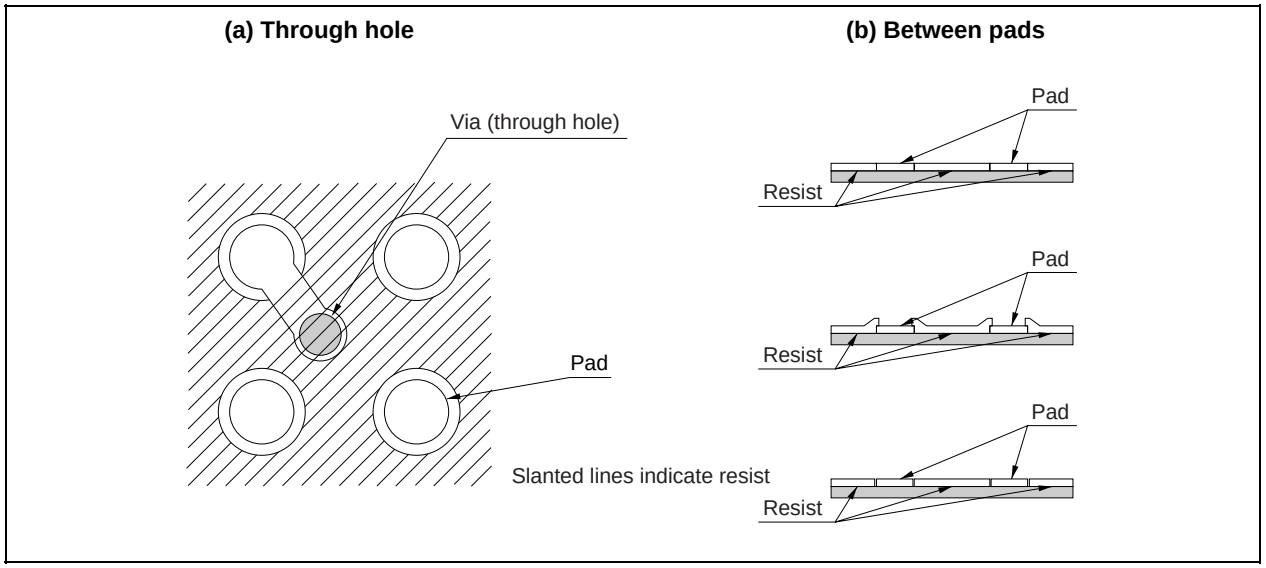
C.3 Notes on Board Design (FBGA Package)

(1) If a through hole is made in an IC pad or nearby, the cream solder melts and flows into the hole, causing open pins.

(2) When making a through hole in an IC pad, fill the hole.

(3) If it is necessary to make a through hole near an IC pad, be sure to apply resist between the pad and through hole as shown in Figure C-4 (a). It is also recommended to apply the resist on the through hole pad. In addition, be sure to apply resist between pads as shown in Figure C-5 (b).

Figure C-4. Application of Resist



(4) When connecting pads to each other in a pattern for a power supply or GND, the solder may be hard to melt if the pattern is too wide because heat diffuses.

(5) To use CSSOCKET with guides, a component hole or through hole is necessary. For the position and dimensions of the hole, refer to the attached drawing.
The guide pin may be of stainless steel (which cannot be soldered) or may be gold-plated (which can be soldered). A stainless steel guide pin only serves as a guide, but a gold-plated guide pin can be soldered from the rear side of the target board if the guide hole is a through hole. This securely attaches the connector and board, and mitigates the stress applied on the connector.

C.4 Soldering CSSOCKET (Main Enclosure Connector) to Target Board (FBGA Package)

(1) Apply cream solder to the BGA pad of the target board. The thickness of the cream solder on the pad should be 100 to 150 μm. Too thick cream solder may cause short-circuiting.

(2) On the part of CSSOCKET to be connected to LSPACK, protective tape (polyimide tape) is attached for protection from flux splashing during reflow soldering. Do not remove this tape until reflow soldering is completed.

(3) Place CSSOCKET on the target board, with its guide pins inserted into the holes for the guides on the target board, as shown in Figure C-5. Confirm that the pad on the board and CSSOCKET are correctly positioned.

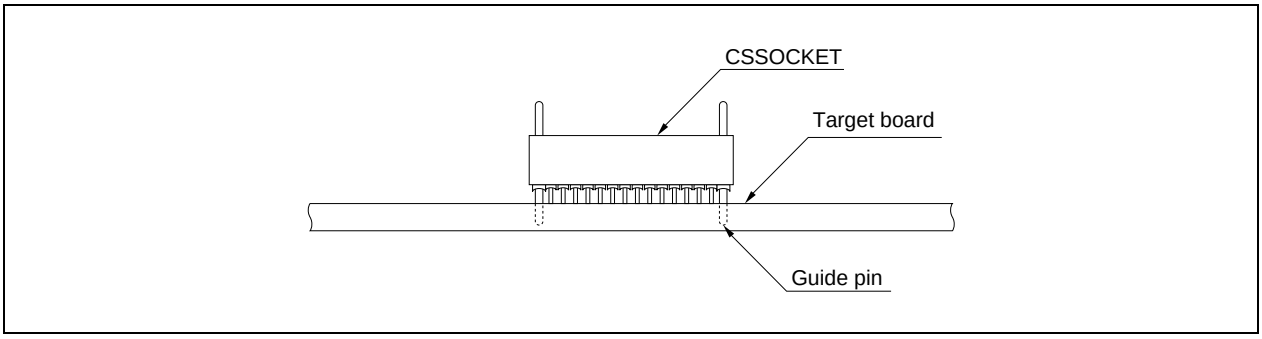
(4) Mounting CSSOCKET
   <1> The dimensions of CSSOCKET are the same as the actual IC package.
   <2> Solder CSSOCKET at a temperature of 210°C or more and for 30 to 60 seconds, as indicated in the table below.
   <3> Table C-1 shows the recommended reflow conditions. Figure C-6 shows an example of the mounting profile of CSSOCKET.

Table C-1. Recommended Reflow Conditions

	Surface Temperature of CSSOCKET Connector
Preheating	150 to 180°C, 180 seconds
Heating	210°C or more, 30 to 60 seconds

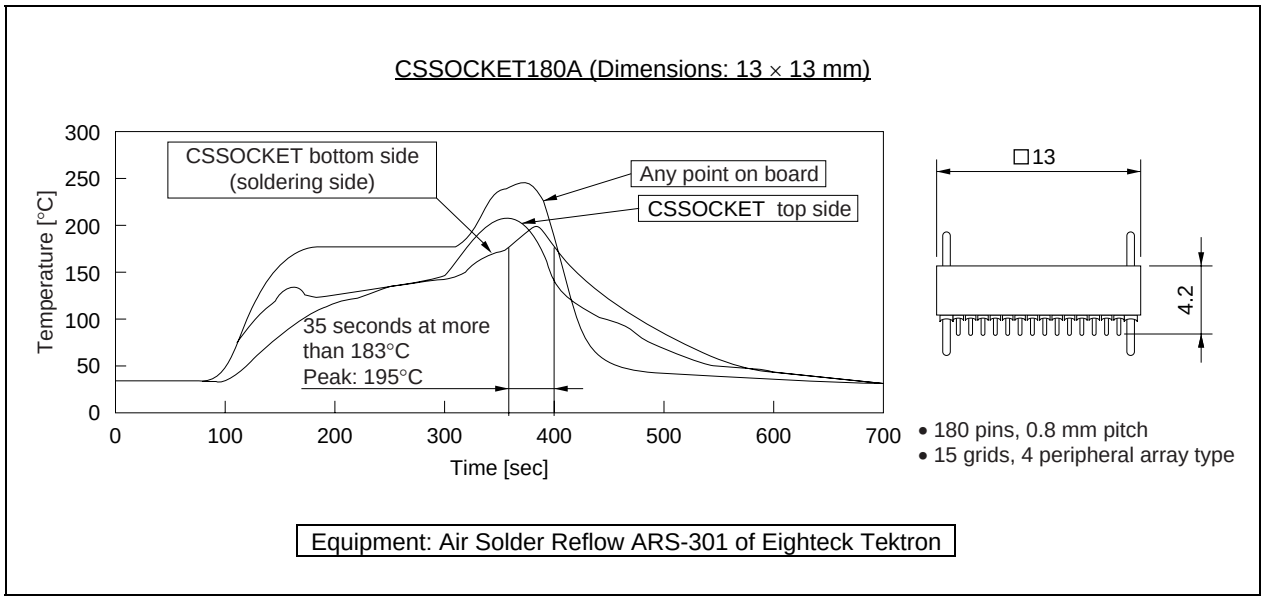
(5) Remove the protective tape from the surface.

Figure C-5. Mounting of CSSOCKET on Target Board



Caution Do not clean CSSOCKET to remove flux.

Figure C-6. Example of Mounting Profile of CSSOCKET



Caution

- **Because the construction of CSSOCKET allows flux and cleaning solvent to remain in the connector, do not dip CSSOCKET into flux or clean it to remove flux. The same applies when using CSSOCKET with other DIP components, as the flux of the DIP component may get into CSSOCKET.**
- **To solder the type of CSSOCKET without guide pins, correctly position it on the pad of the board.**
- **After soldering the CSSOCKET connector, it is recommended to solder the guide pins from the bottom side of the board or to secure the connector peripheral parts with resin, for reinforcement. Use of two-component type epoxy resin or a cure-type adhesive agent, and an adhesive agent for securing the surface mount components is recommended.**

C.5 Using LSPACK to Mount IC (FBGA Package)

Attach LSPACK to CSSOCKET, which has already been soldered, using the guide plate, spacer, and top cover.

(1) Align the guides of CSSOCKET and LSPACK, and attach LSPACK to CSSOCKET.

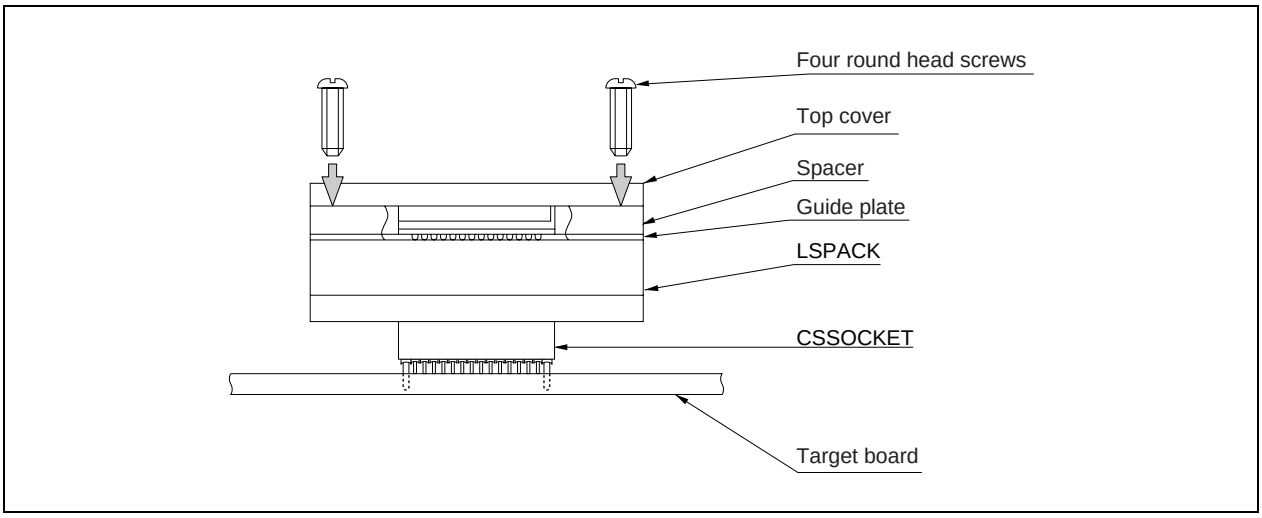
(2) Place the guide plate (included with models released after November 2000) and spacer, in that order, on LSPACK. Align the guide of the spacer with the component hole of LSPACK and the guide plate.

(3) Noting the position of pin 1 of the IC (BGA), gently place the IC from the top in the opening at the center of the spacer, aligning it with the connector pin position.

(4) Place the top cover on the spacer. The holes at the four corners of the guide plate, spacer, and top cover must match. Secure LSPACK and the top cover using the attached screws. Use a dedicated screwdriver to tighten the screws. Hold LSPACK on the sides with your fingers, so that no stress is applied to the soldered parts of LSPACK and CSSOCKET, and sequentially tighten the screws at the four corners. The tightening torque should be 0.55 kg·f·cm (0.054 Nm) maximum.

(5) To remove the top cover from LSPACK, loosen and remove the screws of the top cover while holding the cover on sides, so that no stress is applied to the soldered parts of LSPACK and CSSOCKET.

Figure C-7. Mounting of IC



C.6 Connecting In-Circuit Emulator (FBGA Package)

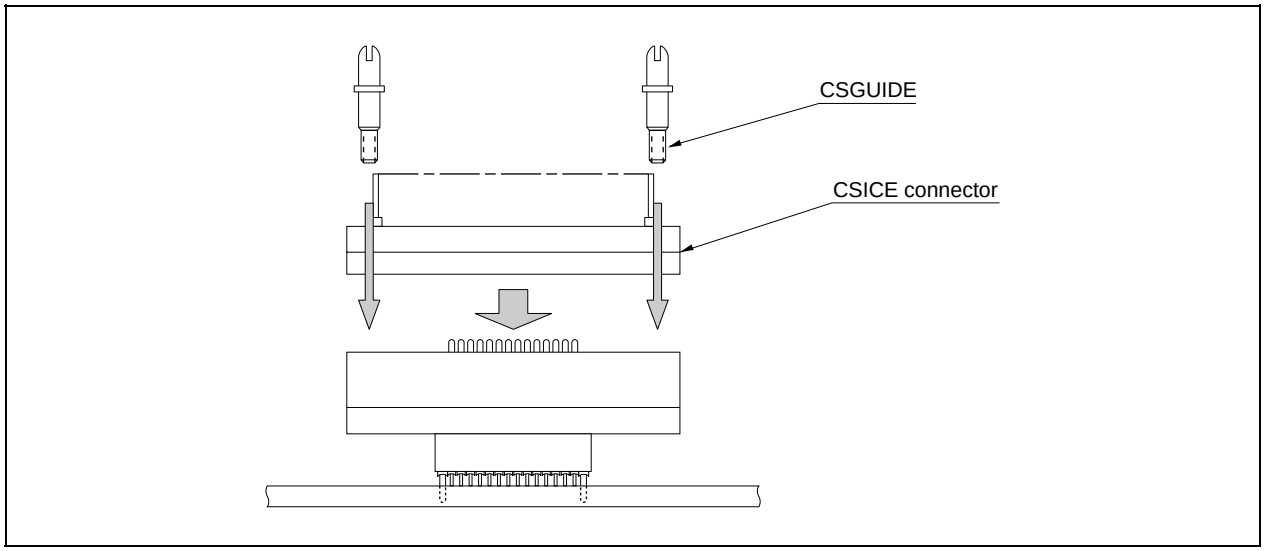
CSICE connector: Conversion adapter to connect an existing tool supporting TQPACK/NQPACK (QFP) and LSPACK (Conversion from BGA to QFP). Also for conversion to different pitches of BGA.

Attach LSPACK to CSSOCKET, which has already been soldered, using the guide plate, spacer, and top cover.

(1) Place the pad side of the CSICE connector on LSPACK. Make sure that the positions of the holes at the four corners match.

(2) Using the attached guide screws (CSGUIDE) for CSICE, secure LSPACK and the CSICE connector. Hold LSPACK the sides with your fingers, so that no stress is applied to the soldered parts of LSPACK and CSSOCKET, and sequentially tighten CSGUIDE at the four corners. The tightening torque of CSGUIDE should be 0.55 kg·f·cm (0.054 Nm) maximum. To remove the CSICE connector, hold LSPACK so that no stress is applied to the soldered parts of LSPACK and CSSOCKET, and remove the screws.

Figure C-8. CSICE Connection



C.7 Notes on Handling LSPACK/CSSOCKET (FBGA Package)

Caution When mounting CSSOCKET for the first time, refer to C.3 Notes on Board Design (FBGA Package), and C.4 Soldering CSSOCKET (Main Enclosure Connector) to Target Board (FBGA Package).

(1) When taking out LSPACK from the case, hold LSPACK and take out the sponge first.

(2) The case may be deformed if it is left for a long time in a location where temperature is 50°C or higher. Store it in a location where it is not subject to direct sunlight, and the temperature is 40°C or below.

(3) Protective tape is attached to CSSOCKET for protection from flux splashing during reflow soldering. Do not remove this tape until reflow soldering is completed.

(4) Recommended reflow conditions
Surface temperature of CSSOCKET
Preheating: 150 to 180°C, 180 seconds
Heating: 210°C or more, 30 to 60 seconds

(5) Because the construction of CSSOCKET allows flux and cleaning solvent to remain in the connector, do not dip CSSOCKET into flux or clean it to remove flux. The same applies when using CSSOCKET with other DIP components, as the flux of the DIP component may get into CSSOCKET.

(6) To secure LSPACK with screws, use a dedicated screwdriver (+) or torque driver to tighten the screws at four places. The tightening torque should be 0.55 kg·f·cm (0.054 Nm) maximum. Do not tighten one screw too much as it may cause a faulty contact.

(7) After soldering the CSSOCKET, it is recommended to solder the guide pins from the bottom side of the board or to secure the connector peripheral parts with resin, for reinforcement.

(8) To use CSSOCKET between CSSOCKET and LSPACK for stacking, exercise care that the pins of CSSOCKET for stacking are not bent.

(9) Use LSPACK/CSSOCKET as connector of evaluation.

(10) LSPACK/CSSOCKET must not be used in an environment subject to constant shock or vibration.

(11) It is assumed that this product is used for development and evaluation in a system. When using this product domestically, it is not subject to The Electric Appliance and Material Control Law and protection from electromagnetic interference.

APPENDIX D INSERTING PLASTIC SPACER

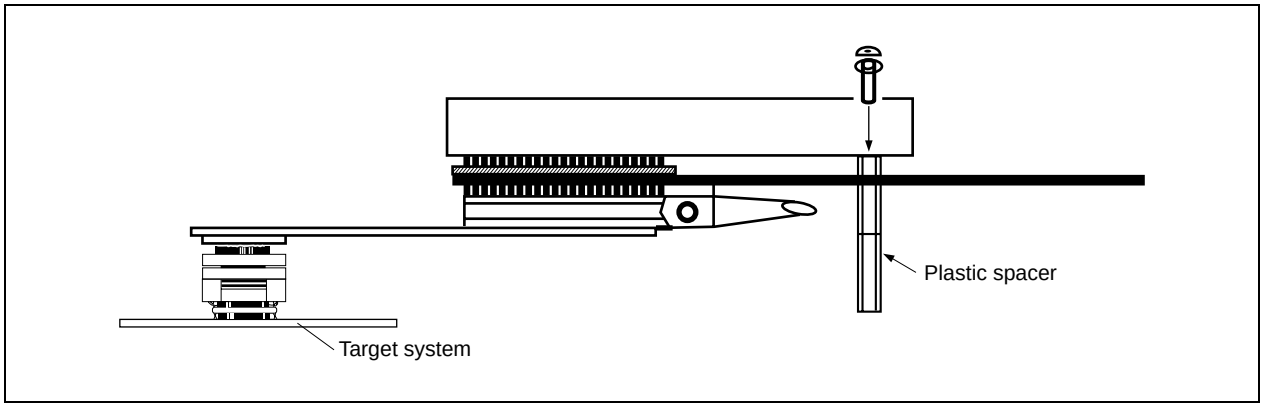
This chapter describes the method for inserting the plastic spacer supplied with the IE-V850E-MC-A.

When using the emulator connected to the target system, insert the plastic spacer in the IE-V850E-MC-A as shown in Figure D-1 to fix the pod horizontally.

- **Inserting plastic spacer in IE-V850E-MC-A**

<1> Remove the nylon rivet from the rear part of the pod.
<2> Fix the plastic spacer with the plastic screw supplied.
<3> To adjust the height, use your own spacer or a stand.

★ **Figure D-1. Method of Inserting Plastic Spacer**



APPENDIX E REVISION HISTORY

The following table shows the revision history up to this edition. The “Applied to:” column indicates the chapter of each edition in which the revision was applied.

(1/2)

Edition	Major Revision from Previous Edition	Applied to:
2nd edition	**1.1 Hardware Configuration** Addition of SWEX-xxxSD-1 to extension probes. Addition of conversion socket for V850E/MA1 (161-pin FBGA). Addition of conversion socket for V850E/MA2 (100-pin LQFP)	**CHAPTER 1 OVERVIEW**
	Change of **1.2 Features (When Connected to IE-V850E-MC-A)** to **1.2 Hardware Specifications (When Connected to IE-V850E-MC-A)**	
	Change of **1.3 Function Specifications (When Connected to IE-V850E-MC-A)** to **1.3 System Specifications of IE-703107-MC-EM1 (When Connected to IE-V850E-MC-A)**	
	Change of **Figure 1-1 System Configuration** to **Figure 1-1 System Configuration (V850E/MA1, 144-Pin LQFP)**	
	Addition of **Figure 1-2 System Configuration (V850E/MA1, 161-Pin FBGA)**	
	Addition of **Figure 1-3 System Configuration (V850E/MA2, 100-Pin LQFP)**	
	1.5 Contents in Carton Addition and modification of description	
	Modification of **Figure 1-4 Contents in Carton**	
	Modification of **Figure 1-5 Connection Between IE-V850E-MC-A and IE-703107-MC-EM1**	
	Modification of **Figure 2-1 IE-703107-MC-EM1**	**CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS**
	Addition and modification of description in **2.1 (6)** to **(10)**	
	2.2 Clock Settings Addition and modification of description	
	Addition of **Figure 2-2 Outline of Clock Settings**	
	Change of **Table 2-1 Clock Setting (When the Emulator is Used as a Stand-Alone Unit)** to **Table 2-1 List of Hardware Settings for Each Clock Setting**	
	Change of **Table 2-2 Clock Setting (When the Emulator is Used in Target System Connection)** to **Table 2-2 Settings When Using Mounted Internal Clock**	
	Addition of **Figure 2-3 Outline When Using Mounted Internal Clock**	
	Addition of **Table 2-3 Settings When Changing Mounted Internal Clock**	
	Addition of **Figure 2-4 Outline When Changing Mounted Crystal Oscillator and Using It as Internal Clock**	
	Addition of **Table 2-4 Settings When Using External Clock**	
	Addition of **Figure 2-5 Outline When Using Crystal Oscillator on Target System as External Clock**	
	Modification of **2.3 MODE Pin Setting** to **2.3 Operation Mode Settings**	
	Addition and modification of description in **2.4 Power Supply Settings**	
	Addition of **2.5 Emulation Memory**	
	Addition and modification of description in **CHAPTER 3 FACTORY SETTINGS**	**CHAPTER 3 FACTORY SETTINGS**
	Addition and modification of description in **CHAPTER 4 CAUTIONS**	**CHAPTER 4 CAUTIONS**

(2/2)

Edition	Major Revision from Previous Edition	Applied to:
2nd edition	Addition of **CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS**	**CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS**
	A.1 Corresponding Package Dimensions • Modification of **(1)** • Addition of **(3)** to **(5)** and **(9)** to **(18)**	**APPENDIX A DIMENSIONS**
	A.2 Conditions for Connecting of In-Circuit Emulator Option Board and Conversion Connector • Addition of **(1)** to **(3)**	
	Change of **(3) Connection between emulator and target system** to **(2) When connecting device using connector for target connection (b) FBGA package**	**APPENDIX B EXAMPLE OF USE OF CONNECTOR FOR TARGET CONNECTION**
	Addition and modification of description in **C.1 Usage (LQFP Package)**	**APPENDIX C CONNECTORS FOR TARGET CONNECTION**
	Addition and modification of description in **C.2 Cautions on Handling Connectors (LQFP Package)**	
	Addition of **C.3 Notes on Board Design (FBGA Package)**	
	Addition of **C.4 Soldering CSSOCKET (Main Enclosure Connector) to Target Board (FGBA Package)**	
	Addition of **C.5 Using LSPACK to Mount IC (FBGA Package)**	
	Addition of **C.6 Connecting In-Circuit Emulator (FBGA Package)**	
	Addition of **C.7 Notes on Handling LSPACK/CSSOCKET (FBGA Package)**	
	Modification of **Figure D-1 Method of Inserting Plastic Spacer**	**APPENDIX D INSERTING PLASTIC SPACER**