EIGHT (1.2 VA) DIGITAL to SYNCHRO/RESOLVER CONVERTERS
4 TWO-SPEED or 8 SINGLE-SPEED or COMBINATION (PROGRAMMABLE)

16 BIT RESOLUTION; To .0083° ACCURACY;
ON-BOARD PROGRAMMABLE REFERENCE SUPPLY
SELF TEST and **Programmable Rotation**

FEATURES:

- 16-bit resolution
- 30 arc-seconds accuracy
- 360 Hz to 10 kHz operation
- 1.2 VA drive capability
- 2,4,6 or 8-channel versions available
- Programmable 2-speed ratios (2 to 255) and angle rotation
- Continuous background BIT testing with Reference and Signal loss detection
- Power-On Self-Test (POST)
- Outputs can be turned ON/OFF
- Either internal or external ±12 VDC supply
- Optional on-board programmable reference supply
- Watchdog timer and soft reset
- Transformer isolated
- No adjustments or trimming required
- Part Number, S/N, Date Code and Revision in permanent memory

DESCRIPTION:

This high density intelligent DSP-based card incorporates up to eight separate transformer isolated Digital-to-Synchro/Resolver converters with 1.2 VA drive, extensive diagnostics, signal & reference loss detection and optional 5 VA reference supply. Either one common or eight separate reference inputs can be specified. Each output can be turned ON or OFF via the bus. Two-speed configuration and constant rotation that includes a start and a stop angle can be programmed. Transformer isolation enables user to ground one of the outputs without affecting performance. The optional on–board reference supply is field programmable for both voltage and frequency. A watchdog timer is provided to monitor the processor. This model will drive passive loads such as CT's etc. Part Number, S/N, Date Code, and Revision are located in permanent memory. The ±12VDC is normally derived from the backplane, but jumpers are supplied to permit the card to be powered from external supplies.

Major diagnostics are incorporated to offer substantial improvements to system reliability because the user is alerted (within 5 seconds) to channel malfunctions. This approach reduces bus traffic because the Status Registers do not require constant polling. See Programming Instructions for further details.

The D2 Test initiates automatic background BIT Testing that compares the output of each channel against the commanded input to a test accuracy of 0.05° and monitors each Output and Reference. Results are available in Status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The D3 Test starts a BIT Test that generates and tests 72 different angles, to a testing accuracy of 0.05°. Results can be read from Status Registers. External reference is required and testing requires no external programming, and can be Initiated or terminated via the bus. CAUTION: Outputs must be ON and are therefore active during this test. Check connected loads for possible interaction.

Power-On Self-Test (POST), if enabled, initiates the D3 Test upon turn-on and is enabled/disabled via the bus.

SPECIFICATIONS (applies to each Channel)

Resolution:	16 bits (.0055°)
Accuracy:	30 arc-seconds (.008°) at 0.3 VA ±1 arc-minute (.017°) at 1.2 VA. No load to full load
Output format:	See part number, transformer isolated
Output voltage:	See code table and part number.
Output load:	1.2 VA max./channel. Short circuit protected (5000 Ω reactive at 90 V_{L-L} Synchro, 90 Ω reactive at 11.8 V_{L-L} Synchro, 110 Ω reactive at 11.8 V_{L-L} Resolver)
Regulation:	5% maximum, no load to Full load
Ratio:	Set any ratio between 2 and 255
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 RPS with a resolution of 0.15°/sec. Step size is 16 bits (0.0055)° up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS.
Reference input voltage:	(See code table and part number) Transformer isolated. 1 ma max./channel
Reference frequency:	360 Hz to 10 kHz (see code table and part number)
Phase shift:	5° max. between output and reference.
Settling time:	Less than 100 microseconds
Power:	+ 5 VDC at 0.4 A ±12 VDC at 1.6 A average, 4 A peak (for 8 channels). Power supplies must be able to supply peak power without current limiting.
Temperature, operating:	0°C to +70°C. Storage temperature: -55°C to +85°C.
Size:	4.5 x13.5 x 0.74 (11.43 x 34.29 x 1.88 cm)
Weight:	12 oz. (.605 kg)

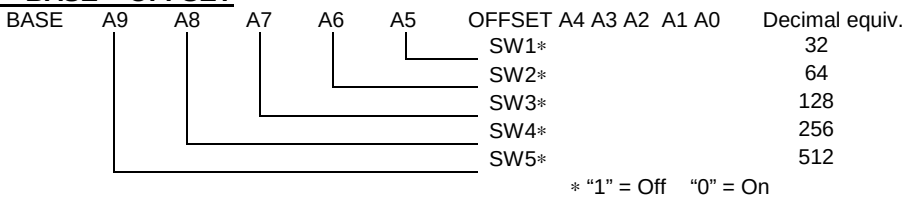
REFERENCE:	Optional (see part number).
Voltage:	2.0 to 28 Vrms programmable (Resolution 0.1Vrms) or 115 Vrms fixed. Accuracy ±2%,
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% maximum, no load to full load.
Output power:	5 VA max. at 40° min. inductive (see part number).

PROGRAMMING:

I/O CONFIGURATION:

This card requires 32 consecutive addresses in the I/O address space on a 32-byte boundary. The base address is switch settable in the 000-3E0 hex (0 to 992) address range.

ADDRESS= BASE + OFFSET



NOTE: Base addresses to avoid:

378-37F	Parallel Printer Port	3B0-3BF	Monochrome Display	3F8-3FF	Asynch Comm I/O	3F0-3F7	Floppy Disk

Page 1 (1E = 0)

00	Ch.1 Lo	write	08	Ch.5 Lo	write	10	Freq. Lo	write/read	1A	Active channels	write/read
01	Ch.1 Hi	write	09	Ch.5 Hi	write	11	Freq. Hi	write/read	1C	Save Lo	write
02	Ch.2 Lo	write	0A	Ch.6 Lo	write	12	Eo Lo	write/read	1D	Save Hi	write
03	Ch.2 Hi	write	0B	Ch.6 Hi	write	13	Eo Hi	write/read	1E	Page register = 0	write
04	Ch.3 Lo	write	0C	Ch.7 Lo	write	14	Status, Reference	read			
05	Ch.3 Hi	write	0D	Ch.7 Hi	write	15	Status, Signal	read			
06	Ch.4 Lo	write	0E	Ch.8 Lo	write	16	Status, Test	read			
07	Ch.4 Hi	write	0F	Ch.8 Hi	write	18	Test (D2) verification	write/read			

Page 2 (1E = 1)

00	Part # Lo read	07	Rev level Hi read	0E	Wrap-around Ch. 4 Lo read	15	Wrap-around Ch. 7 Hi read
01	Part # Hi read	08	Wrap-around Ch. 1 Lo read	0F	Wrap-around Ch. 4 Hi read	16	Wrap-around Ch. 8 Lo read
02	Serial # Lo read	09	Wrap-around Ch. 1 Hi read	10	Wrap-around Ch. 5 Lo read	17	Wrap-around Ch. 8 Hi read
03	Serial # Hi read	0A	Wrap-around Ch. 2 Lo read	11	Wrap-around Ch. 5 Hi read	18	Power-on (POST) read/write
04	Date code Lo read	0B	Wrap-around Ch. 2 Hi read	12	Wrap-around Ch. 6 Lo read	1A/1B	Watchdog timer read/write
05	Date code Hi read	0C	Wrap-around Ch. 3 Lo read	13	Wrap-around Ch. 6 Hi read	1C/1D	Soft reset write
06	Rev level Lo read	0D	Wrap-around Ch. 3 Hi read	14	Wrap-around Ch. 7 Lo read	1E	Page register = 1 write

Page 3 (1E = 2)

00	Stop angle Ch.1 Lo read/write	05	Stop angle Ch.3 Hi read/write	0A	Stop angle Ch.6 Lo read/write	0F	Stop angle Ch.8 Hi read/write
01	Stop angle Ch.1 Hi read/write	06	Stop angle Ch.4 Lo read/write	0B	Stop angle Ch.6 Hi read/write	16	Rotation Complete read
02	Stop angle Ch.2 Lo read/write	07	Stop angle Ch.4 Hi read/write	0C	Stop angle Ch.7 Lo read/write	18	Rotation, Mode write/read
03	Stop angle Ch.2 Hi read/write	08	Stop angle Ch.5 Lo read/write	0D	Stop angle Ch.7 Hi read/write	1A	Test Enable write/read
04	Stop angle Ch.3 Lo read/write	09	Stop angle Ch.5 Hi read/write	0E	Stop angle Ch.8 Lo read/write	1E	Page register = 2 write

Page 4 (1E = 3)

00	Rotate rate Ch.1 Lo read/write	08	Rotate rate Ch.5 Lo read/write	10	Ratio, Ch.1/2 Lo read/write	18	Outputs ON/OFF read/write
01	Rotate rate Ch.1 Hi read/write	09	Rotate rate Ch.5 Hi read/write	11	Ratio, Ch.1/2 Hi read/write	1A	Rotation, Initiate write
02	Rotate rate Ch.2 Lo read/write	0A	Rotate rate Ch.6 Lo read/write	12	Ratio, Ch.3/4 Lo read/write	1C	Rotation, Stop write
03	Rotate rate Ch.2 Hi read/write	0B	Rotate rate Ch.6 Hi read/write	13	Ratio, Ch.3/4 Hi read/write	1E	Page register = 3 write
04	Rotate rate Ch.3 Lo read/write	0C	Rotate rate Ch.7 Lo read/write	14	Ratio, Ch.5/6 Lo read/write		
05	Rotate rate Ch.3 Hi read/write	0D	Rotate rate Ch.7 Hi read/write	15	Ratio, Ch.5/6 Hi read/write		
06	Rotate rate Ch.4 Lo read/write	0E	Rotate rate Ch.8 Lo read/write	16	Ratio, Ch.7/8 Lo read/write		
07	Rotate rate Ch.4 Hi read/write	0F	Rotate rate Ch.8 Hi read/write	17	Ratio, Ch.7/8 Hi read/write		

	D7	D6	D5	D4	D3	D2	D1	D0
Data Hi	180	90	45	22.5	11.25	5.625	2.813	1.406
Data Lo	.703	.352	.176	.088	.044	.022	.011	.0055
Outputs, ON/OFF	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Test Enable	X	X	X	X	D3	D2	X	X
Rotation, Mode	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Rotation, INITIATE	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Rotation, Stop	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Rotation, completed	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Active channels	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Reference	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Signal	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Test	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

At **Power-On** or **System Reset**, all parameters are restored to last saved setup and if POST is enabled**,** a D3 test is initiated.

Enter Active Channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel register at Page 1, 1Ah. "1"=active; "0"=not used. Omitting this step will produce false alarms because unused channels will set faults.

Save Setup: The current setup can be saved by writing 5555h to the Save Register at Page 1, 1C/1Dh. This location will automatically clear to 0000h when the save is completed (within 5 seconds). When save is elected, all parameters are saved, however, any parameter can be changed at will. Saving is optional. If not saved, reenter parameters at each power up.

To restore factory shipped parameters, write AAAAh to the Save Register at Page 1, 1C/1Dh followed by system reset. Note: After a SAVE or RESTORE, Poll Page 1, 1C/1Dh and do not perform any other operation until word is at "0".

Read and Write Angle: For single-speed applications (Ratio=1), in 16-bit mode, write 16-bit binary data (or 16-bit 2's compliment data) to address Page 1, 00h for Ch.1; to 02h for Ch.2 etc. In 8-bit mode, write to offset 00h/01h to 0Eh/0Fh. The Write Registers are double buffered to prevent data ambiguity during 8-bit data transfer. Load data into Hi byte register first, followed by the Lo byte. When reading the wrap around test angles, read the Hi byte first.

Hi byte read holds Lo byte until read (ex. 330°=1110101010101011). For two-speed applications, write only to first channel of channel pair (Coarse speed), and card will set angle of second channel (fine speed), to the Coarse angle multiplied by the ratio. Note: writing to an input angle register will stop any rotation initiated on that channel.

Ratio: Enter the desired ratio, as a binary number, in the Ratio Register corresponding to the pair of channels to be used as a two-speed channel. Example: Single speed = 1; 36:1 = 100100.

ON/OFF: Set the bit corresponding to each channel to be turned on, to "1" in Outputs On/Off Register at page 4, 18h. To turn OFF a channel, set corresponding bit to "0". Default is OFF.

Read Wrap-Around Angles: Read at addresses Page 2, 08h to 17h. AVAILABLE AT ALL TIMES.

Rotation Rate: Write to the corresponding Rotation Rate register a 2's compliment number representing the desired rotation rate, LSB = 0.15°/sec. Ex: 12 RPS =. (12 x 360°/0.15° = 28800 = 7080h), -12 RPS = (-12 x 360°/0.15° = -28800 = 8F80h). Step size is 16 bits (0.0055°) for up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS.

Rotation Mode, Continuous or Start/Stop: For continuous rotation, set the corresponding channel bits to "1" in the register at page 3, 18h. For rotation to cease at a designated stop angle, set the bit to "0".

Stop Angles: Write 16-bit binary data to appropriate address at page 3, 00h to 0Fh. After a channel reaches the stop angle, it will stop rotating and remain at that angle until a new input angle is set. If rotation is initiated again, the angle will start rotating from the present angle.

Initiate Rotation: First set the Rotation Rate Registers and Rotation Mode Register, for each channel that is to rotate. Then, to start rotation for those channels, set the corresponding channel bit to a "1" in the Rotation Initiate Register at page 4, 1Ah.

Stop Rotation: Set the corresponding bit, for each channel to be stopped, to a "1" in the Rotation Stop Register at page 4, 1Ch. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated.

Rotation Completed: Read the Rotation Completed Register at page 3, 16h. Each bit corresponds to a given channel. A "1" = rotation completed, "0"=rotation in process.

Power-On Self-Test (POST) will initiate the D3 test on Power-On, if POST is enabled and saved. Enable by writing "1" or Disable by writing "0" to POST register at page 2, 18h and then save setup.

D2 Test Enable: Writing "1" to D2 of Test Enable Register at page 3, 1Ah initiates automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle, before the output transformer, to the commanded angle, and monitors each Reference and Signal. The status bits will be set to indicate an accuracy problem or Signal/Reference loss and the results can be read from Status Registers within 2 seconds. A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. Outputs must be ON for test to function. Card will write 55h (every 2 seconds) to D2 Test Verify Register at page 1, 18h when D2 is enabled. User can periodically clear to 0000h and then read page 1, 18h again, after 2 seconds, to verify that BIT Testing is activated. This test continuously sequences between the eight channels on the card with each output being measured for approx. 180 mSec. If the measured angle has an error greater the 0.05º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error.

D3 Test Enable: Writing "1" to D3 of Test Enable Register at page 3, 1Ah initiates a BIT Test that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is required and outputs must be ON. The Status bits will be set to indicate an accuracy problem or Signal or Reference loss. Results are available in Status Registers. Test cycle takes about 30 seconds and D3 changes from "1" to "0" when test is complete. The testing requires no external programming, and can be initiated or terminated via the bus. CAUTION: Outputs must be ON during this test and are therefore active. Check connected loads for possible interaction.

Status, Test: Check the corresponding bit of the Test Status Register at page 1, 16h, for status of BIT Testing for each active channel. A ”1” means Accuracy OK; “0” failed (test cycle takes 2 seconds for accuracy error).

Status, Ref: Check the corresponding bit of the Ref Status Register at page 1, 14h, for status of the reference input for each active channel. A ”1” =Ref. ON, “0” = Ref. Loss (Reference loss is detected after 2 seconds).

Status, Sig: Check the corresponding bit of the Sig Status Register at page 1, 15h, for status of the input signals for each active channel. A "1" = Signal ON, “0” = Signal loss (Signal loss is detected after 2 seconds).

Soft Reset (Level sensitive): Writing “1” to page 2, 1Ch/1Dh initiates and holds software reset state. Then, writing “0” initiates reboot (takes 400 ms). This function is equivalent to a power-on self-test.

Watchdog Timer: This feature monitors the watchdog timer register at page 2, 1A/1Bh. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. User, after 100 µSec. should look for the inverted code to confirm that the processor is operating.

Optional Reference Supply: For frequency, write a 16-bit word (Ex: 400 Hz = 1 1001 0000) to address page 1, 10/11h. For voltage, write an 16-bit word (Ex: 26.1 Vrms =1 0000 0101) with Lsb=0.1 Vrms, to address page 1, 12/13h. It is recommended that user program the required frequency before setting the output voltage.

Serial Number: At page 2, 02/03h, is read as a 16-bit binary word.

Date Code: Read as a decimal number at page 2, 04/05h. The four digits represent YYWW (Year,Year,Week.Week

Rev: At page 1, 06/07h.
Example

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1
DSP Rev 1.1						FPGA Rev 3						PC Rev 1			

Front panel Connectors:

DC37P, Mate: DC37S **This connector is used when six (6) or fewer channels are specified**

Pin	Ch. 1	Pin	Ch. 2	Pin	Ch. 3	Pin	Ch. 4	Pin	Ch. 5	Pin	Ch. 6	Pin	
19	S1	16	S1	13	S1	10	S1	7	S1	4	S1	1	Chassis
37	S2	34	S2	31	S2	28	S2	25	S2	22	S2		
18	S3	15	S3	12	S3	9	S3	6	S3	3	S3		
36	S4	33	S4	30	S4	27	S4	24	S4	21	S4		
17	RHi	14	*RHi	11	*RHi	8	*RHi	5	*RHi	2	*RHi		
35	RLo	32	*RLo	29	*RLo	26	*RLo	23	*RLo	20	*RLo		

DD-50P, Mate: DD-50S **This connector is used when seven (7) or eight (8) channels are specified**

Pin	Ch. 1	Pin	Ch. 2	Pin	Ch. 3	Pin	Ch. 4	Pin	Ch. 5	Pin	Ch. 6	Pin	Ch. 7	Pin	Ch. 8	Pin	
16	S1	32	S1	29	S1	26	S1	23	S1	20	S1	2	S1	8	S1	14	RefHi
17	S2	48	S2	45	S2	42	S2	39	S2	36	S2	3	S2	9	S2	1	RefLo
15	S3	31	S3	28	S3	25	S3	22	S3	19	S3	4	S3	10	S3		
50	S4	47	S4	44	S4	41	S4	38	S4	35	S4	5	S4	11	S4		
33	RHi	30	*RHi	27	*RHi	24	*RHi	21	*RHi	18	*RHi	6	*RHi	12	*RHi		
49	RLo	46	*RLo	43	*RLo	40	*RLo	37	*RLo	34	*RLo	7	*RLo	13	*RLo		

S4 pins used only with Resolvers. Do not connect to any undesignated pins.

*These inputs are supplied as individual reference inputs ONLY when specified in the part number.

The Standard output connector for a 2, 4, or 6 channel card, is the 37 pin (DC-37P) connector, however the 50 pin (DD-50P) connector can be ordered as an option, allowing separate pins for the output of the on board reference.

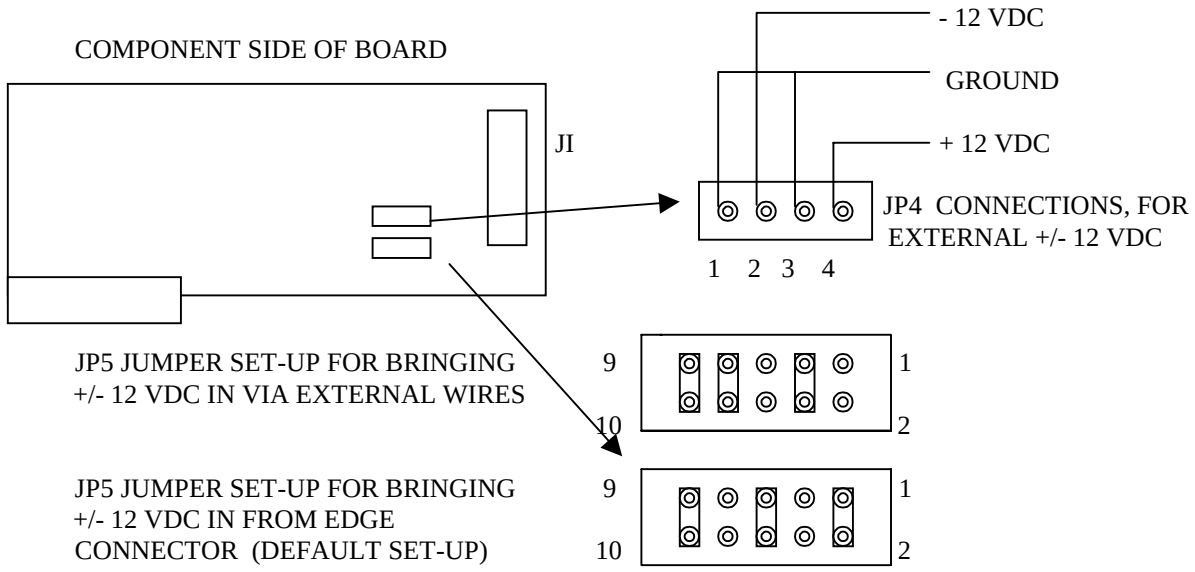
The Standard output connector for a 8 channel card, is the 50 pin (DC-50P) connector.

For the 37 pin connector, the reference is brought IN on pins 17 & 35 (without the optional internal reference). If the optional internal reference generator is specified, this internal reference will come OUT on pins 17 & 35.

For the 50 pin connector, the reference is brought IN on pins 33 & 49 (without the optional internal reference). If the optional internal reference generator is specified, this internal reference will come OUT on pins 33 & 49 AND on pins 14 & 1.

EXTERNAL +/- 12VDC: The card is shipped, configured for operation from +/- 12 VDC power supplied from edge connector. To operate from External +/- 12VDC supplies: From jumper block JP5, remove jumpers 1-2, and 5-6, then connect jumpers 3-4 , and 7-8. Leave jumper 9 – 10 connected.
Connect external +12 VDC to JP4-4 (labeled +12), connect external –12 VDC to JP4-2 (labeled –12) and external grounds to JP4-1 and JP4-3 (common tie points)

CONNECTIONS FOR BRINGING +/- 12 VDC INTO THE CARD FROM AN EXTERNAL SOURCE



Code Table

Code	Output (VL-L)	Ref (Vrms)	Frequency (Hz)	Load (VA)	Notes
01	11.8	26	400	1.2	
02	90	115	400	1.2	
25	2.0	2.0	7200	1.2	
26	2.0	6.0	4000	1.2	
27	2.0	8.0	2400	1.2	
28	2.0	11.8	2400	1.2	
29	3.5	7.07	3000	1.2	
31	6.8	115	400	1.2	
32	10.0	10.0	400	1.2	
33	11.8	11.8	2500	1.2	
34	11.8	115	400	1.2	
50	11.8 11.8	26 115	400 400	1.2 1.2	Channel 1 Channel 2
51	26 2.0	26 6.0	400 4000	1.2 1.2	Channels 1 and 2 Channels 3 to 8
52	2.5	5.0	2900	1.2	
53	26	26	400	1.2	2 ch resolver
54	7	7	400	1.2	4 ch resolver
55	1.5	3.0	2048		50 ma drive

PART NUMBER DESIGNATION

77DS1 - X X X X X X - XX

TOTAL NUMBER OF CHANNELS
2 = 2 D/S Channels
4 = 4 D/S Channels
6 = 6 D/S Channels
8 = 8 D/S Channels

ENVIRONMENTAL
C = No Conformal Coating
K = Removable Conformal Coating

FORMAT
S = Synchro
R = Resolver
M = Mixed (See Code Table)
P = S/R Programmable

ISA BUS
1 = 8-Bit ISA Bus
2 = 16-Bit ISA Bus

CODE (See Code Table)

OPTIONS 2
0 = None

9 = Custom Design (See Separate Spec)

OPTIONS 1

With On-Board Reference:
1 = One Common Reference Input Tied to the On-Board Reference Supply
2 = Individual Reference Inputs
5 = 2, 4, or 6 channels with Optional 50 Pin connector, with separate pins for reference output

Without On-Board Reference:
3 = One Common Reference Input
4 = Individual Reference Inputs