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256K x 4 Monolithic VideoRAM

MVM4256K/T/V-10/12/15

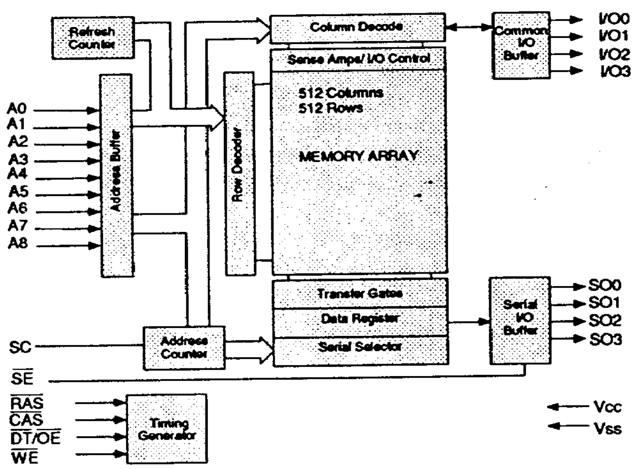
Issue 3.1: November 1991

262,144 x 4 CMOS High Speed Video Dynamic RAM

Features

- RAM Access Time of 100,120,150 ns
- SAM Access Time of 35,40, 50ns
- 5 Volt Supply ± 5%
- 512 Refresh Cycles (8 ms)
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
- $\overline{\text{RAS}}$ only Refresh
- Hidden Refresh
- Fast Page Mode Capability
- Directly TTL Compatible
- May Be Processed to MIL-STD-883B RevC

Block Diagram



Pin Definition

Package Types: 'K','T','V'

SC	1	28	GND
SI/O0	2	27	SI/O3
SI/O1	3	26	SI/O2
$\overline{\text{DT/OE}}$	4	25	$\overline{\text{SE}}$
I/O0	5	24	I/O3
I/O1	6	23	I/O2
$\overline{\text{WE}}$	7	22	NC
NC	8	21	$\overline{\text{CAS}}$
$\overline{\text{RAS}}$	9	20	NC
A8	10	19	A0
A6	11	18	A1
A5	12	17	A2
A4	13	16	A3
Vcc	14	15	A7

Pin Functions

A0-A8	Address Inputs
I/O0-3	RAM Data Input/Output
SI/O0-3	SAM Data Input/output
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{DT/OE}}$	Data Transfer/Output Enable
$\overline{\text{WE}}$	Read/Write Input
SC	Serial Clock
$\overline{\text{SE}}$	SAM Enable
V_{cc}	Power (+5V)
GND	Ground
NC	No Connect

Package Details

Pin Count	Description	Package Type	Material	Pinout
28	400 mil Dual-in-Line(DIP)	K	Ceramic	JEDEC
28	300 mil Dual-in-Line(DIP)	T	Ceramic	JEDEC
28	100 mil Vertical-in-Line(VIL)	V	Ceramic	JEDEC

Package Dimensions and details on page 22.

VIL is a trademark of Mosaic Semiconductor Inc., Patent Number D316251

Operation of RAM Port

RAM Read Cycle

(DT/OE high, CAS high, at the falling edge of RAS)

At the falling edge of RAS the row address is entered and at the falling edge of CAS the column address is entered. When WE is high, DT/OE is low, and CAS is low, data from the selected address is output onto the I/O pin. At the falling edge of RAS, DT/OE and CAS go high. t_{AA} and t_{RAD} timings are added to enable high speed page mode.

RAM Write Cycle

(DT/OE high, CAS high, at the falling edge of RAS)

Normal Mode:

(WE high at the falling edge of RAS)

A write cycle is executed when CAS and WE are set low after RAS is set low. Once all 4 I/Os are written, WE should be high at the falling edge of RAS to change to mask write mode.

An early write cycle occurs when WE is set low before the falling edge of CAS. At the CAS falling edge, data is entered. I/O is in high impedance.

A delayed write cycle occurs when WE is set low after the falling edge of CAS. Data is input at the falling edge of WE. Data should be entered when OE is high because I/O does not become high impedance.

A read-modify-write cycle occurs when WE is set low after the falling edge of CAS and after t_{CWD}(min) and t_{AWD}(min). This cycle allows a write operation after a read operation in the same address cycle. To avoid I/O contention, data should be input after a read and OE set high.

Mask Write Mode:

(WE low at the falling edge of RAS)

This cycle allows data to be written only to selected I/O. The I/O level (mask data) at the falling edge of RAS determines whether or not I/O is written. The data is written in high I/O pins and masked in low I/O pins. Internal data is preserved and masked data is available during the RAS cycle.

High Speed Page Mode Cycle

(DT/OE high, CAS high, at the falling edge of RAS)

During this cycle, the device can read or write the data of the same row address by toggling CAS with RAS low. This page mode cycle time is one third of the random read/write cycle time. Because this device is based on a static column mode, t_{AA}, t_{RAD}, and t_{ACP} have been added. 512-word memory cells can be accessed in one RAS cycle. Access frequency must be specified within t_{RAS} max.

Transfer Cycles

The data transfer cycles available in this device are the read transfer, the pseudo transfer, and the write transfer cycles. They are enabled by driving DT/OE low after the falling edge of RAS. These cycles can determine the first SAM address to access after transferring at the column address. CAS does not need to be set and the SAM start address can be latched internally, as long as this SAM address is not changed.

Read Transfer Cycle

(CAS high, DT/OE low, WE high, at the falling edge of RAS)

During this cycle, the row address data is transferred synchronously at the rising edge of DT/OE. After this point, the new address data outputs from the SAM start address determined by the column address.

Serial SAM access during transfer is possible during this cycle (real time data transfer). Here, t_{SDD} (min) is specified between the last SAM access before transfer and DT/OE rising edge. t_{SDH} (min) is specified between the first SAM access and DT/OE rising edge.

Once a read transfer cycle has been executed, SI/O goes into an output mode.If the previous transfer cycle is a pseudo transfer or a write transfer and SI/O is in input mode, inputs should be set at high impedance before t_{RLZ} (min) after the falling edge of RAS. This will avoid data contention.

Pseudo Transfer Cycle

(CAS high, DT/OE low, WE low, SE high at the falling edge of RAS)

To avoid data in RAM being rewritten, this cycle allows the SI/O to be switched from output to input mode. The output buffer in SI/O becomes high impedance within t_{SRZ} (max.) from the falling edge of RAS. Data should be input into SI/O after t_{SID} (min.) to avoid data contention. SAM access is enabled after t_{SRD}(min.). During RAS low, SAM access is inhibited. Thus, SC should be kept low.

Write Transfer Cycle

(CAS high, DT/OE low, WE low, SE low at the falling edge of RAS)

During this cycle, a row of data input can be transferred by serial write cycle to RAM. The address at the falling edge of RAS determines the row address of the transferred data. The column address is specified as the first address to serial write after completing this cycle. SAM access is enabled after t_{SRD}(min.). While RAS is low, SAM access is inhibited. Thus, SC should be kept low.

Refresh Cycles

Because the RAM portion of this device is composed of dynamic circuits, refresh is required to retain data. Refresh is achieved by accessing all 512 row addresses every 8mS. However, any cycle that activates RAS can refresh the row address. Therefore, a refresh cycle is not required for accessing all row addresses.

During a RAS Only refresh cycle, refresh is achieved by activating a RAS cycle, with CAS set high, by inputting the refresh/row address through external circuits. Output is in high impedance state during this cycle. DT/OE should be high at the falling edge of RAS to differentiate this cycle from a data transfer cycle.

A CAS Before RAS refresh is performed by activating CAS before RAS. In this cycle, a refresh address is provided by an internal address counter. Outputs are in high impedance.

A Hidden Refresh cycle is initiated by reactivating RAS when DT/OE and CAS remain low in normal RAM read cycles.

Operation of SAM Port

Serial Read Cycle

When the previous data transfer cycle is a read transfer cycle, the SAM port is in read mode. Access is synchronized with SC rising. SAM data is output from SI/O. SI/O becomes high impedance if $\overline{SE}$ is set high. The internal pointer will be incremented at the rising edge of SC.

Serial Write Cycle

The SAM port is in write mode when the previous data transfer cycle is pseudo transfer or write transfer. During this cycle, SI/O data is programmed into the data register at the rising edge of SC. If $\overline{SE}$ is high, SI/O data will not be input into the data register. The internal pointer is incremented at the rising edge of SC, so $\overline{SE}$ high can mask data for SAM.

OPERATION CYCLES

$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	Operation Cycle
H	H	H	X	RAM Read/Write
H	H	L	X	Mask Write
H	L	H	X	Read Transfer
H	L	L	H	Pseudo Transfer
H	L	L	L	Write Transfer
L	X	X	X	CBR Refresh

X: Don't Care   Input Levels: falling edge of $\overline{RAS}$

Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_t	-1 V to +7	V
Power Dissipation	P_t	1.0	W
Storage Temperature	T_{stg}	-55 to +150	°C

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{cc}	4.75	5.0	5.75	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V
Operating Temperature	T_a	0	-	70	°C
	T_{al}	-40	-	85	°C (**)
	T_{am}	-55	-	125	°C (**)

*-3.0V for a pulse width ≤ 10ns
**RAM Port Access Times

Capacitance (V_{cc}=5V±5%, T_a=25°C)

Parameter		*Symbol*	*typ*	*max*	*Unit*	*Notes*
Input Capacitance:	Address	C_{I1}	-	5	pF	1
Input Capacitance:	Clocks	C_{I2}	-	5	pF	1
I/O Capacitance:	Data-in/out	$C_{I/O}$	-	7	pF	1,2

Notes: 1. Capacitance calculated, not measured.
2. $\overline{CAS}$=V_{IH} to disable Dout.

DC Electrical Characteristics(T_a = 0 to 125°C, V_{CC} = 5V+5%)

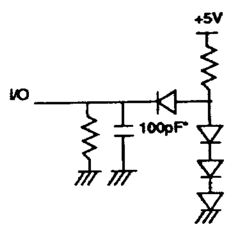
Parameter	Symbol	Test Condition RAM Port	Test Condition SAM Port	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Operating Current 1,2	I_{cc1}	$\overline{RAS}$,$\overline{CAS}$ cycling t_{RC}=min.	$\overline{SE}$=V_{IH},SC=V_{IL}	-	70	-	60	-	55	mA
			$\overline{SE}$=V_{IL}, SC cycling t_{SCC}=min.	-	120	-	100	-	85	mA
$\overline{RAS}$ Only Refresh Current,1	I_{cc3}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min.	$\overline{SE}$=V_{IH},SC=V_{IL}	-	70	-	60	-	55	mA
			$\overline{SE}$=V_{IL},SC cycling t_{SCC}=min.	-	120	-	100	-	85	mA
$\overline{CAS}$ before $\overline{RAS}$ Refresh Current	I_{CC5}	$\overline{RAS}$ cycling, t_{RC} min.	$\overline{SE}$=V_{IH},SC=V_{IL}	-	60	-	50	-	40	mA
	I_{CC11}		$\overline{SE}$=V_{IL},SC cycling t_{SCC}=min.	-	110	-	90	-	70	mA
Page Mode Current,1,3	I_{cc7}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling, t_{RC}=min.	$\overline{SE}$=V_{IH},SC=V_{IL}	-	80	-	70	-	60	mA
			$\overline{SE}$=V_{IL},SC cycling t_{SCC}=min.	-	130	-	110	-	90	mA
Data Transfer Current,2	I_{CC6}	$\overline{RAS}$,$\overline{CAS}$ t_{RC}=min.	$\overline{SE}$=V_{IH},SC=V_{IL}	-	95	-	90	-	85	mA
	I_{CC12}		$\overline{SE}$=V_{IL},SC cycling t_{SCC}=min.	-	135	-	125	-	115	mA
Standby Current,1	I_{cc2}	$\overline{RAS}$,$\overline{CAS}$ =V_{IH}	$\overline{SE}$=V_{IH},SC=V_{IL}	-	7	-	7	-	7	mA
	I_{CC8}		$\overline{SE}$=V_{IL},SC cycling t_{SCC}=min.	-	55	-	55	-	40	mA
Input Leakage	I_{LI}	V_{IN}=0 to +7V		-10	10	-10	10	-10	10	µA
Output Leakage	I_{LO}	V_{out}=0 to +7V, Dout is disabled.		-10	10	-10	10	-10	10	µA
Output Levels	V_{OH}	I_{out}=-2mA		2.4	-	2.4	-	2.4	-	V
	V_{OL}	I_{out}=4.2mA		-	0.4	-	0.4	-	0.4	V

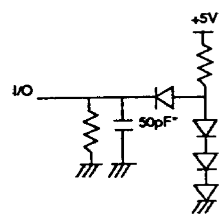
Note 1: Icc depends on output loading condition when the device is selected,Icc max. is specified at the output open condition.
2: Address can be changed less than three times while RAS=V_{IL}.
3: Address can be changed once or less while CAS=V_{IH}.

AC Test Conditions

- Input pulse levels: 0.8 to 2.4V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 0.4V, 2.4V
- Output load: 2 TTL gates + 100pF

Output Load Circuits



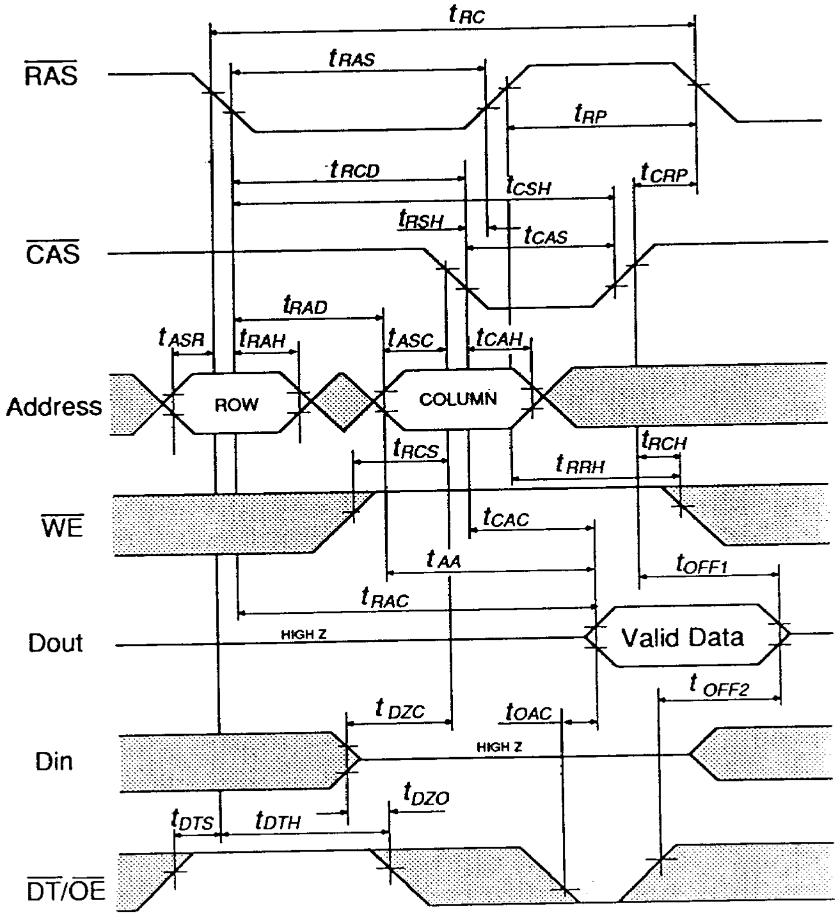


* Including jig and scope

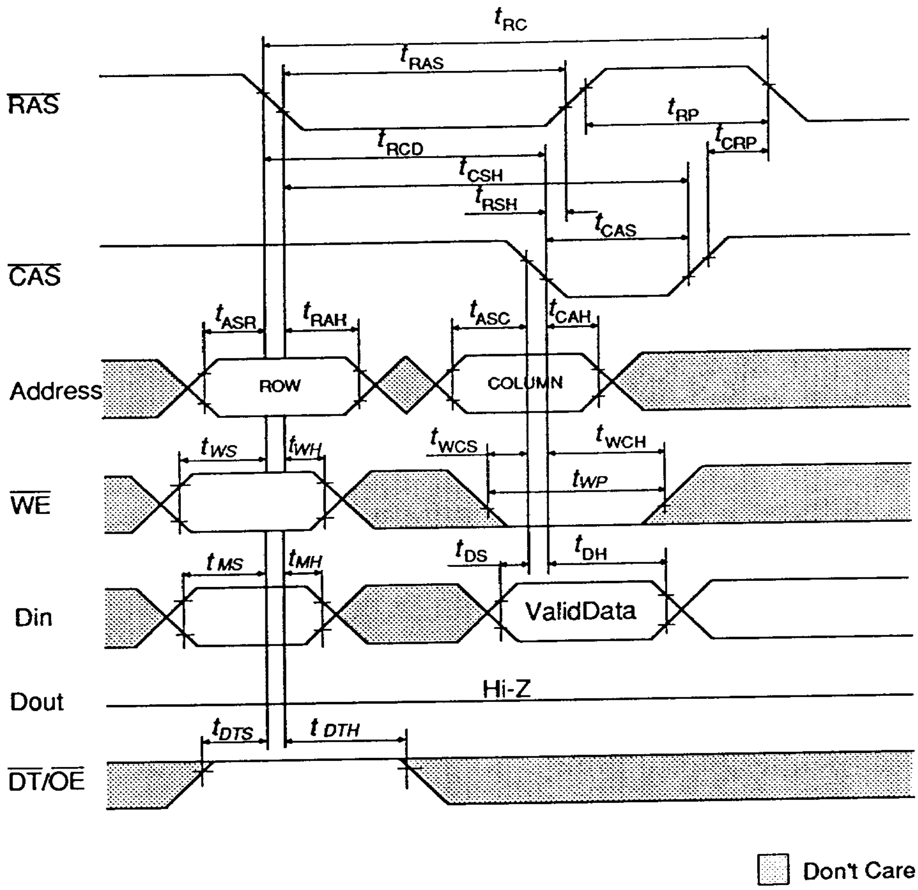
Common Timing Parameters

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
Random Read or Write Cycle Time	t_{RC}	190	-	220	-	260	-	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	-	90	-	100	-	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	35	10000	40	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	85	30	110	ns	5,6
$\overline{RAS}$ Hold Time	t_{RSH}	30	-	35	-	40	-	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	-	120	-	150	-	ns	
$\overline{CAS}$ to RAS Precharge Time	t_{CRP}	10	-	10	-	10	-	ns	
Row Address Setup Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	15	-	15	-	20	-	ns	
Column Address Setup Time	t_{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t_{CAH}	20	-	20	-	25	-	ns	
Transition rise to fall time	t_T	3	50	3	50	3	50	ns	8
Refresh Period (512 Cycles)	t_{REF}	-	8	-	8	-	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	-	0	-	0	-	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	-	15	-	20	-	ns	
Data-in to $\overline{OE}$ Delay	t_{DZO}	0	-	0	-	0	-	ns	
Data-in to $\overline{CAS}$ Delay	t_{DZC}	0	-	0	-	0	-	ns	

Read Cycle



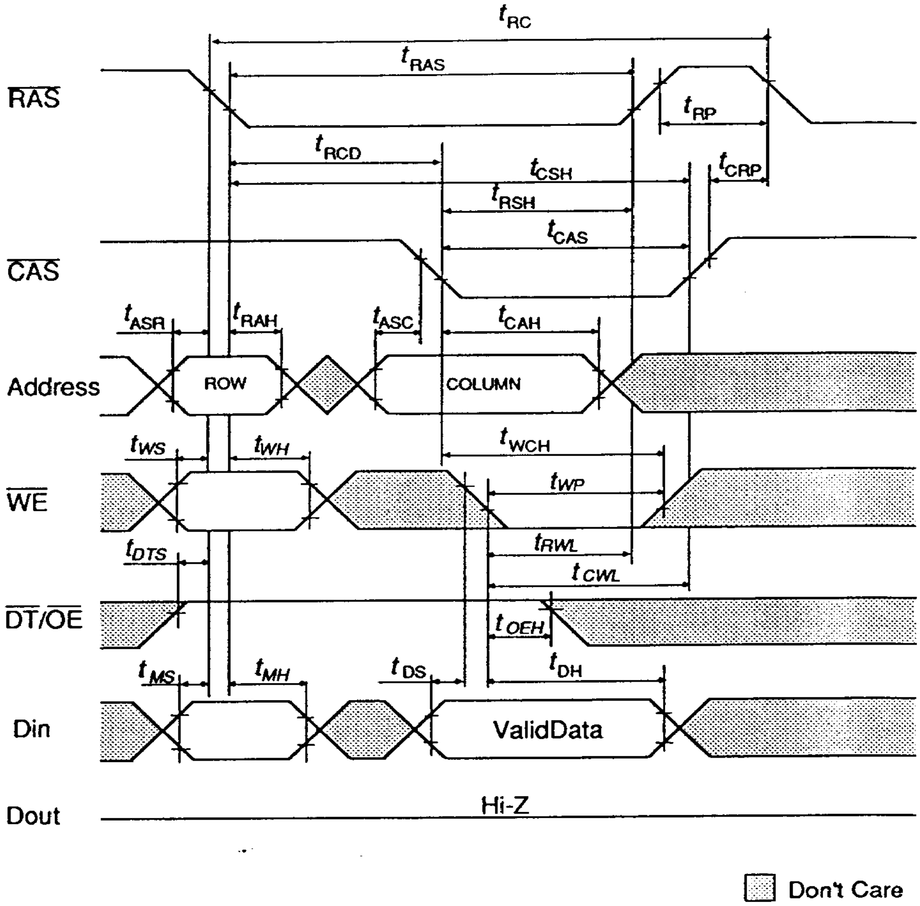
Early Write Cycle Timing Waveform



Notes:

1. When $\overline{WE}$ is high, all data on I/O's can be written into memory. When $\overline{WE}$ is low, data is not written into memory except when the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle Timing Waveform



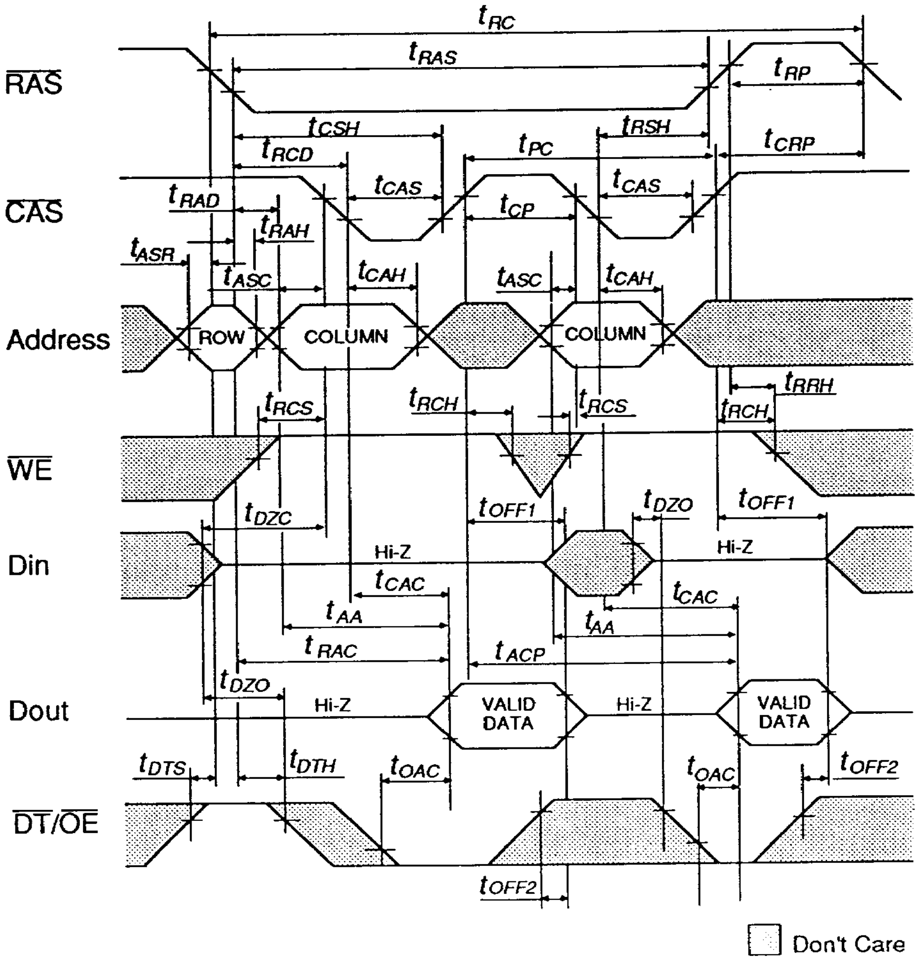
Notes:

1. When $\overline{WE}$ is high, all data on I/O's can be written into memory. When $\overline{WE}$ is low, data is not written into memory except when the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
Access Time from $\overline{RAS}$	t_{RAC}	-	100	-	120	-	150	ns	2,3
Access Time from $\overline{CAS}$	t_{CAC}	-	30	-	35	-	40	ns	3,5
Access Time from $\overline{OE}$	t_{OAC}	-	30	-	35	-	40	ns	3
Address AccessTime	t_{AA}	-	45	-	55	-	70	ns	3,6
Output Turnoff Delay (Referenced to $\overline{CAS}$)	t_{OFF1}	-	25	-	30	-	40	ns	7
Output Turnoff Delay (Referenced to $\overline{OE}$)	t_{OFF2}	-	25	-	30	-	40	ns	7
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time	t_{RCH}	0	-	0	-	0	-	ns	12
Read Command Hold Time	t_{RRH}	10	-	10	-	10	-	ns	12
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	65	25	80	ns	5,6
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	-	50	-	60	-	75	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	-	15	-	20	-	ns	
Page Mode Cycle Time	t_{PC}	55	-	65	-	80	-	ns	

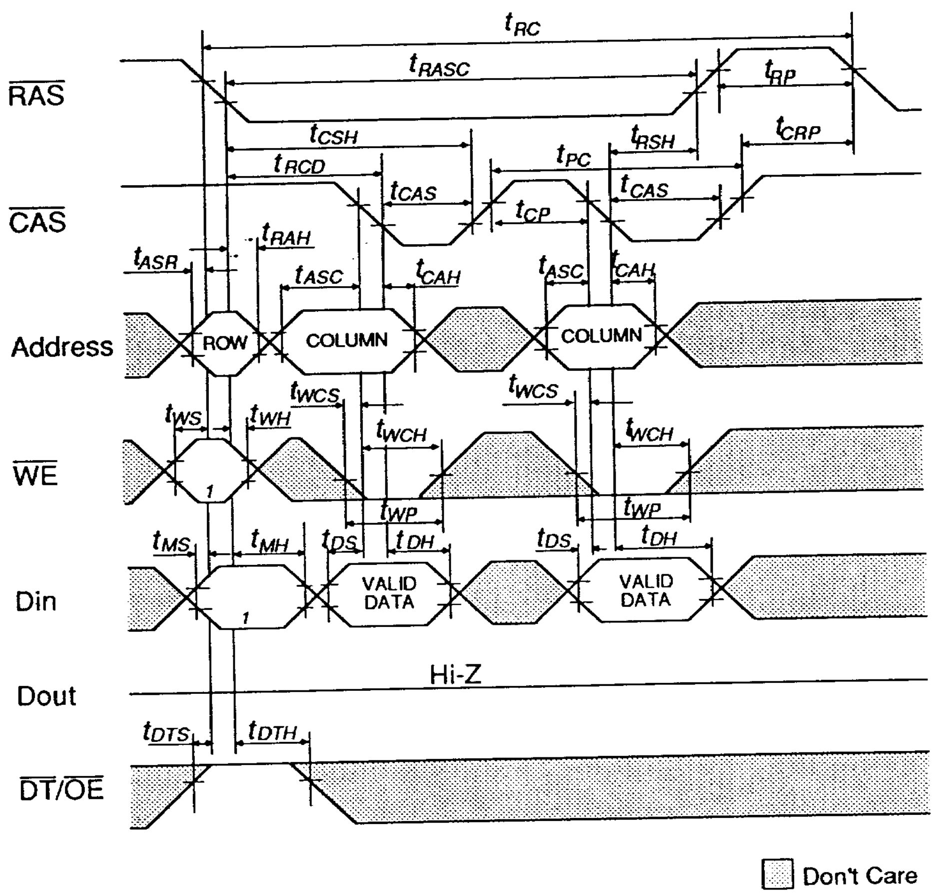
Page Mode Read Cycle Timing Waveform



Page Mode Write Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
Write Command Setup Time	t_{WCS}	0	-	0	-	0	-	ns	9
Write Command Hold Time	t_{WCH}	25	-	25	-	30	-	ns	
Write Command Pulse Width	t_{WP}	15	-	20	-	25	-	ns	
Write Command to RAS Lead Time	t_{RWL}	30	-	35	-	40	-	ns	
Write Command to CAS Lead Time	t_{CWL}	30	-	35	-	40	-	ns	
Data in Setup Time	t_{DS}	0	-	0	-	0	-	ns	10
Data in Hold Time	t_{DH}	25	-	25	-	30	-	ns	10
WE to RAS Setup Time	t_{WS}	0	-	0	-	0	-	ns	
WE to RAS Hold Time	t_{WH}	15	-	15	-	20	-	ns	
Mask Data to RAS Setup Time	t_{MS}	0	-	0	-	0	-	ns	
Mask Data to RAS Hold Time	t_{MH}	15	-	15	-	20	-	ns	
OE Hold Time (Referenced to WE)	t_{OEH}	10	-	15	-	20	-	ns	
Page Mode Cycle Time	t_{PC}	55	-	65	-	80	-	ns	
CAS Precharge Time	t_{CP}	10	-	15	-	20	-	ns	

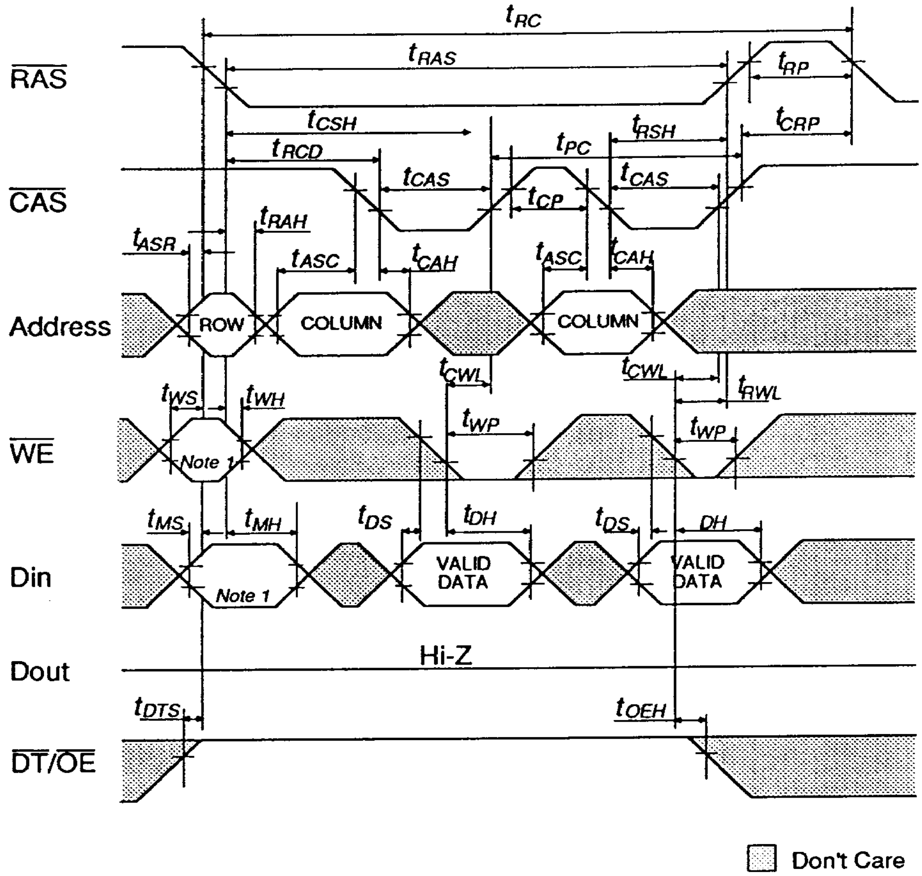
Page Mode Early Write Cycle Timing Waveform



Notes:

1. When WE is high, all data on I/O's can be written into memory. When WE is low, data is not written into memory except when the I/O is high at the falling edge of RAS.

Page Mode Delayed Write Cycle Timing Waveform



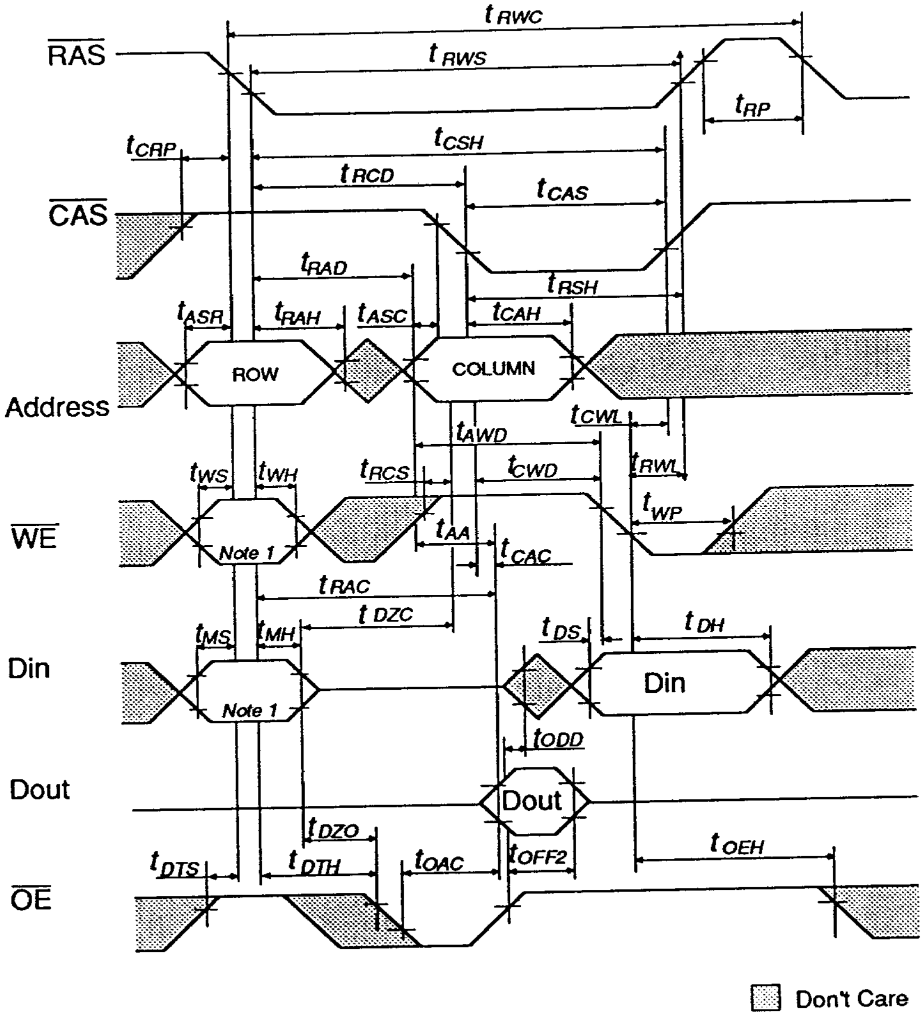
Notes:

1. When $\overline{WE}$ is high, all data on I/O's can be written into memory. When $\overline{WE}$ is low, data is not written into memory except when the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
Read Modify Write Cycle Time	t_{RWC}	255	-	295	-	350	-	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	-	75	-	90	-	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	-	95	-	120	-	ns	9
$\overline{OE}$ to Data-in Delay	t_{ODD}	25	-	30	-	40	-	ns	
Access Time from $\overline{RAS}$	t_{RAC}	-	100	-	120	-	150	ns	2,3
Access Time from $\overline{CAS}$	t_{CAC}	-	30	-	35	-	40	ns	3,5
Access Time from $\overline{OE}$	t_{OAC}	-	30	-	35	-	40	ns	3
Address Access Time	t_{AA}	-	45	-	55	-	70	ns	3,6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	65	25	80	ns	5,6
Output Buffer Turn-off Delay	t_{OFF2}	-	25	-	30	-	40	ns	
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	ns	
Write Command Pulse Width	t_{WP}	15	-	20	-	25	-	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	-	35	-	40	-	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	-	35	-	40	-	ns	
Data in Setup Time	t_{DS}	0	-	0	-	0	-	ns	10
Data in Hold Time	t_{DH}	25	-	25	-	30	-	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	-	0	-	0	-	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	-	15	-	20	-	ns	
$\overline{OE}$ Hold Time (referenced to $\overline{WE}$)	t_{OEH}	10	-	15	-	20	-	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	-	0	-	0	-	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	-	15	-	20	-	ns	

Read-Modify-Write Cycle Timing Waveform



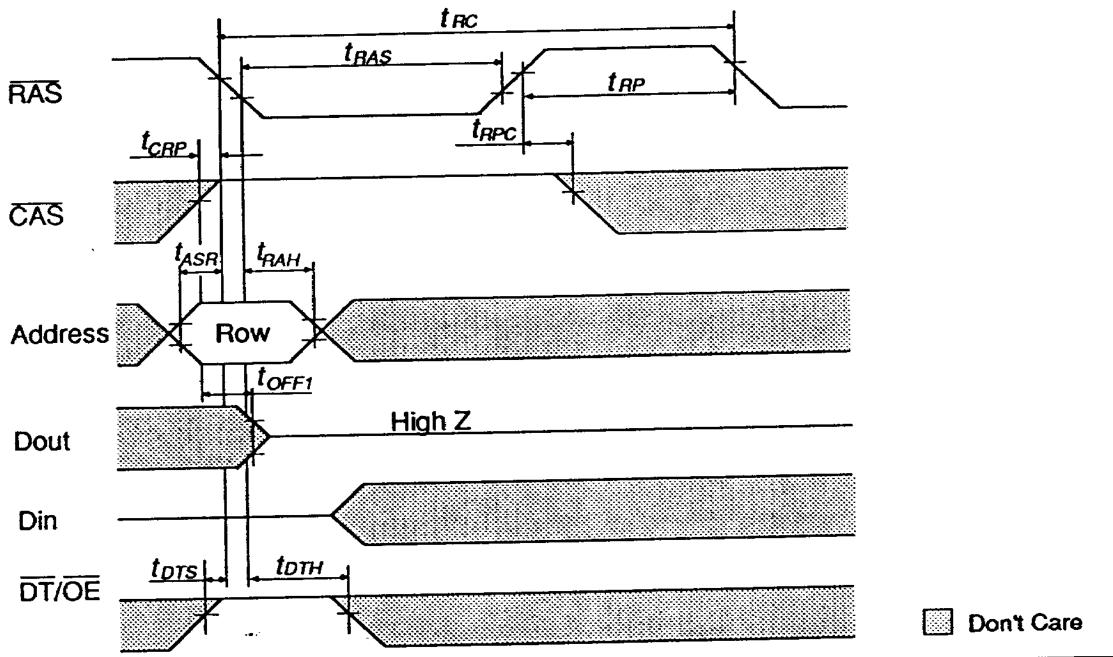
Notes:

1. When $\overline{WE}$ is high, data on I/O's can be written into memory. When $\overline{WE}$ is low, data on I/O's are not written except when the I/O is high at the falling edge of $\overline{RAS}$.

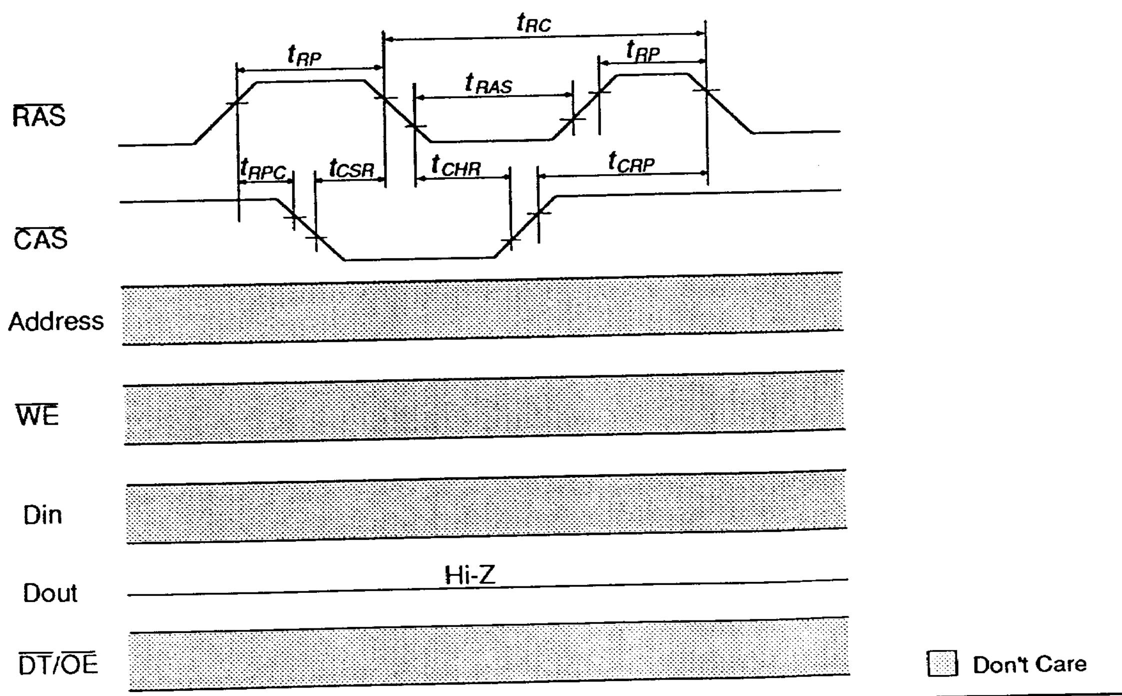
Refresh Cycle Timing

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{CSR}	10	-	10	-	10	-	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{CHR}	20	-	25	-	30	-	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	10	-	10	-	10	-	ns	

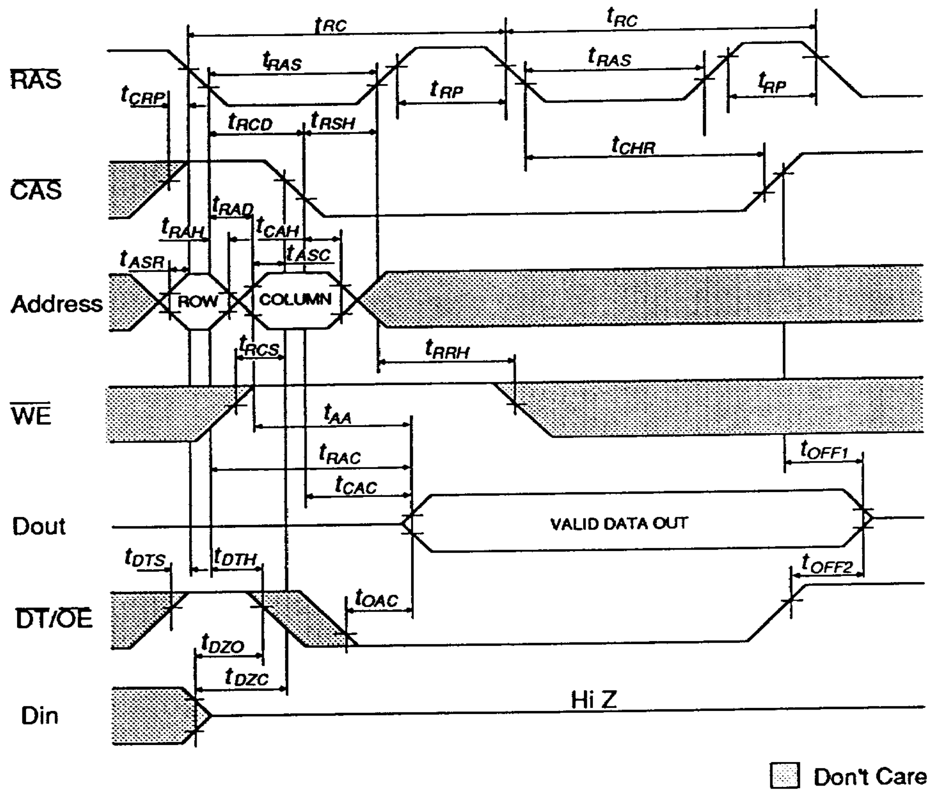
$\overline{\text{RAS}}$-Only Refresh Cycle Timing Waveform



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle Timing Waveform



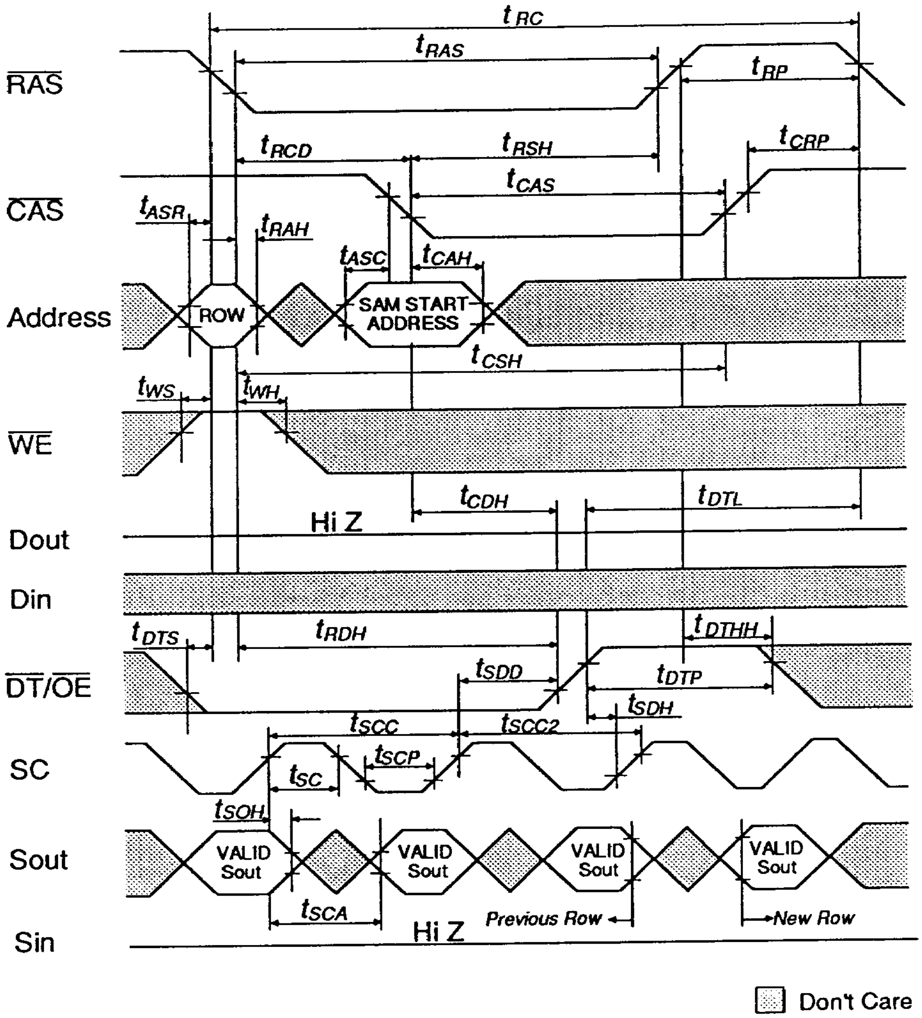
Hidden Refresh Cycle Timing Waveform



Transfer Cycle Timing

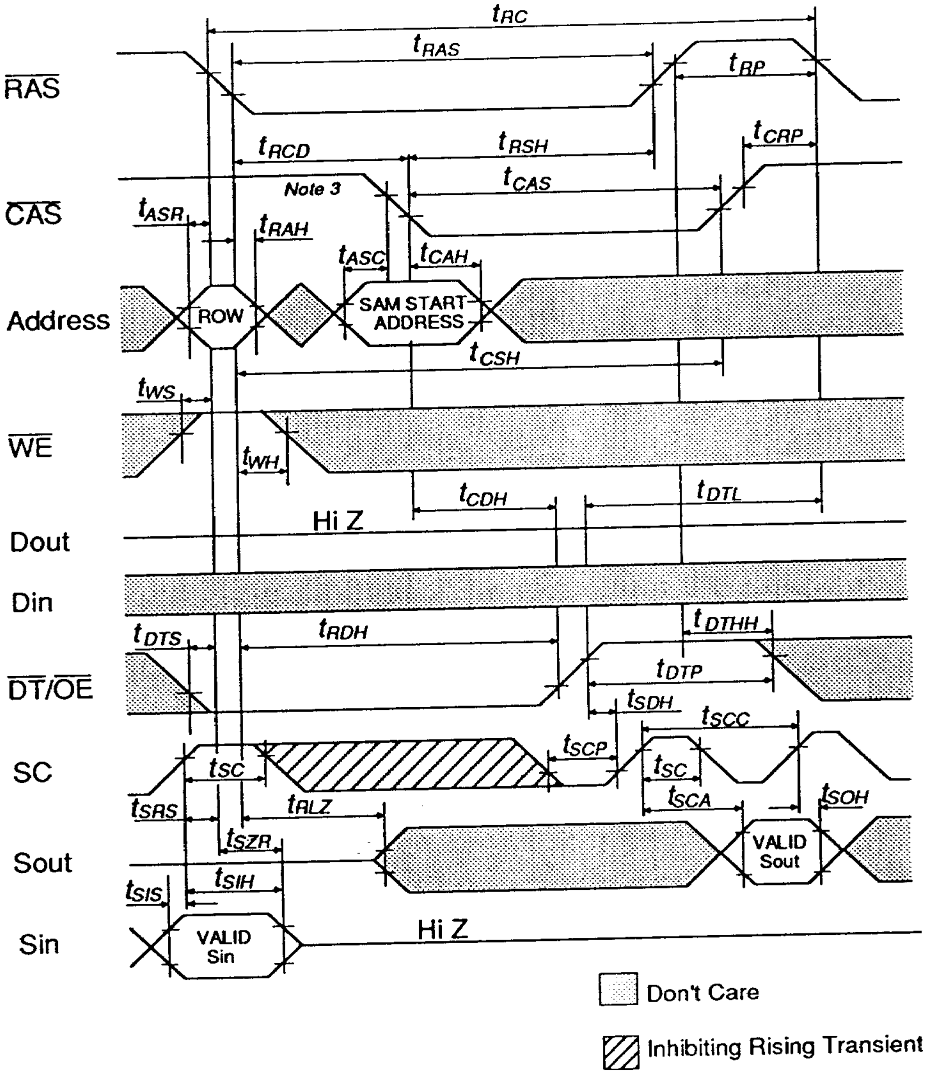
Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	-	0	-	0	-	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	-	15	-	20	-	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	-	0	-	0	-	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	-	15	-	20	-	ns	
$\overline{RAS}$ to SC Delay	t_{SRD}	30	-	30	-	35	-	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	40	-	40	-	45	-	ns	
$\overline{DT}$ Hold Time from $\overline{RAS}$	t_{RDH}	90	-	90	-	110	-	ns	
$\overline{DT}$ Hold Time from $\overline{CAS}$	t_{CDH}	30	-	30	-	45	-	ns	
Last SC to $\overline{DT}$ Delay	t_{SDD}	5	-	5	-	10	-	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	-	25	-	30	-	ns	
$\overline{DT}$ to $\overline{RAS}$ Lead Time	t_{DTL}	50	-	50	-	50	-	ns	
$\overline{DT}$ Hold Time (Referenced to $\overline{RAS}$ High)	t_{DTHH}	25	-	25	-	30	-	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	35	-	35	-	40	-	ns	
Serial Data Input Delay from $\overline{RAS}$	t_{SID}	60	-	60	-	75	-	ns	
Serial Data Input to $\overline{RAS}$ Delay	t_{SZR}	-	10	-	10	-	10	ns	
Serial Output Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to Sout in Low Z Delay	t_{RLZ}	10	-	10	-	10	-	ns	
Serial Clock Cycle Time	t_{SCC}	40	-	40	-	60	-	ns	
Access Time from SC	t_{SCA}	-	40	-	40	-	50	ns	4
Serial Data Out Hold Time	t_{SOH}	7	-	7	-	7	-	ns	4
SC Pulse Width	t_{SC}	10	-	10	-	10	-	ns	
SC Precharge Time	t_{SCP}	10	-	10	-	10	-	ns	
Serial Data in Setup Time	t_{SIS}	0	-	0	-	0	-	ns	
Serial Data in Hold Time	t_{SIH}	20	-	20	-	25	-	ns	

Read Transfer Cycle Timing Waveform (1) *(1,2)



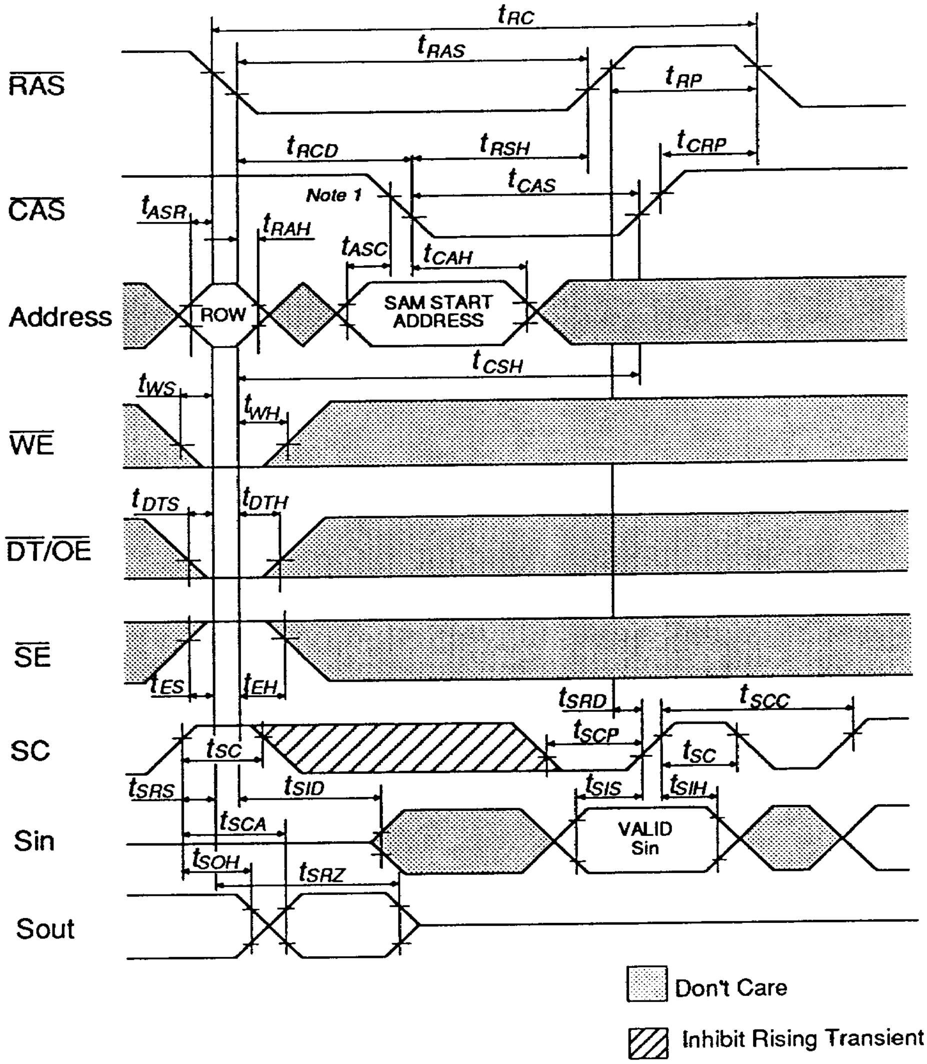
*Notes:
1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
2. SE is low.

Read Transfer Cycle Timing Waveform (2) *(1,2)



*Notes:
1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
2. $\overline{SE}$ is low.

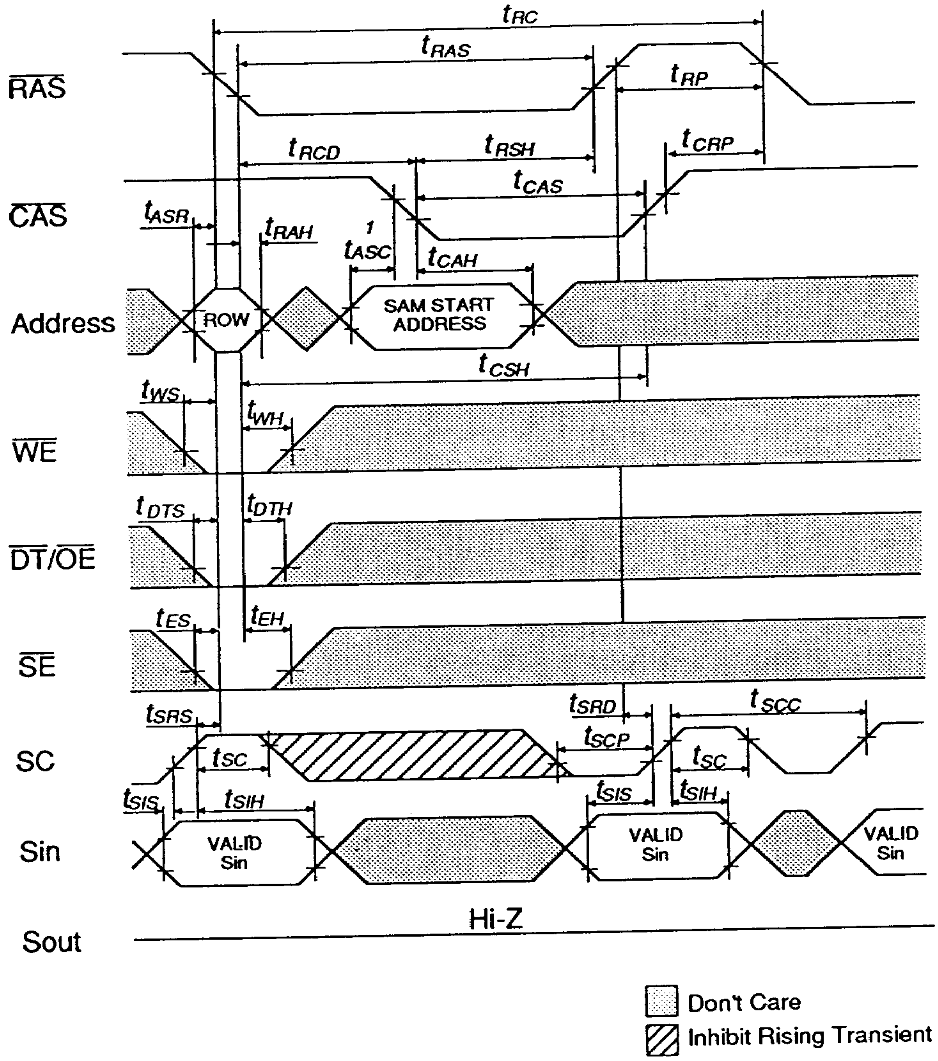
Pseudo Transfer Cycle Timing Waveform



Notes:

1. $\overline{CAS}$ and SAM address don't need to be specified every cycle, if SAM address is not changed.

Write Transfer Cycle Timing Waveform



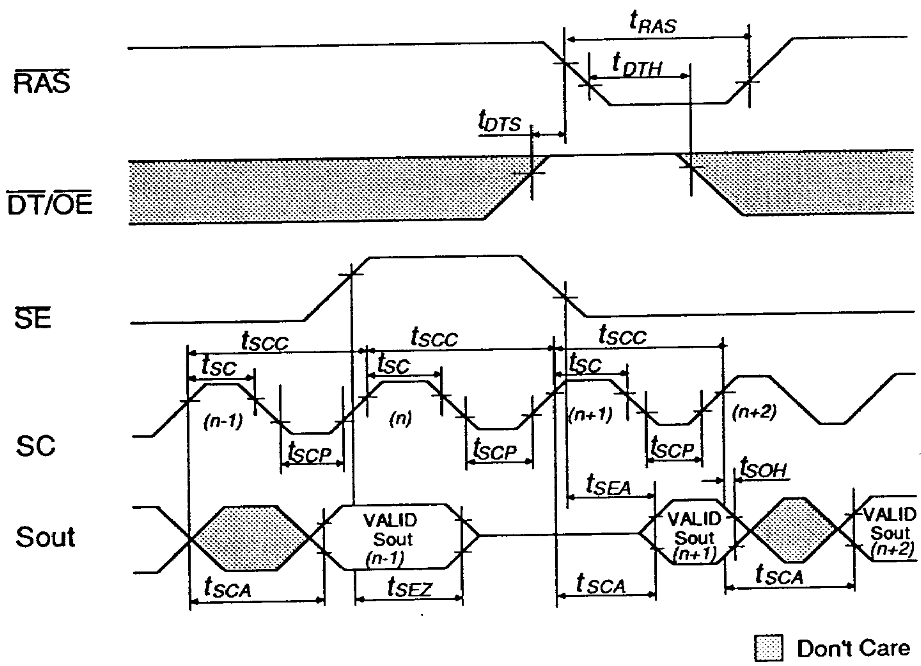
Notes:

1. $\overline{\text{CAS}}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.
2. I/O's are in a "Don't Care" state.

Serial Read Cycle Timing

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
Serial Clock Cycle Time	t_{SCC}	40	-	40	-	60	-	ns	
Access Time from SC	t_{SCA}	-	40	-	40	-	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	-	30	-	30	-	40	ns	4
Serial Data in Hold Time	t_{SOH}	7	-	7	-	7	-	ns	4
SC Pulse Width	t_{SC}	10	-	10	-	10	-	ns	
SC Precharge Time	t_{SCP}	10	-	10	-	10	-	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	-	25	-	25	-	30	ns	7

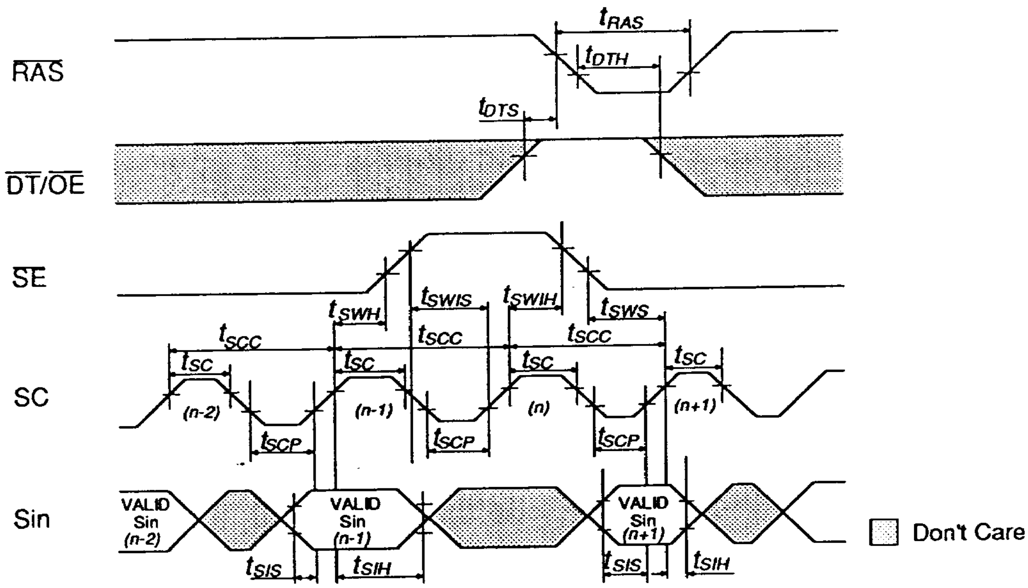
Serial Read Cycle Timing Waveform



Serial Write Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit	Note
Serial Clock Cycle Time	t_{SCC}	40	-	40	-	60	-	ns	
SC Pulse Width	t_{SC}	10	-	10	-	10	-	ns	
SC Precharge Time	t_{SCP}	10	-	10	-	10	-	ns	
Serial Data in Setup Time	t_{SIS}	0	-	0	-	0	-	ns	
Serial Data in Hold Time	t_{SIH}	20	-	20	-	25	-	ns	
Serial Write Enable Setup Time	t_{SWS}	0	-	0	-	0	-	ns	
Serial Write Enable Hold Time	t_{SWH}	35	-	35	-	50	-	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	-	0	-	0	-	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	-	35	-	50	-	ns	

Serial Write Cycle Timing Waveform



Notes:

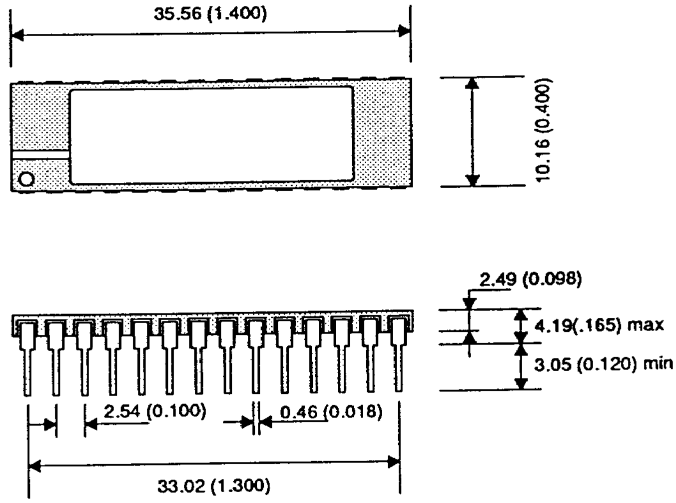
1. When $\overline{SE}$ is high in a serial write cycle, data is not written into SAM, however, the address pointer is incremented.

Notes:

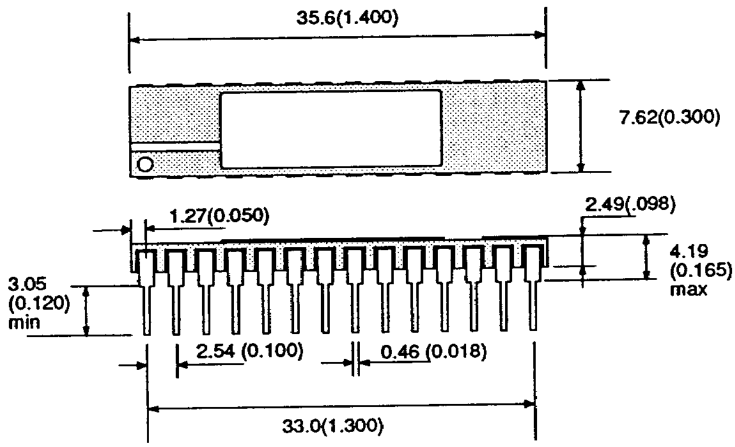
1. AC measurements assume t_T=5ns.
2. Assumes that t_{RCD} is less than or equal to t_{RCD} (max.). If t_{RCD} is greater than the max. recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load current equivalent to two TTL loads and 100pF.
4. Measured with a load current equivalent to two TTL loads and 50pF.
5. When t_{RCD} is greater than or equal to t_{RCD} (max.), access time is specified as t_{CAC}.
6. When t_{RCD} is less than or equal to t_{RCD} (max), access time is specified as t_{AA}.
7. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition (V_{OH} -200mV, V_{OL} +200mV) and is not referenced to output voltage levels.
8. V_{ih} (min.) and V_{il} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{ih} and V_{il}.
9. When t_{WCS} is greater or equal to t_{WCS} (min.), the cycle is an early write cycle. I/O pins remain in an open circuit condition. When $t_{AWD} \geq t_{AWD}$(min.) and $t_{CWD} \geq t_{CWD}$ (min.), the cycle is read-modify-write cycle. Impedance on the I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. An initial pause of 100µs is required after power-up. Then execute at least 8 initialization ($\overline{RAS}$) cycles.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. t_{SCC2} defines the last SAM pulse width before read transfer in read transfer cycle(1).

Package Details Dimensions in mm (inches). Tolerance on all dimensions ±.254 (.010).

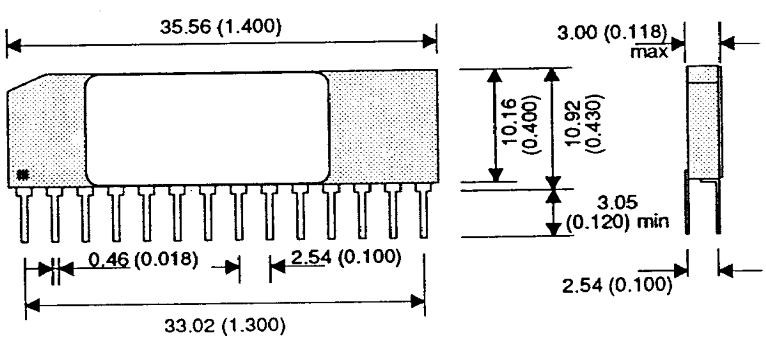
28 Pin Dual-in-Line ('K' Package)



28 Pin Dual-In-Line ('T' Package)



28 Pin Vertical-in-Line (VIL™) ('V' Package)



Military Screening Procedure

Component Screening Flow for high reliability product processed to Mil-883C method 5004 and is detailed below:

MB COMPONENT SCREENING FLOW

SCREEN	TEST METHOD (Per MIL 883C)	LEVEL
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ 150°C)	100%
Temperature Cycle	1010 Condition C (10 Cycles, -65°C to 150°C)	100%
Constant acceleration	2001 Condition E (Y axis only), (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specification @ Ta+25°C	100%
Final Electrical Tests	Per applicable device specification	
Static (dc)	a) @ Ta=25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable(PDA)	Calculated at post-burn-in @ Ta=25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MVM4256VMB-10

- Speed: 100,120,150 ns
- Temp. range/screening:
  - Blank = Commercial Temp.
  - I = Industrial Temp.
  - M = Military Temp.
  - MB = Processed to MIL-883 Class B, Method 5004
- Power: Blank = Standard Power Part
- Package:
  - K = 28 Pin 400 mil DIP
  - T = 28 Pin 300 mil DIP
  - V = 28 Pin 100 mil Vertical-in-Line (VIL)™

Mosaic Semiconductor Inc.

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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