CS-8126

5V, 750mA Low Dropout Linear Regulator with Delayed RESET

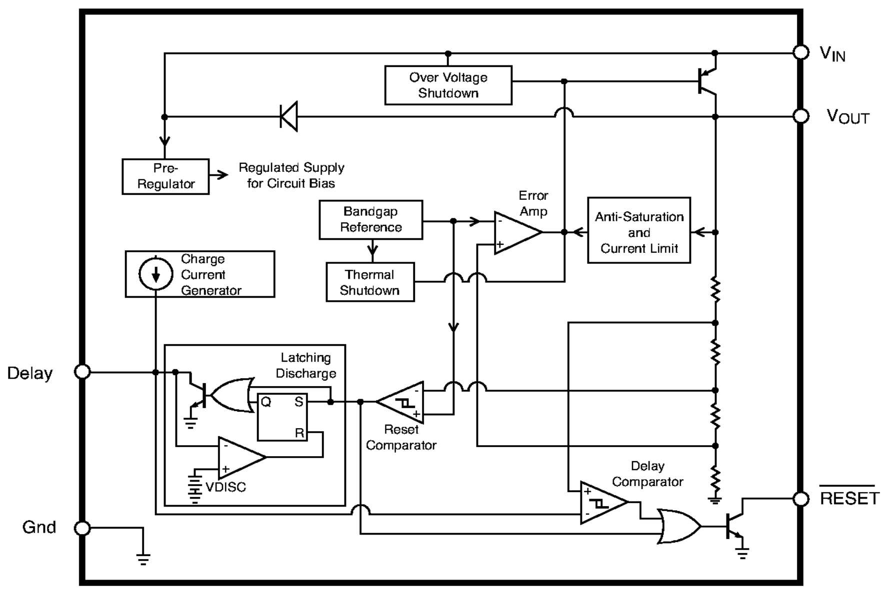
Description

The CS-8126 is a low dropout, high current 5V linear regulator. It is an improved replacement for the CS-8156. Improvements include higher accuracy, tighter saturation control, better supply rejection, and enhanced RESET circuitry. Familiar PNP regulator features such as reverse battery protection, overvoltage shutdown, thermal shutdown, and current limit make the CS-8126 suitable for use in automotive and battery operated equipment. Additional on-chip filtering has been included to enhance rejection of high frequency transients on all external pins.

An active microprocessor RESET function is included on-chip with externally programmable delay time. During power-up, or after detection of any error in the regulated output, the RESET pin will remain in the low state for the duration of the delay. Types of errors include short circuit, low input voltage, overvoltage shutdown, thermal shutdown, or others that cause the output to become unregulated. This function is independent of the input voltage and will function correctly with an output voltage as low as 1V. Hysteresis is included in both the reset and Delay comparators for enhanced noise immunity. A latching discharge circuit is used to discharge the Delay capacitor, even when triggered by a relatively short fault condition. This circuit improves upon the commonly used SCR structure by providing full capacitor discharge (0.2V type).

Note:The CS-8126 is pin compatible with the CS-8156, LM2925, TLE4260, L4947, LM2927, and LM2926.

Block Diagram

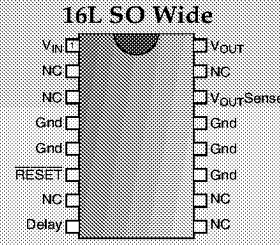


Features

- **Low Dropout Voltage (0.6V at 0.5A)**
- **Output Current in Excess of 750mA**
- **3% Output Accuracy**
- **Active RESET**
- **External RESET Delay for Reset**
- **Protection Circuitry**
  - **Reverse Battery Protection**
  - **60V Load Dump Protection**
  - **-50V Reverse Transient Protection**
  - **Short Circuit Protection**
  - **Internal Thermal Overload Protection**

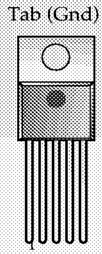
Package Options

16L SO Wide



TO-220 5 Lead

Tab (Gnd)



CS-8126-1
1 V_{IN}
2 V_{OUT}
3 Gnd
4 Delay
5 RESET

CS-8126-2
1 V_{IN}
2 RESET
3 Gnd
4 Delay
5 V_{OUT}

Consult Factory for D^2PAK package

Cherry Semiconductor

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A CHERRY Company

Absolute Maximum Ratings

Power Dissipation....................Internally Limited
Transient Input Voltage....................–50V, 60V
Output Current....................Internally Limited
ESD Susceptibility (Human Body Model)....................4kV
Operating Temperature....................–45°C to 125°C
Junction Temperature....................–45°C to 150°C
Storage Temperature....................–55 to 150°C
Lead Temperature Soldering Wave Solder(through hole styles only)....................10 sec. max, 260°C peak
Reflow (SMD styles only)....................60 sec. max above 183°C, 230°C peak

Electrical Characteristics: T_A=-40°C to +125°C, T_J=-40°C to +150°C, V_{IN}=6 to 26V, I_O=5 to 500mA, R_{RESET}=4.7kΩ to V_{CC} unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Stage (V_{OUT})					
Output Voltage		4.85	5.00	5.15	V
Dropout Voltage	I_{OUT} = 500mA		0.35	0.60	V
Supply Current	$I_{OUT} \leq$ 10mA $I_{OUT} \leq$ 100mA $I_{OUT} \leq$ 500mA		2 6 55	7 12 100	mA
Line Regulation	V_{IN} = 6 to 26V, I_{OUT} = 50mA		5	50	mV
Load Regulation	I_{OUT} = 50 to 500mA, V_{IN} = 14V		10	50	mV
Ripple Rejection	f = 120Hz, V_{IN} = 7 to 17V, I_{OUT} = 250mA	54	75		dB
Current Limit		0.75	1.20		A
Overvoltage Shutdown		32		40	V
Maximum Line Transient	$V_{OUT} \leq$ 5.5V	60	95		V
Reverse Polarity Input Voltage DC	$V_{OUT} \geq$ -0.6V, 10Ω Load	-15	-30		V
Reverse Polarity Input Voltage Transient	1% Duty Cycle, T < 100ms, 10Ω Load	-50	-80		V
■ $\overline{\text{RESET}}$ and Delay Functions					
Delay Charge Current	V_{Delay} = 2V	5	10	15	μA
$\overline{\text{RESET}}$ Threshold	V_{OUT} Increasing, V_{RT} ON V_{OUT} Decreasing, V_{RT} OFF	4.65 4.50	4.90 4.70	V_{OUT} - 0.01 V_{OUT} - 0.15	V V
$\overline{\text{RESET}}$ Hysteresis	V_{RH}=V_{RT} ON-V_{RT} OFF	150	200	250	mV
Delay Threshold	Charge, V_{DC} HI Discharge, V_{DC} LO	3.25 2.85	3.50 3.10	3.75 3.35	V V
Delay Hysteresis		200	400	800	mV
$\overline{\text{RESET}}$ Output Voltage Low	1V < V_{OUT} < V_{RTL}, 3kΩ to V_{OUT}		0.1	0.4	V
$\overline{\text{RESET}}$ Output Leakage Current	V_{OUT} > V_{RTH}		0	10	μA
Delay Capacitor Discharge Voltage	Discharge Latched "ON", V_{OUT} > V_{RT}		0.2	0.5	V
Delay Time	C_{Delay} = 0.1μF* (Note 1)	16	32	48	ms

$$\text{Delay Time} = \frac{C_{Delay} \times V_{Delay}\ \text{Threshold Charge}}{I_{Charge}} = C_{Delay} \text{x} 3.2 \text{x} 10^5 \text{ (typ)}$$

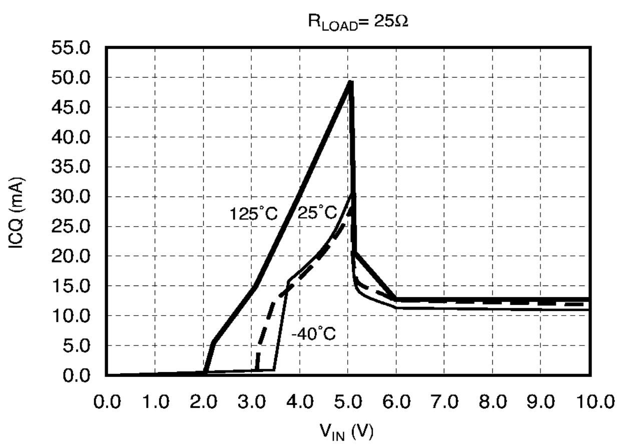
Note 1: assumes ideal capacitor

Package Pin Description

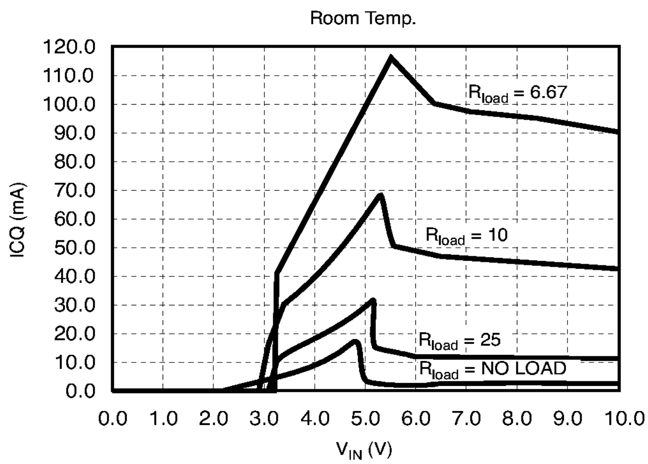
PACKAGE PIN #			PIN SYMBOL	FUNCTION
TO-220 8126-1	TO-220 8126-2	16L SO		
1	1	1	V_{IN}	Unregulated supply voltage to IC.
2	5	16	V_{OUT}	Regulated 5V output.
3	3	4,5,11,12,13	Gnd	Ground connection.
4	4	8	Delay	Timing capacitor for $\overline{\text{RESET}}$ function.
5	2	6	$\overline{\text{RESET}}$	CMOS/TTL compatible output pin. $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops below 6% of it's regulated value.
		14	$V_{OUT_{SENSE}}$	Remote sensing of output voltage

Typical Performance Characteristics

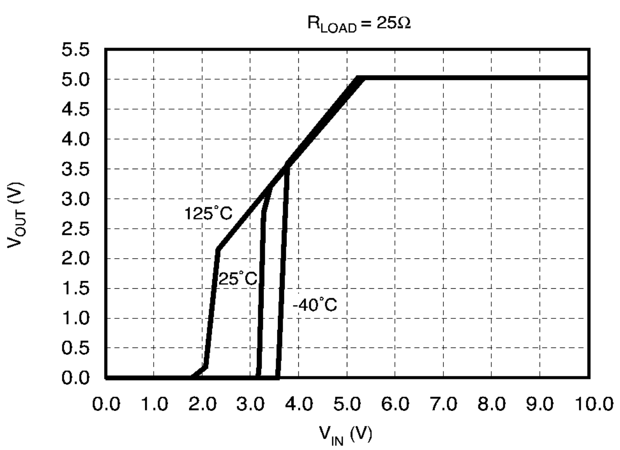
I_{CQ} vs. V_{IN} over Temperature



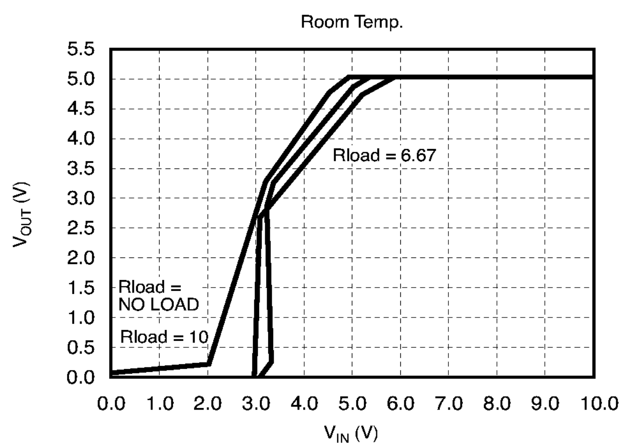
I_{CQ} vs. V_{IN} over R_{LOAD}



V_{OUT} vs V_{IN} over Temperature

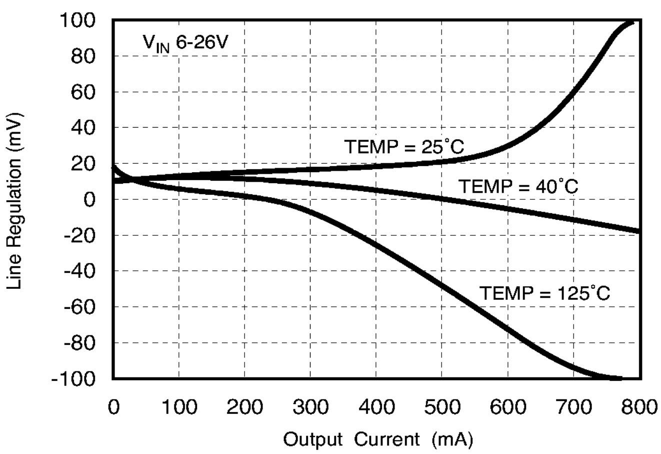


V_{OUT} vs. V_{IN} over R_{LOAD}

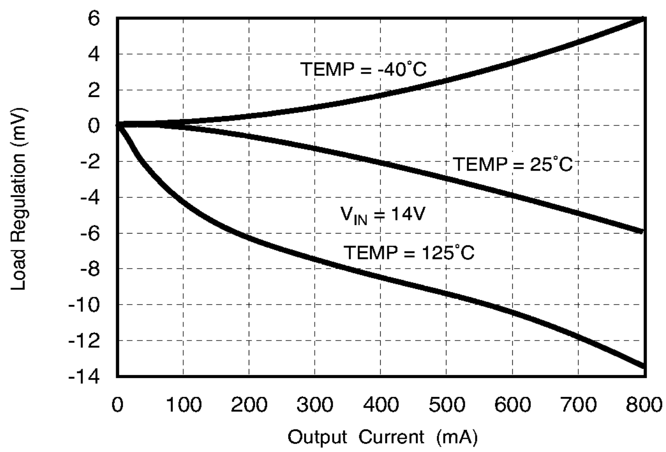


Typical Performance Characteristics: continued

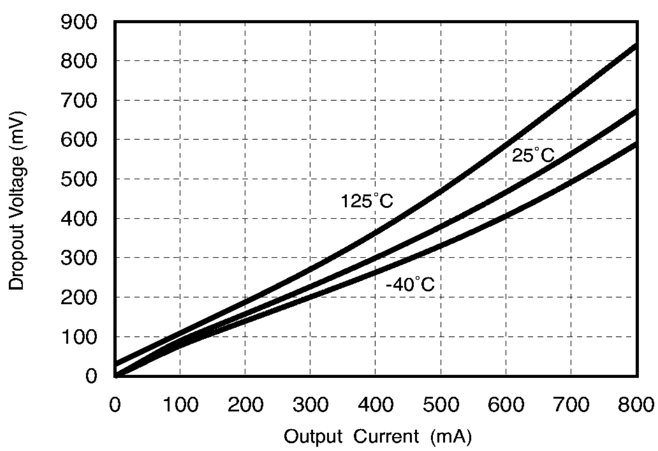
Line Regulation vs. Output Current over Temperature



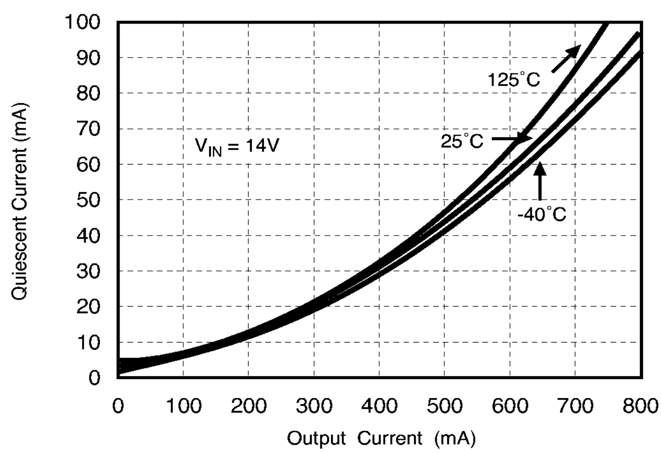
Load Regulation vs. Output Current over Temperature



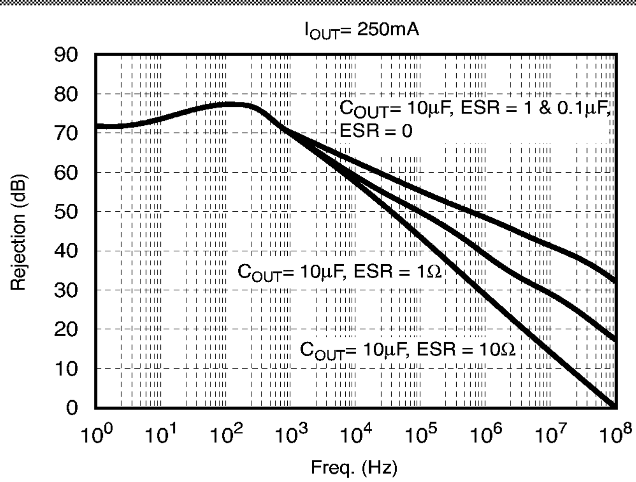
Dropout Voltage vs. Output Current over Temperature



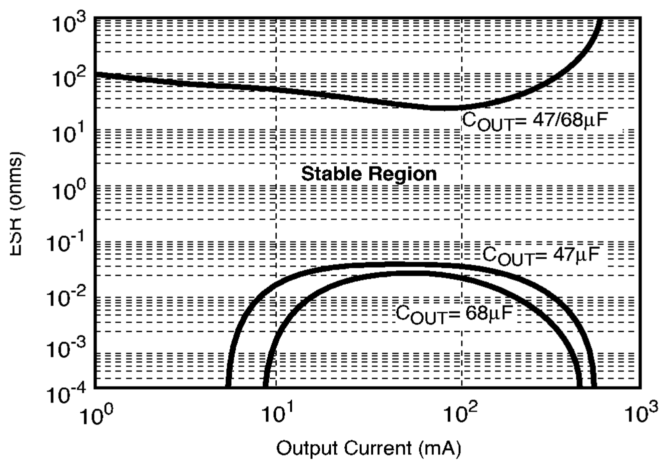
Quiescent Current vs. Output Current over Temperature



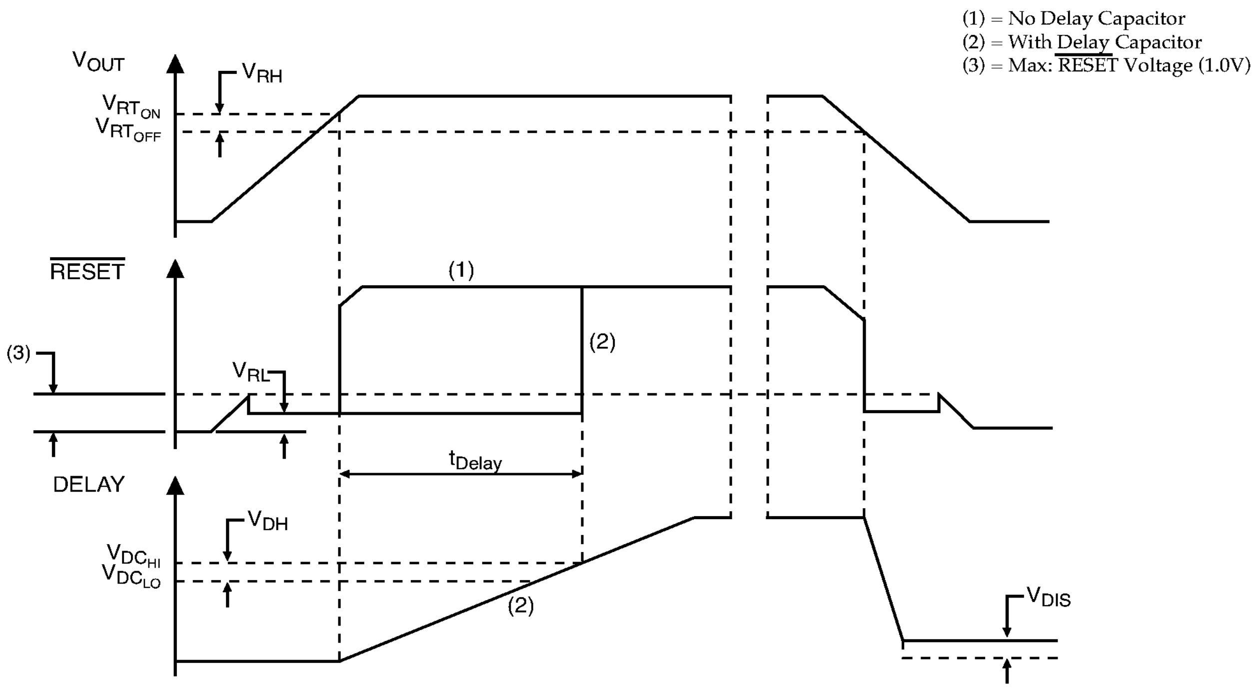
Ripple Rejection



Output Capacitor ESR



$\overline{\text{RESET}}$ Circuit Waveform



Circuit Description

The CS-8126 $\overline{\text{RESET}}$ function, has hysteresis on both the Reset and Delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1V.

The $\overline{\text{RESET}}$ circuit output is an open collector type with ON and OFF parameters as specified. The $\overline{\text{RESET}}$ output NPN transistor is controlled by the two circuits described (see Block Diagram).

Low Voltage Inhibit Circuit

This circuit monitors output voltage, and when output voltage is below the specified minimum, causes the $\overline{\text{RESET}}$ output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the $\overline{\text{RESET}}$ output transistor to go into the OFF state if allowed by the RESET Delay circuit.

$\overline{\text{RESET}}$ Delay Circuit

This circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output pin. The Delay pin provides source current to the external delay capacitor only when the "Low Voltage Inhibit" circuit indicates that output voltage is above $V_{RT_{ON}}$. Otherwise, the Delay pin sinks current to ground (used to discharge the delay capacitor).

The discharge current is latched ON when the output voltage is below $V_{RT_{OFF}}$. The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures a controlled $\overline{\text{RESET}}$ pulse is generated following detection of an error condition. The circuit allows the $\overline{\text{RESET}}$ output transistor to go to the OFF (open) state only when the voltage on the Delay pin is higher than V_{DCH1}.

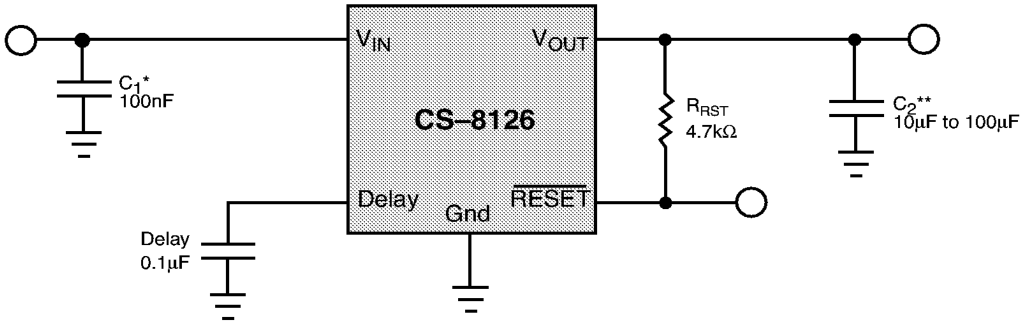
The Delay time for the $\overline{\text{RESET}}$ function is calculated from the formula:

$$\text{Delay time} = \frac{C_{Delay} \times V_{Delay}\ \text{Threshold}}{I_{Charge}}$$

$$\text{Delay time} = C_{Delay} \times 3.2 \times 10^{5}$$

If C_{Delay}=0.1μF, Delay time (ms)=32ms ± 50%: i.e. 16ms to 48ms. The tolerance of the capacitor must be taken into account to calculate the total variation in the delay time.

Application Diagram



C_1* is required if the regulator is far from the power source filter.

C_2** is required for stability

Application Notes

Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The value for the output capacitor C_2 shown in the test and applications circuit should work for most applications, however it is not necessarily the best solution.

To determine an acceptable value for C_2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs on the oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor.

(Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of +/- 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 1) is

$$P_{D(max)}=\{V_{IN(max)}-V_{OUT(min)}\}I_{OUT(max)}+V_{IN(max)}I_Q \qquad (1)$$

where

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current, for the application

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \qquad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

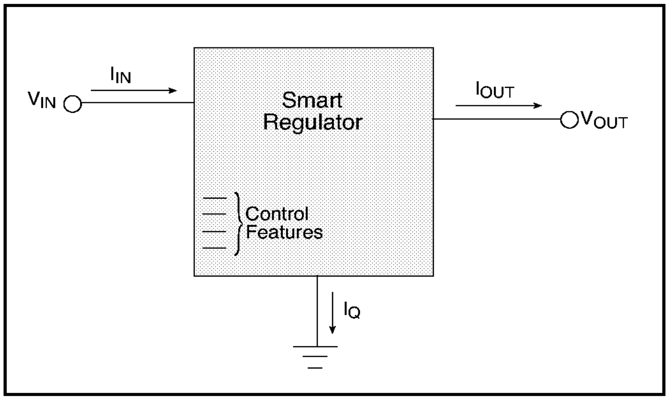


Figure 1: Single output regulator with key performance parameters labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \qquad (3)$$

where

$R_{\Theta JC}$ = the junction–to–case thermal resistance,
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and
$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

Package Specification

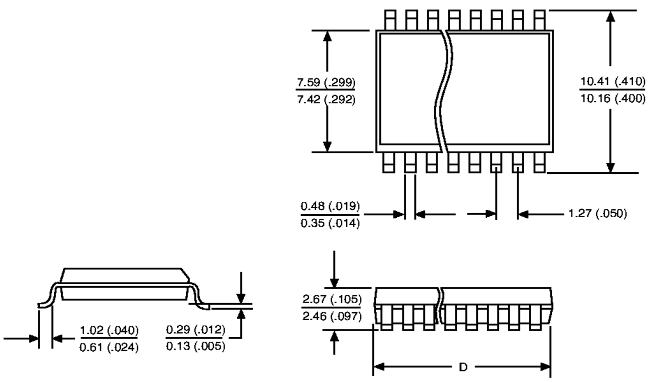
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16 Lead SO	10.00	9.80	.394	.385

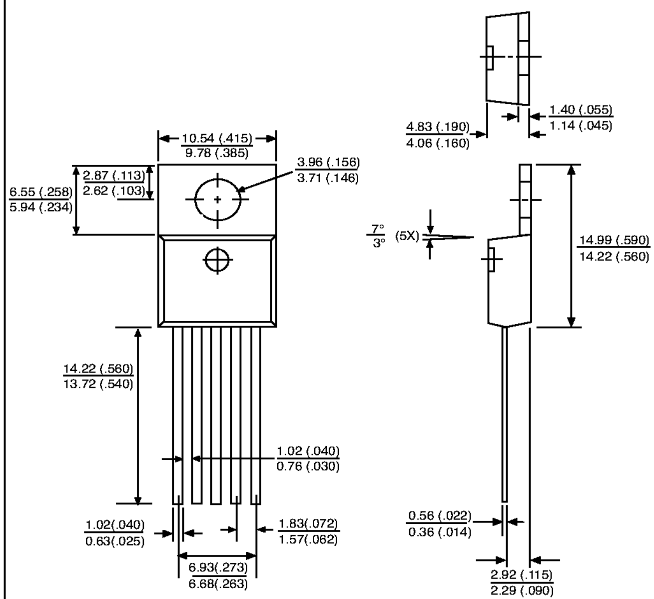
PACKAGE THERMAL DATA

Thermal Data		TO-220 5 Lead	SO Wide 16 Lead	
$R_{\Theta JC}$	typ	2.1	28	°C/W
$R_{\Theta JA}$	typ	50	105	°C/W

16 Lead SO



5 Lead TO-220 Straight



Ordering Information

Part Number	Description
CS-8126-1T5	TO-220 Straight
CS-8126-1TV5	TO-220 Vertical
CS-8126-1TH5	TO-220 Horizontal
CS-8126-2T5	TO-220 Straight
CS-8126-2TV5	TO-220 Vertical
CS-8126-2TH5	TO-220 Horizontal
CS-8126DW16	SOIC Wide

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