Monolithic MMI Memories

16-Bit CMOS Multiplier Slice 67C7555 67C7556

ADVANCE INFORMATION

Features/Benefits

- Twos-complement, unsigned, or mixed operands
- Full 32-bit product immediately available on each cycle
- High-speed 16x16 parallel multiplier
- Latched or registered inputs/outputs
- Three-state output controls, independent for each half of the product
- Single +5 V supply (via multiple pins)
- Zero standby power CMOS technology
- Available in 84-terminal Leadless-Chip Carrier and 88-Pin-Grid-Array packages

Description

The 'C7555 and 'C7556 are high-speed 16x16 combinatorial multipliers which can multiply two 16-bit unsigned or signed twos-complement numbers on every cycle. Each operand X and Y has an associated mode-control line, XM and YM respectively. When a mode-control line is at a LOW logic level, the operand is treated as an unsigned 16-bit number; when the mode-control line is at a HIGH logic level, the operand is treated as a 16-bit signed twos-complement number. Additional inputs RS and RU allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding.

Ordering Information

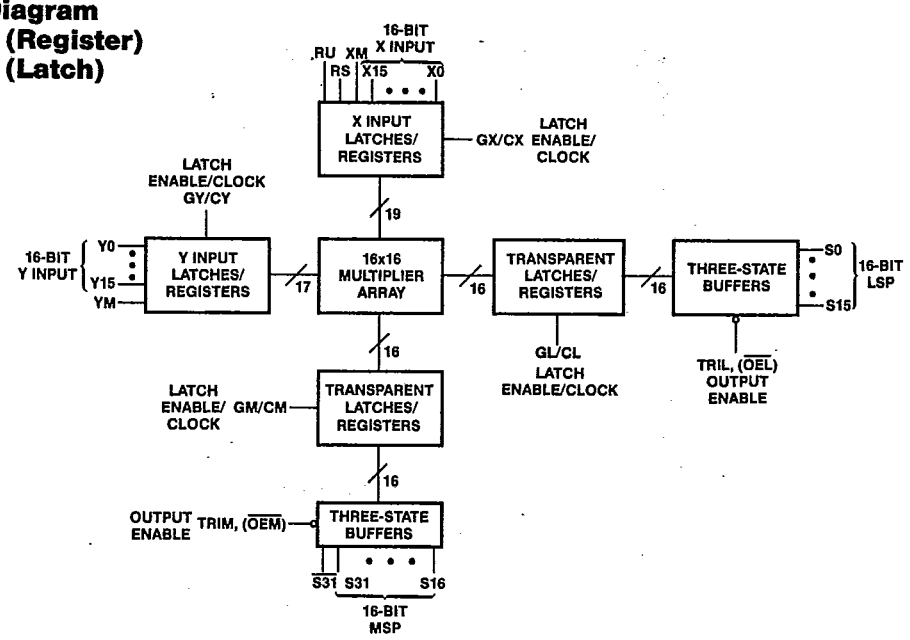
PART NUMBER	PACKAGE	TEMPERATURE
67C7555	P88, L84	Com
67C7556	P88, L84	Com

The entire 32-bit double-length product is available at the outputs at one time.

The most-significant product bit, S31, is available in both true and complemented form to simplify longer-wordlength multiplications. The product outputs are three-state, controlled by assertive-low enables. The MSP outputs are controlled by the TRIM ($\overline{OEM}$) control input, while the LSP outputs are controlled by the TRIL ($\overline{OEL}$) control input. This allows one or more multipliers to be connected to a parallel bus or to be used in a pipelined system.

All inputs and outputs have transparent latches in the 'C7556. The latches become transparent when the input to the corresponding gate control line GX, GY, GM, GL is HIGH. If latches are not required, these control inputs may be tied HIGH, leaving the multiplier fully transparent for combinatorial cascading. The device uses a single +5 V power supply, and is available both in an 84-terminal leadless chip carrier (LCC) package and in an 88-pin-grid-array package.

Block Diagram 'C7555 (Register) 'C7556 (Latch)



17

SUMMARY OF SIGNALS/PINS	
X_{15-0}	Multiplicand 16-bit data inputs
Y_{15-0}	Multiplier 16-bit data inputs
XM, YM	Mode-control inputs for each data word; LOW for unsigned data and HIGH for twos-complement data
S_{31-0}	Product 32-bit output
$\overline{S}_{31}$	Inverted MS product bit (for expansion)
RS, RU	Rounding inputs for signed and unsigned data, respectively
GX/CX	Gate contro/clock for X_i, RS, RU
GY/CY	Gate control/clock for Y_i
GL/CL	Gate control/clock for least-significant half of product
GM/CM	Gate control/clock for most-significant half of product
TRIL / $\overline{OEL}$	Three-state control for least-significant half of product
TRIM / $\overline{OEM}$	Three-state control for most-significant half of product

Rounding Inputs

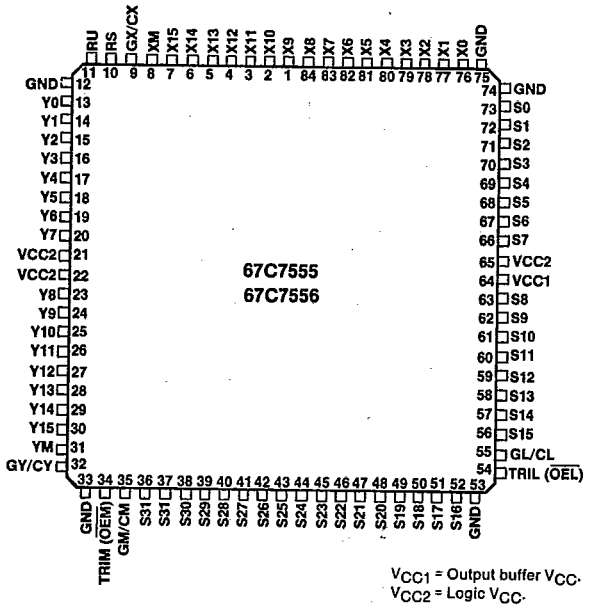
INPUTS		ADDS		USUALLY USED WITH	
RU	RS	2^{15}	2^{14}	XM	YM
L	L	No	No	X	X
L	H	No	Yes	H†	H†
H	L	Yes	No	L	L
H	H	Yes	Yes	*	*

† In mixed mode, one of these could be low but not both.
* Usually a nonsense operaion.

Mode-Control Inputs

OPERATING MODE	INPUT DATA		MODE-CONTROL INPUTS	
	X_{15-0}	Y_{15-0}	XM	YM
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos-Comp.	L	H
	Twos-Comp.	Unsigned	H	L
Signed	Twos-Comp.	Twos-Comp.	H	H

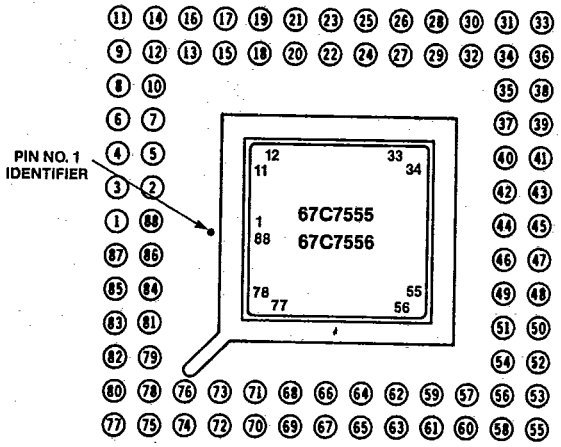
84-Terminal Leadless Chip Carrier Pinout



V_{CC1} = Output buffer V_{CC}.
V_{CC2} = Logic V_{CC}.

All V_{CC} and GND pins must be connected to the respective V_{CC} and GND connections on the board and should not be used for daisychaining through the IC.

88 Pin-Grid-Array Pin Location Bottom View



Pin-Guide for Pin Grid Array

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1	X9	23	N/C*	45	S25	67	V_{CC2}†
2	X10	24	Y8	46	S24	68	N/C*
3	X11	25	Y9	47	S23	69	S7
4	X12	26	Y10	48	S22	70	S6
5	X13	27	Y11	49	S21	71	S5
6	X14	28	Y12	50	S20	72	S4
7	X15	29	Y13	51	S19	73	S3
8	XM	30	Y14	52	S18	74	S2
9	GX/CX	31	Y15	53	S17	75	S1
10	RS	32	YM	54	S16	76	S0
11	RU	33	GY/CY	55	GND	77	GND
12	GND	34	N/C*	56	TRIL ($\overline{OEL}$)	78	N/C*
13	Y0	35	GND	57	GL/CL	79	GND
14	Y1	36	TRIM ($\overline{OEM}$)	58	S15	80	X0
15	Y2	37	GM/CM	59	S14	81	X1
16	Y3	38	$\overline{S31}$	60	S13	82	X2
17	Y4	39	S31	61	S12	83	X3
18	Y5	40	S30	62	S11	84	X4
19	Y6	41	S29	63	S10	85	X5
20	Y7	42	S28	64	S9	86	X6
21	V_{CC2}†	43	S27	65	S8	87	X7
22	V_{CC2}†	44	S26	66	V_{CC1}††	88	X8

* Not connected. † V_{CC2} = Logic V_{CC}. †† V_{CC1} = Output buffer V_{CC}.

17