



## LOCAL BUS IDE SOLUTION

### GENERAL DESCRIPTION

The W83769 is a high-performance, low-cost, highly integrated logic design for IDE hard disk applications in PCI (Peripheral Component Interconnect) local bus systems. It provides a bridge between a standard IDE drive and the PCI local bus. The W83769 is fully compatible with the ANSI ATA 3.0 specifications for IDE hard disk operation and the PCI SIG revision 2.0 specifications for the PCI local bus protocol. Packaged in a 100-pin PQFP, the W83769 directly supports the 32-bit PCI bus without requiring any external TTLs.

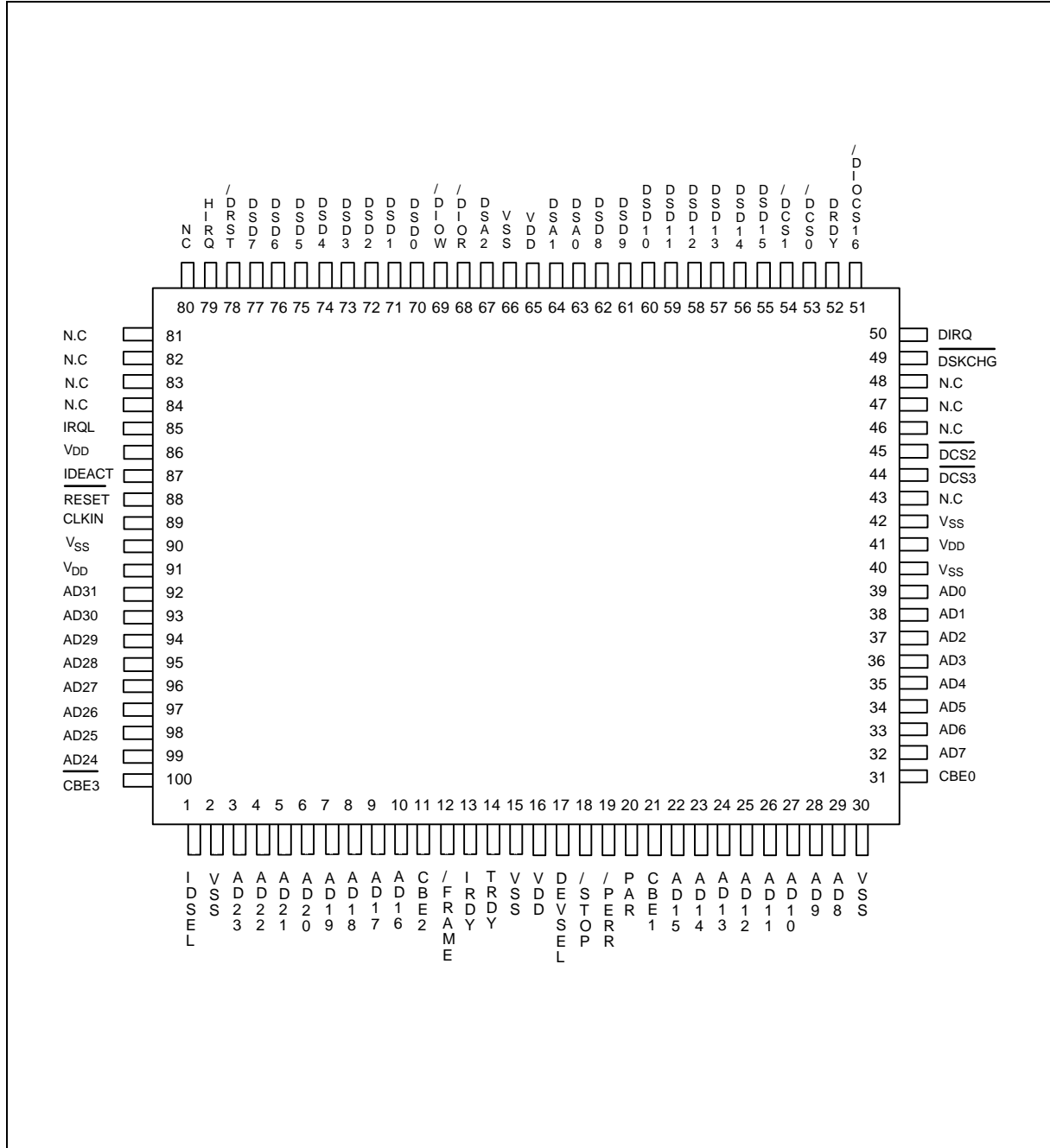
The W83769 operates at up to 50 MHz and provides a full 32-bit data path to the PCI bus. Double-word read and write operations are provided via internal control and conversion logic. Write posting and read-ahead allows CPU memory cycles to run concurrently with IDE cycles and improves the hard disk buffer-to-host transfer rate.

The IDE drive interface timing of the W83769 is completely software programmable, including command active/recovery timing and address setup-hold timing for each drive. The device supports Fast ATA/Enhanced IDE mode 3 timing and IORDY monitoring for better performance. The W83769 directly supports four IDE drives with 170/1F0 dual IDE connectors. The IObase addresses of the primary/secondary IDE connector are exchangeable by power-on strap option.

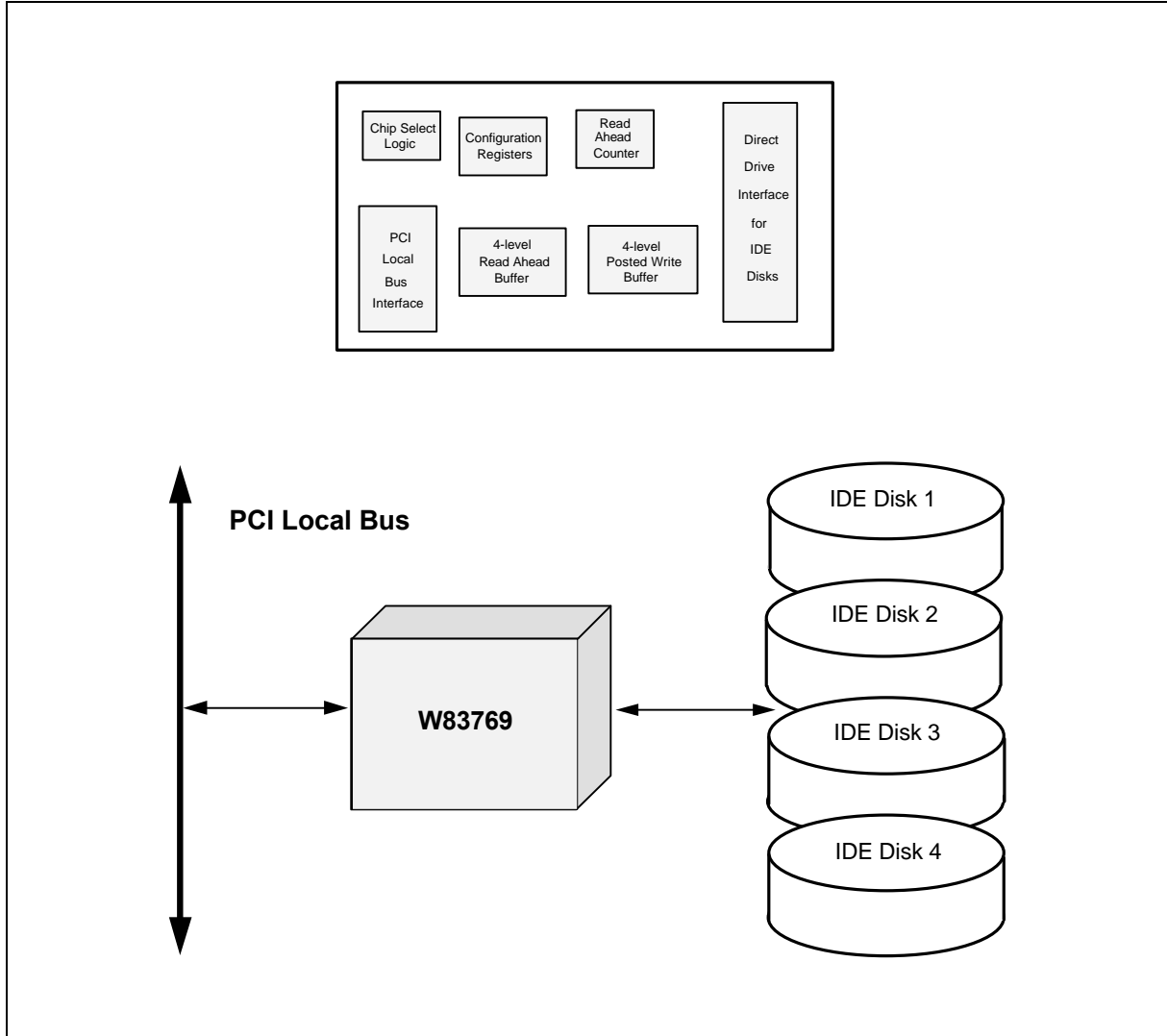
### FEATURES

- 100% PCI Local Bus 2.0 compatible
- IDE primary/secondary address selection
- 32-bit local bus interface
- Automatic standby mode for power saving
- On-chip decode and select logic
- Supports local bus operation at up to 50 MHz
- Four-level pipelined read-ahead and four-level posted write buffers for concurrent system operations
- Programmable parameters for command active and recovery timing
- Direct supports four IDE disk drives
- Programmable address setup timing and data active/recovery timing for each drive
- Slew-rate-controlled direct driving capability to interface with IDE disk
- Drivers for DOS, Windows, Novell, and OS/2
- Supports ATA 3.0 IDE standard
- Packaged in 100-pin PQFP

**PIN CONFIGURATION**



**BLOCK DIAGRAM**



**1. FUNCTIONAL DESCRIPTION**

**1.1 32-bit Local Bus Interface**

The W83769 is a Local Bus IDE Interface device that serves as an interface between standard IDE hard disks and a high-performance local bus. It is fully compatible with the PCI Local Bus 2.0 standard.

The W83769 provides all the required pins and logic needed for direct connection to the CPU bus, including the 32-bit data bus. The chip can be mounted on a local bus adapter card using the PCI Local Bus standard or mounted directly onto the motherboard.



## 1.2 Chip Decode and Select Logic

The W83769 contains all required chip select and decode logic needed to function without any additional buffering or interface logic to the local bus. This includes all address decoding, data buffering, and control logic.

## 1.3 Direct Drive IDE Disk Interface

The W83769 provides a slew-rate-controlled direct drive interface to four IDE drives. The interface conforms to relevant industry standards, including the ANSI ATA Rev. 3.0 standard. Up to four W83769 devices, and therefore 16 IDE drives, can be interfaced to the local bus. Additional drives can reside on expansion buses. Drive selection and switching are handled by software.

Each device permits either of the two interfaced IDE ports to be assigned and addressed as the primary or secondary port. Each port can support two drives, which can be assigned as the master drive (drive 0) or slave drive (drive 1). Individual IDE disk drive performance can be optimized through the W83769's programmable registers. Each drive's command active and recovery timing, address setup and hold, and data read/write active and recovery timing may be controlled independently.

## 1.4 Four-level Read Ahead Buffer and Counter

The W83769's read-ahead feature significantly enhances disk drive read performance. In pipelined read-ahead mode, when the host CPU is occupied with other or previous data transfers, the IDE controller can automatically request and concurrently transfer additional data from the disk drive. These data are stored in the device's four-level FIFO read-ahead buffer. The controller will continue to read data from the drive as long as the buffer is not full, the read-ahead counter is not zero, and the host CPU continues to request data. Data transfer sizes are determined by the host CPU request and can be word or double-word.

A programmable read-ahead counter is used in conjunction with the read-ahead buffer to regulate the flow of data from the disk drive. The counter is normally initialized with the number of bytes per sector. This is determined from the disk formatting and can be different for each drive. As data is transferred, the counter is decremented to zero. It is then reinitialized for the next sector transfer.

## 1.5 Four-level Posted Write Buffer

The W83769 also contains a four-level FIFO posted-write buffer which can be used by the CPU to pipeline data to the disk drive, thereby significantly increasing throughput. The CPU data are written to the posted-write buffer. Concurrently, data are written to the disk drive by the IDE controller at the appropriate data transfer rate. While the buffered data are waiting to be written, the CPU is left free to fetch additional data for the next transfer.

## 1.6 Interrupt Operation

To ensure proper interrupt operation between the IDE drives and the host CPU, the drives' interrupts can be passed through the W83769. The interrupts are input on the DIRQ pin and asynchronously output to the host chipset on the HIRQ pin as IRQ14, the standard IDE PC/AT interrupt. If four drives, i.e., two drive cables, are present, the interrupts from both pairs of drives can be connected to HIRQ. The interrupt status of individual drives can be read from the general purpose configuration register, RX50, bit 2. A 10K ohm pullup should be connected to the HIRQ input to prevent floating.

Alternatively, with four drives present, the interrupt from each pair of drives can be connected directly to the host CPU chipset IRQ14 and IRQ15.



### 1.7 3F7h Register Operation

The disk drive status register 3F7h is a read-only register that provides hard drive status in bits 6-0 to the host CPU. Floppy drive status is provided as bit 7; this status indication originates from pin 34 of the floppy drive cable. All 8 bits can be combined, buffered, and passed to the host CPU chipset as a normal ISA bus cycle. The W83769 will detect the 3F7h address on the host address bus as an IDE cycle but will not generate any clocked transfer cycle.

### 1.8 Power-Save Mode

The W83769 contains a power-save feature for notebook or green PC applications. If no IDE cycles are in progress, the power-save circuitry forces all but the CPU tracking and address decoding logic into a static state to reduce power consumption. This also reduces EMI radiation because the IDE cable is inactive while the device is in power-save mode.

### 1.9 Reset Initialization

The first step in setting up the W83769 for operation is to reset the device using the active high RESET pin. A reset immediately terminates any operation in progress and returns the W83769 to a known state from which it can be initialized. Immediately following a reset, the controller determines its operational mode via pin configuration.

If the IDEACT pin is sampled high, IDE operation will be enabled, and disk transfer cycles can be executed. If the IDEACT pin is sampled low, IDE operation is disabled, and the controller will respond only to configuration cycles via the general purpose I/O ports. This permits BIOS software to test the system for installed disks and enable/disable the W83769 and specific features and operations.

### 1.10 Hardware Configurations

Several hardware configuration options can be defined using the DSA1 and  $\overline{\text{DCS0}} - 1$  pins during the power-on reset:

DSA1	Digital Input Register
0	Disable
1	Enable
$\overline{\text{DCS0}} - 1$	Device ID selection (for multiple chip only)
00	60h
01	61h
10	62h
11	63h

To select the value of 0 for each bit in the above configuration, the corresponding pin needs to be pulled down during the power-on reset. Pulling the pin up will set the value to 1.

### 1.11 I/O Registers



A number of I/O registers are implemented in W83769 that allow the chip to be programmed by system software. These I/O registers can be divided into two categories: PCI configuration registers and general purpose registers. This section defines the possible settings of these registers. Underlined register settings designate the default values of the registers at power-on.

### 1.11.1 PCI Configuration Registers

In the PCI mode, the PCI configuration read/write will set up the PCI configuration registers.

#### **Host Address 0–1(VID)**

Vendor ID (RO)

10ADh for Winbond

#### **Host Address 2–3(DID)**

Device ID (RO)

0001h for W83769

#### **Host Address 4–5 (PCMD)**

PCI Command Register (R/W)

bit 15–9: reserved

bit 8–7: always 0

bit 6: parity checking

0      disable

1        enable

bit 5–1: always 0

bit 0: always 1

#### **Host Address 6–7 (PSTTS)**

Device Status Register (R/W)

bit 15: parity error detected

bit 14–11: always 0

bit 10–9: DEVSEL timing (RO)

00      fast

01     medium

10      slow

11      reserved

bit 8–0: reserved

#### **Host Address 8 (REVID)**

Revision ID (RO)

00h for Rev BB

02h for Rev A3C

**Host Address 9 (PGIF)**

Programming Interface (RO)

00h

**Host Address Ah (SUBCLS)**

Sub-Class (RO)

01h for IDE Controller

**Host Address Bh (BASCLS)**

Base Class (RO)

01h for Mass Storage  
Controller

**Host Address 3Ch (INTLINE)**

Interrupt Line (RO)

0Eh (value of 14)

**Host Address 3Dh (INTPIN)**

Interrupt Pin (RO)

01h (value of 1)

## 1.11.2 General Purpose Registers

Two IO ports are used to access the entire set of general purpose I/O registers: the index port at address 0B4h and the data port at 0B8h. To access a register, first write the index into the index port and then read or write the data through the data port. The index and data port can be relocated to address 034h and 038h by pulling up the DSA2 pin. Every internal register is assigned an 8-bit index.

The general purpose registers allow driver software to program the IDE controller to work with different hard disks with various characteristics. The majority of the registers defined here are related to the hard disk's timing parameters.

### **RX50 (CFR)**

Device Configuration Register (RO)

bit 7:	reserved
bit 6:	Digital Input register
<u>0</u>	<u>disable</u>
1	enable
bit 5:	reserved
bit 4,3:	Device ID selection
00	60h
01	61h
10	62h
<u>11</u>	<u>63h</u>
bit 2	IDE drive interrupt status (read CFR will clear this bit)
<u>0</u>	<u>no interrupt pending</u>
1	interrupt pending
bit 1:	reserved
bit 0:	enable/disable 2nd IDE port (R/W)
<u>0</u>	<u>disable</u>
1	enable

Note that RX50 is read-only, with the exception of bit 0. This bit is for enabling or disabling the second IDE port and therefore is a read/write bit. This bit is writable through RX50 but is readable only through RX57.

### **RX51 (CNTRL)**

Control Register (R/W)

bit 7:	reserved
bit 6:	Read ahead enable
0	enable
<u>1</u>	<u>disable</u>



bit 5:	Host write fifo/reg longer data hold time
<u>0</u>	<u>enable</u>
1	disable
bit 4:	PCI parity check
<u>0</u>	<u>disable</u>
1	enable
bit 3:	timing selection for drives of secondary port
<u>0</u>	<u>disks 0,2 use timing set 0 and disks 1,3 use timing set 1</u>
1	disks 0,1 use timing set 0 and disks 2,3 use timing set 1
bit 2:	DEVESL timing
<u>0</u>	<u>medium</u>
1	fast
bit 1:	Host write timing
<u>0</u>	<u>slow timing</u>
1	fast timing
bit 0:	Host read timing
<u>0</u>	<u>slow timing</u>
1	fast timing

**RX52 (CMDTLM)**

## IDE Command Timing Register (RW)

bit 7-4:	IOR\W active count
<u>0000</u>	<u>16 clocks</u>
0001	2 clocks
0010	2 clocks
0011	3 clocks
0100	4 clocks
0101	5 clocks
0110	6 clocks
0111	7 clocks
1000	8 clocks
1001	9 clocks
1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	13 clocks

1110	14 clocks
1111	15 clocks
bit 3–0:	Command Recovery count
<u>0000</u>	<u>16 clocks</u>
0001	1 clocks
0010	2 clocks
0011	3 clocks
0100	4 clocks
0101	5 clocks
0110	6 clocks
0111	7 clocks
1000	8 clocks
1001	9 clocks
1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	13 clocks
1110	14 clocks
1111	15 clocks

**RX53 (ARTIM0)**

Drive 0 Address Setup/Data Recovery Timing Register (R/W)

bit 7–6:	address set up count
<u>00</u>	<u>3 clocks</u>
01	1 clocks
10	2 clocks
11	4 clocks
bit 5–4:	reserved
bit 3–0:	Data (1F0h) recovery count
<u>0000</u>	<u>16 clocks (read/write)</u>
0001	4 clocks (read) 5 clock (write)
0010	4 clocks (read) 5 clock (write)
0011	5 clocks (read/write)
0100	6 clocks (read/write)
0101	7 clocks (read/write)
0110	8 clocks (read/write)

0111	9 clocks (read/write)
1000	10 clocks (read/write)
1001	11 clocks (read/write)
1010	12 clocks (read/write)
1011	13 clocks (read/write)
1100	14 clocks (read/write)
1101	15 clocks (read/write)
1110	16 clocks (read/write)
1111	17 clocks (read/write)

**RX54 (DRWTLM0)**

Drive 0 Data Read/Write Active Timing Register (R/W)

bit 7–4: Data read active count

<u>0000</u>	<u>16 clocks</u>
0001	2 clocks
0010	2 clocks
0011	3 clocks
0100	4 clocks
0101	5 clocks
0110	6 clocks
0111	7 clocks
1000	8 clocks
1001	9 clocks
1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	13 clocks
1110	14 clocks
1111	15 clocks

bit 3–0: Data write active count

<u>0000</u>	<u>16 clocks</u>
0001	2 clocks
0010	2 clocks
0011	3 clocks

0100	4 clocks
0101	5 clocks
0110	6 clocks
0111	7 clocks
1000	8 clocks
1001	9 clocks
1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	13 clocks
1110	14 clocks
1111	15 clocks

**RX55 (ARTIM1)**

Drive 1 Address Setup/Data Recovery Timing Register (R/W)

bit 7–6:	address set up count
<u>00</u>	<u>3 clocks</u>
01	1 clocks
10	2 clocks
11	4 clocks
bit 5–4:	reserved
bit 3–0:	Data (1F0h) recovery count
<u>0000</u>	<u>16 clocks (read/write)</u>
0001	4 clocks (read) 5 clocks (write)
0010	4 clocks (read) 5 clock (write)
0011	5 clocks (read/write)
0100	6 clocks (read/write)
0101	7 clocks (read/write)
0110	8 clocks (read/write)
0111	9 clocks (read/write)
1000	10 clocks (read/write)
1001	11 clocks (read/write)
1010	12 clocks (read/write)
1011	13 clocks (read/write)



1100	14 clocks (read/write)
1101	15 clocks (read/write)
1110	16 clocks (read/write)
1111	17 clocks (read/write)

**RX56 (DRWTIM1)**

Drive 1 Data Read/Write Active Timing Register (R/W)

bit 7–4: Data read active count

0000 16 clocks

0001 2 clocks

0010 2 clocks

0011 3 clocks

0100 4 clocks

0101 5 clocks

0110 6 clocks

0111 7 clocks

1000 8 clocks

1001 9 clocks

1010 10 clocks

1011 11 clocks

1100 12 clocks

1101 13 clocks

1110 14 clocks

1111 15 clocks

bit 3–0: Data write active count

0000 16 clocks

0001 2 clocks

0010 2 clocks

0011 3 clocks

0100 4 clocks

0101 5 clocks

0110 6 clocks

0111 7 clocks

1000 8 clocks

1001 9 clocks

1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	13 clocks
1110	14 clocks
1111	15 clocks

**RX57 (GR1)**

General Register #1 (R/W)

bit 7–1:	reserved
bit 0:	enable/disable 2nd IDE port
<u>0</u>	<u>disable</u>
1	enable

Bit 0 of RX57 is related to bit 0 of RX50. Refer to the description of RX50 above.

**RX58 (GR2)**

General Register #2 (R/W)

bit 7–0:	reserved
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**RX59 (BRSTLNG)**

Burst Length Control Register (R/W)

bit 7–0:	Burst length (in double words)
	<u>40h</u> (default value is 256 bytes)

## 2. SIGNAL DESCRIPTION

NAME	NO.	TYPE	DESCRIPTION
<b>CLOCK AND RESET</b>			
CLKIN	89	I	Input clock to the W83769. This clock has the same frequency as the local bus clock.
$\overline{\text{RESET}}$	88	I	Reset pin from local bus to reset the chip.
IDEACT	87	I	Chip enable pin. When set high, the W83769 is enabled after reset. When set low, the W83769 is disabled.
<b>HOST INTERFACE</b>			
$\overline{\text{FRAME}}$	12	I	$\overline{\text{FRAME}}$ is driven by the current master to indicate the beginning and duration of an access. While $\overline{\text{FRAME}}$ is asserted, data transaction continues. When $\overline{\text{FRAME}}$ is de-asserted, the transaction is in the final data phase.
$\overline{\text{IRDY}}$	13	I	$\overline{\text{IRDY}}$ indicates the PCI bus master can complete the current data phase of the transaction.
$\overline{\text{TRDY}}$	14	B	$\overline{\text{TRDY}}$ indicates the PCI bus slave can complete the current data phase of the transaction.
$\overline{\text{DEVSEL}}$	17	O	The W83769 drives this signal active to indicate that it has decoded its address as the target of the current access.
$\overline{\text{STOP}}$	18	B	$\overline{\text{STOP}}$ indicates the W83769 is requesting that the current master stop the current transaction.
IDSEL	1	I	IDSEL is asserted by PCI system to select the W83769 during configuration read and write transactions.
PAR	20	B	The W83769 drives PAR in read data phases for parity checking.
HIRQ	79	O	IRQ14 output to the system chip set.
$\overline{\text{CBE0-3}}$	31, 21, 11, 100	I	These inputs are the multiplexed Bus Command and Byte Enable signals on the PCI bus.
IRQL	85	I	The IRQL pin controls the polarity of the HIRQ output. When this pin is tied high, the polarity of HIRQ will follow that of DIRQ (pin 50). When this pin is tied low, the polarity of HIRQ will be the reverse of that of DIRQ.
$\overline{\text{PERR}}$	19	B	The $\overline{\text{PERR}}$ pin reports data parity errors during data read phases.



Signal Description, continued

NAME	NO.	TYPE	DESCRIPTION
AD31-0	92-99, 3-10 22-29, 32-39	B	These bidirectional signals are the multiplexed Address and Data on the PCI bus.
<b>DIRECT IDE DRIVE INTERFACE</b>			
$\overline{\text{DRST}}$	78	O	Reset signal to the IDE drives.
$\overline{\text{DCS0}}$	53	B	Chip select signal for IDE drive 0, 1 task file registers 1F0H-1F7H. During power-on reset, this pin is an input.
$\overline{\text{DCS1}}$	54	B	Chip select signal for IDE drive 0, 1 task file registers 3F6H and 3F7H. During power-on reset, this pin is an input.
$\overline{\text{DCS2}}$	45	O	Chip select signal for IDE drive 2, 3 task file registers 170H-177H.
$\overline{\text{DCS3}}$	44	O	Chip select signal for IDE drive 2, 3 task file registers 376H and 377H.
DSA0-2	63, 64, 67	B	These signals are the IDE disk drive address bits 0-2. DSA0-2 are to be used together with $\overline{\text{DCS0}} - 3$ to decode the individual IDE task file registers. During power-on reset, these pins are inputs.
$\overline{\text{DIOR}}$	68	O	Disk IO read command signal to initiate a read access from IDE drives.
$\overline{\text{DIOW}}$	69	O	Disk IO write command signal to initiate a write access to IDE drives.
$\overline{\text{DIOCS16}}$	51	I	IO cycle 16-bit select input from the IDE drives. When this pin is driven low, it indicates the IDE drives are ready to send/receive a 16-bit word.
DRDY	52	I	Disk drive ready signal. Indicates that the IDE drives have completed the current command cycle.
DIRQ	50	I	Interrupt request from the IDE drives to generate the HIRQ output.
$\overline{\text{DSKCHG}}$	49	I	$\overline{\text{DSKCHG}}$ is connected to pin 34 of a floppy disk connector. This active low input pin indicates the status of port 3F7, bit 7, which is reported from the floppy disk controller.
DSD15-0	55-62, 77-70	B	16-bit disk data bus.





Signal Description, continued

NAME	NO.	TYPE	DESCRIPTION
N.C.	43, 46–48, 80–84		
VSS	2, 15, 30, 40, 42, 66, 90		
VDD	16, 41, 65, 86, 91		

## DC TEST SPECIFICATIONS

Power supply definition: VDD = +5.0 Volts +/- 5%, VSS = system ground

SYMBOL IDENTIFICATION	MINIMUM	MAXIMUM	UNIT
IDD Power supply current (static)	---	20.0	mA
IDD Power supply current (dynamic)	---	50.0	mA
LIL Low Input leakage current (inputs other than pull-up inputs) (@ VIN = VSS)	---	+/- 10	μA
LIL Low Input leakage current (inputs with pull-up structure) (@ VIN = VSS)	-300.0	10	μA
LIH High Input leakage current (inputs with pull-down structure) (@ VIN = VDD)	-300.0	10	μA
LIH High Input leakage current (inputs other than pull-down inputs) (@ VIN = VDD)	---	+/- 10	μA
ZIL Low IO Tri-State leakage current (@ VIN = VSS)	---	+/- 10	μA
ZIH High IO Tri-State leakage current (@ VIN = VDD)	---	+/- 10	μA
VIL (TTL) Logic Low Input Level	---	0.8	V
VIH (TTL) Logic High Input Level	2.0	---	V
VIL (CMOS) Logic Low Input Level	---	0.8	V
VIH (COMS) Logic High Input Level	3.5	---	V



DC Test Specifications, continued

SYMBOL IDENTIFICATION	MINIMUM	MAXIMUM	UNIT
VOL Output Logic Low Level * output sink of 8.0, 12.0, 18.0 mA		0.45	V
VOH Output Logic High Level * Output source of -8.0, -12.0, -18.0 mA	2.4		V
CIN Capacitance Input	---	10.0	pF
COUT Capacitance Output	---	10.0	pF

PCLK VIL MIN = 2.1 Volts

8 mA output drive current pins:

AD[31:0],  $\overline{\text{PERR}}$ ,  $\overline{\text{PAR}}$ 

12 mA output drive current pins:

 $\overline{\text{DEVSEL}}$ ,  $\overline{\text{HIRQ}}$ ,  $\overline{\text{TRDY}}$ ,  $\overline{\text{STOP}}$ 

18 mA output drive current pins:

 $\overline{\text{DCS0}}\text{--}\overline{\text{DCS3}}$ ,  $\overline{\text{DSA0}}\text{--}\overline{\text{DSA2}}$ ,  $\overline{\text{DSD15}}\text{--}\overline{\text{DSD0}}$ ,  $\overline{\text{DRST}}$ ,  $\overline{\text{DIOR}}$ ,  $\overline{\text{DIOW}}$ **ABSOLUTE MAXIMUM RATINGS**

PARAMETER	RATING	UNIT
Case Temperature Under Bias	-65 to 110	°C
Storage Temperature	-65 to 150	°C
Supply Voltage with Respect to Ground	-0.5 to V <sub>DD</sub> + 0.5	V
Voltage on Any Pin	-0.5 to V <sub>DD</sub> + 0.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

(See APP.doc, 3 pages)





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Note: All data and specifications are subject to change without notice.